ORDER NO. VSD9606M501B

⚠ WARNING
This service information is designed for experienced repair technicians only and is not designed for use by the general public. It does not contain warnings or cautions to advice non-technical individuals of potential dangers in attempting to service a product. Products powered by electricity should be serviced or repaired only by experienced professional technicians. Any attempt to service or repair the product or products deal with in this service manual by anyone else could result in serious injury or death.

Service Manual

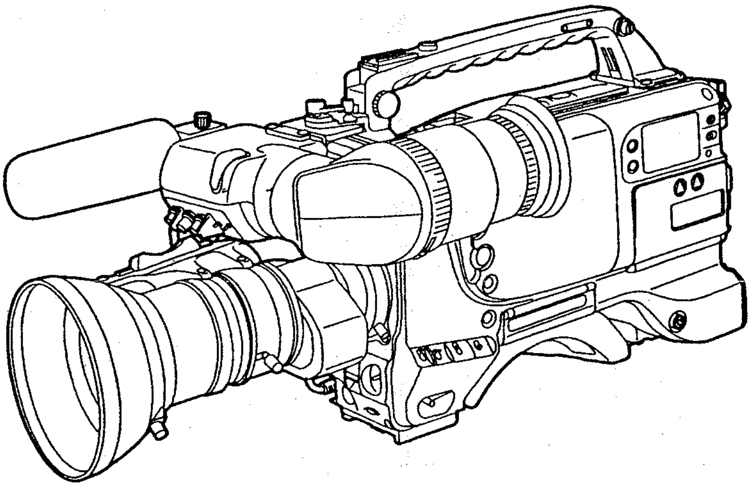
Vol. 2

DVCPRO

Sec. 1 *Block Diagrams*
Sec. 2 *Schematic Diagrams*
Sec. 3 *Circuit Board Diagrams*
Sec. 4 *IC Information*

DVCPRO Camera Recorder

AJ-D700E/EN



Panasonic

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INTRODUCTION

This service manual contains technical information which allow service personnel to understand and service the DVCPRO Camera Recorder AJ-D700E,EN.

Specifications

General

Power supply voltage: DC 12 V
Power consumption: 24 W

Operating temperature: 0°C to 40°C
Storage temperature: −20°C to 60°C
Operating humidity: Less than 85% (relative humidity)
Continuous operating time: Approx. 90 min. (using 1 Anton Bauer Trimpak 14 battery)
Weight: Approx. 5.85 kg (incld. main unit, viewfinder, lens, battery pack, tape and microphone)
Dimensions (W×H×D): 119.2×255.5 (includ. handle)×326.3 mm

Camera Section

Pick-up devices: 1/2-inch on-chip FIT type of CCD
System: RGB 3-CCD system
Picture elements: 480,000 pixel
Spectral system: F1.4 prism system
Built-in filters: 1; 3200K
2; 5600K+1/4 ND
3; 5600K
4; 5600K+1/16 ND
Quantization: 10-bit A/D (R, G and B channels), 14.4 MHz
Digital signal processing: 16-bit long operation, 14.4 MHz/28.8 MHz
Programmable gains: 3 positions can be set from among −3, 0, 3, 6, 9, 12, 15, 18, 21, 24 and 30 dB.
Shutter speeds: 1/60, 1/120, 1/250, 1/500, 1/1000 and 1/2000 sec.
Synchro scan mode; 1/29.9−1/47.6 sec., 1/51.5−1/252.0 sec.
Lens mount: 1/2″ Bayonet type
Sensitivity: F8 (2000 lux, 89.9% reflection)
Minimum subject brightness: 2 lux (F1.4, +30 dB)
Image S/N ratio: 60 dB (typical)
Horizontal resolution: 750 lines (centre)
Vertical resolution: 450 lines (normal mode)/500 lines (Super V mode)
Registration: Below 0.03% (entire range) (excld. lens)
Geometric distortion: Below measurable limit (excld. lens)

Viewfinder

CRT: 1.5 type monochrome
Resolution: 600 lines (centre)

Specifications

VTR Video System (during playback on a standard playback unit)

Bands:	Brightness; 25 Hz to 5.75 MHz +1.0 dB/−3.0 dB
S/N ratio:	55 dB
K factor (2T pulse):	Within 2%
Y/C delay:	Within 20 ns

VTR Audio System (during playback on a standard playback unit)

Sampling frequency:	48 kHz (synchronized to video)
Quantization:	16-bits/sample
Frequency response:	20 Hz to 20 kHz±1.0 dB (at reference level)
Dynamic range:	85 dB or more (at 1 kHz, AWTD)
Distortion:	Within 0.1% (at 1 kHz, operating level)
Wow/flutter:	Below measurable limit
Head room:	18 dB
Emphasis:	T1=50 µs, T2=15 µs (can be turned ON/OFF)

VTR Tape Running System

Tape speed:	33.854 mm/s
Recording/playback time:	Approx. 63 min. (using the AJ-P63MP)
FF/REW time:	Approx. 3 min. (using the AJ-P63MP)

Connectors

Input

AUDIO IN CH1/CH2 (XLR, 3-pin, male):	MIC/LINE switchable MIC; Menu setting to −60/−50/−40 dBu LINE; Menu setting to −6/0/+4 dBu
MIC IN (XLR, 3-pin, female):	Menu setting to −60/−50/−40 dBu, balanced 3 kohm
GENLOCK IN (BNC):	1.0 Vp-p, 75 ohm
TIME CODE IN (12-pin):	0.5 to 18 Vp-p, 10 kohm

Output

CAMERA OUT (BNC):	1.0 Vp-p, 75 ohm
VIDEO OUT (BNC):	1.0 Vp-p, 75 ohm
AUDIO OUT (XLR, 3-pin, female):	0 dBu, balanced, low-impedance (Menu setting to CH1/CH2/MIX)
AUDIO CH1/CH2 OUT (12-pin, TC IN/OUT combined):	−20 dBu, unbalanced, low-impedance
VTR (26-pin, option):	
TIME CODE OUT (12-pin):	1.0 Vp-p, 75 ohm
PHONES (mini-jack×2):	

Other

DC IN (XLR, 4-pin, male):	DC 11 to 17 V
DC OUT (4-pin):	DC 11 to 17 V, maximum rated current; 0.1 A
LENS (12-pin):	
REMOTE (ECU, 6-pin):	
(for AJ-D700EN)	

Accessories

Shoulder belt (1)
Sony battery connector, NP-1 screw
Video input connector (1)

Weight and dimensions shown are approximate.
Specifications are subject to change without notice.

Power supply related
AU-BP220, AU-BP402 battery packs
AG-B425 battery charger (for charging the AU-BP220 and AU-BP402 battery packs)
AU-M402H battery case
AU-B110 AC adaptor

Video cassette tapes
AJ-P6MP, AJ-P12MP, AJ-P23MP, AJ-P33MP, AJ-P63MP metal tapes

Viewfinder
5-inch viewfinder

External VTR-related
Portable video cassette recorder
AJ-YA710P time code input/output/video input adaptor
AJ-YA700P 26-pin *output connector (for connecting an external* VTR to the 26-pin interface)
AQ-EC1 extension control unit (for AJ-D700EN)
Connection cables
- for connecting an external VTR to the 26-pin interface
- for connecting an external VTR to the 14-pin/26-pin interface
- SHAN-C12TCA multi connector cable (complementary)

Audio components
AJ-MC700P microphone kit
Stereo microphone
AJ-MH700P microphone holder
WX-RA700 wireless receiver
WX-R980 camera attachment

Maintenance products
AJ-CL12MP cleaning tape
AJ-SC700 soft carrying case
SHAN-B700 carrying case (complementary)
SHAN-RC700 rain cover (complementary)

SAFETY PRECAUTIONS

GENERAL GUIDELINES

1. When servicing, observe the original lead dress. If a short circuit is found, replace all parts which have been overheated or damaged by the short circuit.
2. After servicing, see to it that all the protective devices such as insulation barriers, insulation papers shields are properly installed.
3. After servicing make the following leakage current checks to prevent the customer from being exposed to shock hazards.

LEAKAGE CURRENT COLD CHECK

1. Unplug the AC cord and connect a jumper between the two prongs on the plug.
2. Measure the resistance value, with an ohm meter, between the jumpered AC plug and each exposed metallic cabinet part on the equipment such as screwheads, connectors, control shafts, etc. When the exposed metallic part has a return path to the chassis, the reading should be between 1 MΩ and 5.2MΩ.
   When the exposed metal dose not have a return path to the chassis, the reading must be ∞.

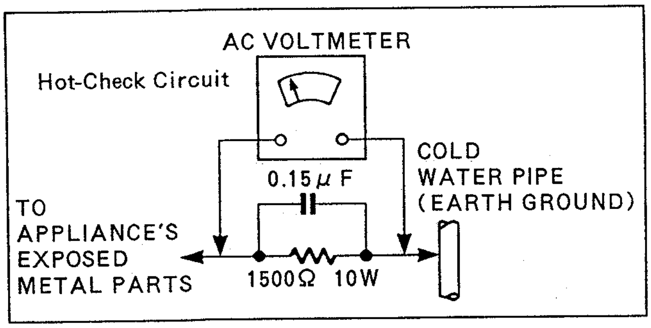


Figure 1

LEAKAGE CURRENT HOT CHECK (See Figure 1)

1. Plug the AC cord directly into the AC outlet.
   Do not use an isolation transformer for this check.
2. Connect a 1.5KΩ, 10W resistor, in parallel with 0.15μF capacitor, between each exposed metallic part on the set an a good earth ground such as a water pipe, as shown in Figure 1.
3. Use an AC voltmeter, with 1000 ohms/volt or more sensitivity, to measure the potential across the resistor.
4. Check each exposed metallic part, and measure the voltage at each point.
5. Reverse the AC plug in the AC outlet repeat each of the above measurements.
6. The potential at any point should not exceed 0.75 volts RMS. A leakage current tester (Simpson Model 229 equivalent) may be used to make the hot checks, leakage current must not exceed 1/2 milliamp. In case a measurement is outside of the limits specified, there is a possibility of a shock hazard, and the equipment should be repaired and rechecked before it is returned to the customer.

ELECTROSTATICALLY SENSITIVE (ES) DEVICES

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically sensitive (ES) Devices. Examples of typical ES devices are integrated circuits and some field-effect transistors and semiconductor "chip" components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground.
   Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ES devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded tip soldering iron to solder or unsolder ES devices.
4. Use only an anti-static solder removal device classified as "anti-static" can generate electrical charges sufficient to damage ES devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ES devices.
6. Do not remove a replacement ES device from its protective package until immediately before you are ready to install it. (most replacement ES devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive material).
7. Immediately before removing the protective material from the leads of replacement ES device, touch the protective material to the chassis or circuit assembly into which the device will be installed.
   CAUTION: Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.
8. Minimize bodily motions when handling unpackaged replacement ES devices. (Otherwise harmless mother such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ES device).

X-RADIATION

WARNING

1. The potential source of X-Radiation in EVF sets is the High Voltage section and the picture tube.
2. When using a picture tube test jig for service, ensure that jig is capable of handling 10kV without causing X-Radiation.

NOTE: It is important to use an accurate periodically calibrated high voltage meter.

3. Measure the High Voltage. The meter (electric type) reading should indicate 2.5kV, ± 0.15kV. If the meter indication is out of tolerance, immediate service and correction is required to prevent the possibility of premature component failure. To prevent an X-Radiation possibility, it is essential to use the specified picture tube.

For your safety

- **DO NOT REMOVE PANEL COVER BY UNSCREWING.**
  To reduce the risk of the electric shock, do not remove cover. No user serviceable parts inside. Refer servicing to qualified service personnel.

WARNING:

TO REDUCE THE RISK OF FIRE OR SHOCK HAZARD, DO NOT EXPOSE THIS EQUIPMENT TO RAIN OR MOISTURE.

CAUTION:

TO REDUCE THE RISK OF FIRE OR SHOCK HAZARD AND ANNOYING INTERFERENCE, USE THE RECOMMENDED ACCESSORIES ONLY.

Lithium Battery

Warning
The lithium battery in this equipment must only be replaced by qualified personnel. When necessary, contact your local Panasonic supplier.

"The lithium battery is a critical component (type number CR2032 manufactured by Panasonic).

It must never be subjected to excessive heat or discharge. It must therefore only be fitted in equipment designed specifically for its use.

Replacement batteries must be of the same type and manufacturer. They must be fitted in the same manner and location as the original battery, with the correct polarity connections observed.

Do not attempt to re-charge the old battery or re-use it for any other purpose. It should be disposed of in waste products destined for burial rather than incineration."

CAUTION

Danger of explosion if battery is incorrectly replaced.
Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

VARNING

Explosionsfara vid felaktigt batteribyte.
Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

ADVARSEL!

Eksplosionsfare ved fejlagtig håndtering.
Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

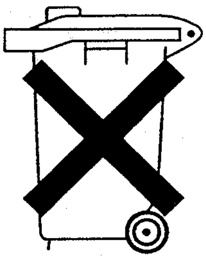
VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu.
Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyypiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

Attention/Attentie

- This apparatus contains a lithium battery for memory back-up.
- For the removal of the battery at the moment of the disposal at the end of the service life please consult your dealer.
- Do not throw away the battery. Instead, hand it in as hazardous waste.

- Dit apparaat bevat een lithiumbatterij voor memory back-up.
- Raadpleeg uw leverancier over de verwijdering van de batterij op het moment dat u het apparaat bij einde levensduur afdankt.
- Gooi de batterij niet weg, maar lever hem in als KCA.



vol.2

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Section 1. Block Diagrams
Each block diagram has a brief description.

Section 2. Schematic Diagrams

Section 3. Circuit Board Diagrams
This section includes TP & VR location.

Section 4. IC Information

SECTION 1

BLOCK DIAGRAMS

1. BLOCK DIAGRAMS

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1-2. CDS 1-2
1-3. PULSE 1-4
1-4. PRE PROCESS 1-6
1-5. CCD 1-8
1-6. CAMERA SYSCON 1-10
1-7. DSP 1-12
1-8. ENCODER 1-14
1-9. SYNC 1-16
1-10. VIDEO I/F 1-18
1-11. VTR SYSCON 1-20
1-12. SERVO 1-22
1-13. RF 1-24
1-14. VIDEO MAIN 1-26
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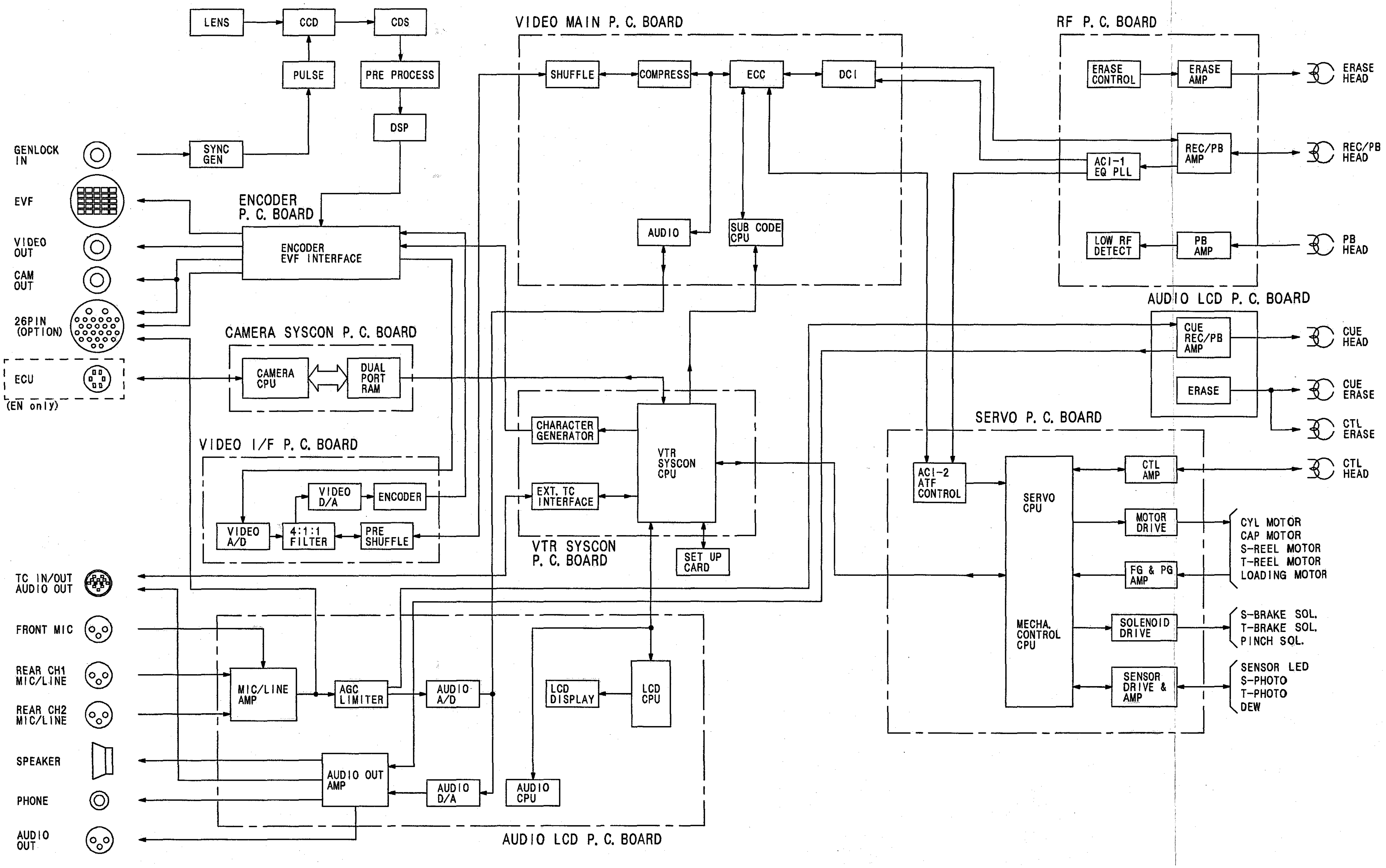
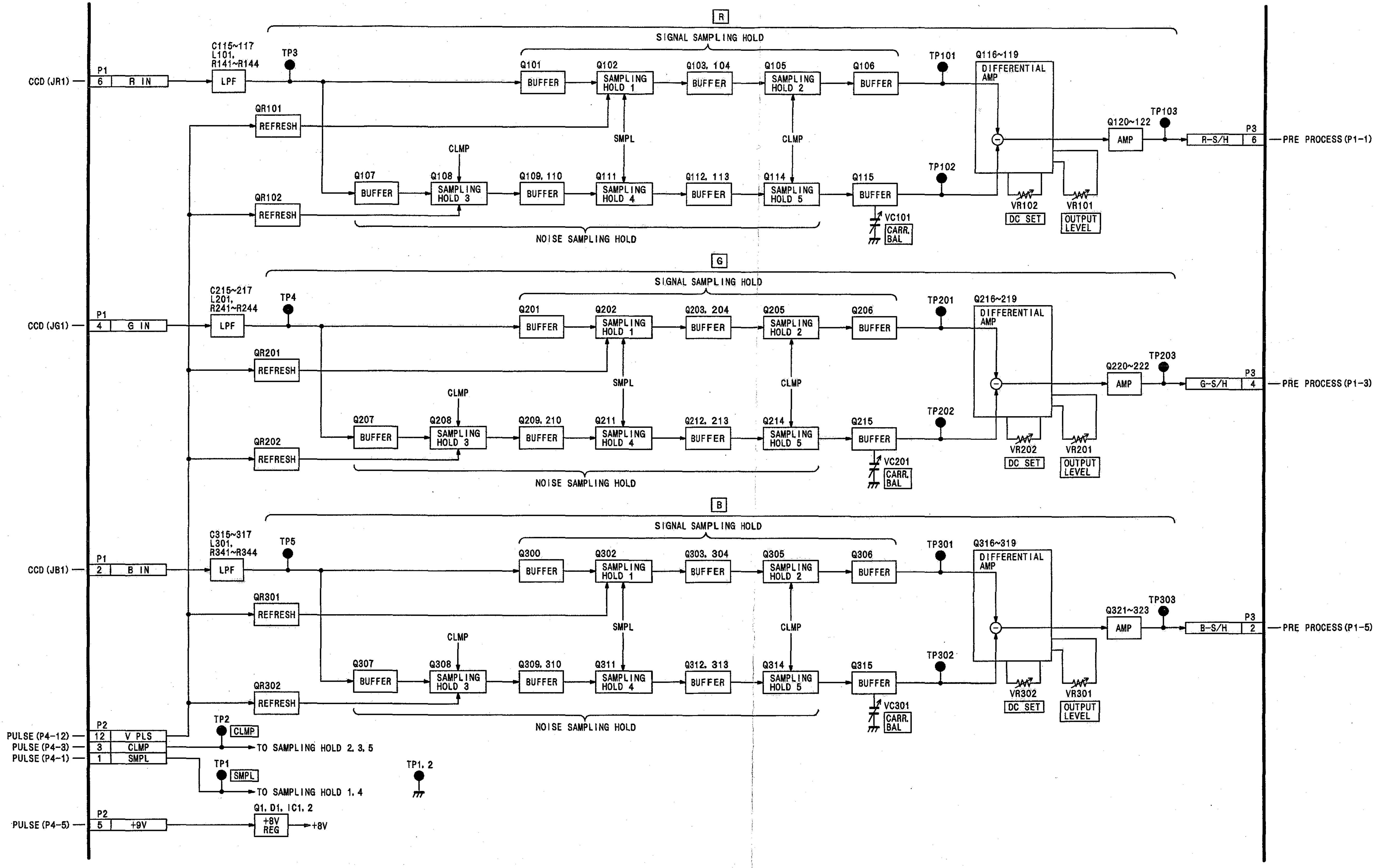
1-16. EVF 1-30

OVERALL BLOCK DIAGRAM


LENS
CCD
CDS
PULSE
PRE PROCESS
DSP
SYNC GEN
GENLOCK IN
EVF
VIDEO OUT
CAM OUT
26PIN (OPTION)
ECU
(EN only)
ENCODER P. C. BOARD
ENCODER EVF INTERFACE
CAMERA SYSCON P. C. BOARD
CAMERA CPU
DUAL PORT RAM
VIDEO I/F P. C. BOARD
VIDEO D/A
ENCODER
VIDEO A/D
4:1:1 FILTER
PRE SHUFFLE
VIDEO MAIN P. C. BOARD
SHUFFLE
COMPRESS
ECC
DCI
AUDIO
SUB CODE CPU
CHARACTER GENERATOR
EXT. TC INTERFACE
VTR SYSCON CPU
VTR SYSCON P. C. BOARD
SET UP CARD
RF P. C. BOARD
ERASE CONTROL
ERASE AMP
ERASE HEAD
REC/PB AMP
REC/PB HEAD
ACI-1 EQ PLL
LOW RF DETECT
PB AMP
PB HEAD
AUDIO LCD P. C. BOARD
CUE REC/PB AMP
CUE HEAD
ERASE
CUE ERASE
CTL ERASE
SERVO P. C. BOARD
ACI-2 ATF CONTROL
SERVO CPU
MECHA. CONTROL CPU
CTL AMP
CTL HEAD
MOTOR DRIVE
CYL MOTOR
CAP MOTOR
S-REEL MOTOR
T-REEL MOTOR
LOADING MOTOR
FG & PG AMP
SOLENOID DRIVE
S-BRAKE SOL.
T-BRAKE SOL.
PINCH SOL.
SENSOR DRIVE & AMP
SENSOR LED
S-PHOTO
T-PHOTO
DEW
TC IN/OUT AUDIO OUT
FRONT MIC
REAR CH1 MIC/LINE
REAR CH2 MIC/LINE
SPEAKER
PHONE
AUDIO OUT
MIC/LINE AMP
AGC LIMITER
AUDIO A/D
LCD DISPLAY
LCD CPU
AUDIO OUT AMP
AUDIO D/A
AUDIO CPU
AUDIO LCD P. C. BOARD

CDS BLOCK DIAGRAM


R
SIGNAL SAMPLING HOLD
CCD (JR1)
P1
6
R IN
C115~117
L101,
R141~R144
LPF
TP3
Q101
BUFFER
Q102
SAMPLING HOLD 1
Q103, 104
BUFFER
Q105
SAMPLING HOLD 2
Q106
BUFFER
TP101
Q116~119
DIFFERENTIAL AMP
QR101
REFRESH
SMPL
CLMP
Q120~122
AMP
TP103
P3
R-S/H
6
PRE PROCESS (P1-1)
CLMP
Q107
BUFFER
Q108
SAMPLING HOLD 3
Q109, 110
BUFFER
Q111
SAMPLING HOLD 4
Q112, 113
BUFFER
Q114
SAMPLING HOLD 5
Q115
BUFFER
TP102
QR102
REFRESH
VC101
CARR. BAL
VR102
DC SET
VR101
OUTPUT LEVEL
NOISE SAMPLING HOLD
G
SIGNAL SAMPLING HOLD
CCD (JG1)
P1
4
G IN
C215~217
L201,
R241~R244
LPF
TP4
Q201
BUFFER
Q202
SAMPLING HOLD 1
Q203, 204
BUFFER
Q205
SAMPLING HOLD 2
Q206
BUFFER
TP201
Q216~219
DIFFERENTIAL AMP
QR201
REFRESH
SMPL
CLMP
Q220~222
AMP
TP203
P3
G-S/H
4
PRE PROCESS (P1-3)
CLMP
Q207
BUFFER
Q208
SAMPLING HOLD 3
Q209, 210
BUFFER
Q211
SAMPLING HOLD 4
Q212, 213
BUFFER
Q214
SAMPLING HOLD 5
Q215
BUFFER
TP202
QR202
REFRESH
VC201
CARR. BAL
VR202
DC SET
VR201
OUTPUT LEVEL
NOISE SAMPLING HOLD
B
SIGNAL SAMPLING HOLD
CCD (JB1)
P1
2
B IN
C315~317
L301,
R341~R344
LPF
TP5
Q300
BUFFER
Q302
SAMPLING HOLD 1
Q303, 304
BUFFER
Q305
SAMPLING HOLD 2
Q306
BUFFER
TP301
Q316~319
DIFFERENTIAL AMP
QR301
REFRESH
SMPL
CLMP
Q321~323
AMP
TP303
P3
B-S/H
2
PRE PROCESS (P1-5)
CLMP
Q307
BUFFER
Q308
SAMPLING HOLD 3
Q309, 310
BUFFER
Q311
SAMPLING HOLD 4
Q312, 313
BUFFER
Q314
SAMPLING HOLD 5
Q315
BUFFER
TP302
QR302
REFRESH
VC301
CARR. BAL
VR302
DC SET
VR301
OUTPUT LEVEL
NOISE SAMPLING HOLD
P2
PULSE (P4-12)
12
V PLS
PULSE (P4-3)
3
CLMP
PULSE (P4-1)
1
SMPL
TP2
CLMP
TO SAMPLING HOLD 2, 3, 5
TP1
SMPL
TO SAMPLING HOLD 1, 4
TP1, 2
P2
PULSE (P4-5)
5
+9V
Q1, D1, IC1, 2
+8V REG
+8V

CDS P.C.Board

CDS is the abbreviation of Correlated Double Sampling which smoothes CCD outputs.

Input signal, **R IN,** from CCD P.C.Board is processed with **LPF.** After that it has two ways. Upper one is for signal component process, lower one is for noise component.

In upper way the sample pulse,**SMPL,** samples and holds the charge level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of signal component.

In lower way the sample pulse,**SMPL,** samples and holds the noise level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of noise component.

The difference between signal component and noise component is output to Pre Process P.C.Board as **R-S/H.**

VC101 is the VR to minimize career leak. **VR102** adjusts DC level, and **VR101** does output level.

Input signal, **G IN,** from CCD P.C.Board is processed with **LPF.** After that it has two ways. Upper one is for signal component process, lower one is for noise component.

In upper way the sample pulse,**SMPL,** samples and holds the charge level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of signal component.

In lower way the sample pulse,**SMPL,** samples and holds the noise level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of noise component.

The difference between signal component and noise component is output to Pre Process P.C.Board as **G-S/H.**

VC201 is the VR to minimize career leak. **VR202** adjusts DC level, and **VR201** does output level.

Input signal, **B IN,** from CCD P.C.Board is processed with **LPF.** After that it has two ways. Upper one is for signal component process, lower one is for noise component.

In upper way the sample pulse,**SMPL,** samples and holds the charge level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of signal component.

In lower way the sample pulse,**SMPL,** samples and holds the noise level of signal component. The clamp pulse,**CLMP,** samples and holds the pedestal level of noise component.

The difference between signal component and noise component is output to Pre Process P.C.Board as **B-S/H.**

VC301 is the VR to minimize career leak. **VR302** adjusts DC level, and **VR301** does output level.

Pulse P.C.Board

This circuit makes those pulses which drive CCD.

IC2 makes V-CCD Drive Pulse of **VA1～VA4,VB1～VB4,**Charge Pulse of **CH1,CH2** and Shutter Pulse of **CHS** from V Drive Pulse **CCD VD** supplied from Sync P.C.Board. Shutter speed is controlled by **SHUT A,SHUT B** and **SHUT C.** The logic table is located on the top left of the diagram.

SLOW SHUTTER of **IC7,IC8** and **IC9** make the shutter pulse used in 1/50 of shutter speed. V-CCD Drive Pulses are supplied to CCD P.C.Board as **XVA1～XVA2、XVB1～XVB4.**

VR14 can shift H Drive, **CCD HD**, to change moduration.

The PLL which is composed of phase comparator in **IC2** and oscillator **X1** generates H-CCD Drive Pulse **H12** and **H34** in **IC1** locked to **CCD HD.** These are supplied to CCD P.C.Board as **XH1、XH2.**

Reset Pulse of**XR**, Clamp Pulse of **CLMP** and Sample Pulse of **SMPL** are generated in the same way and supplied to CCD P.C.Board.

OG Voltage of R/G/B depend on **VR10,VR11** and **VR12.** SUB Voltage depend on **VR7,VR8** and **VR9.**

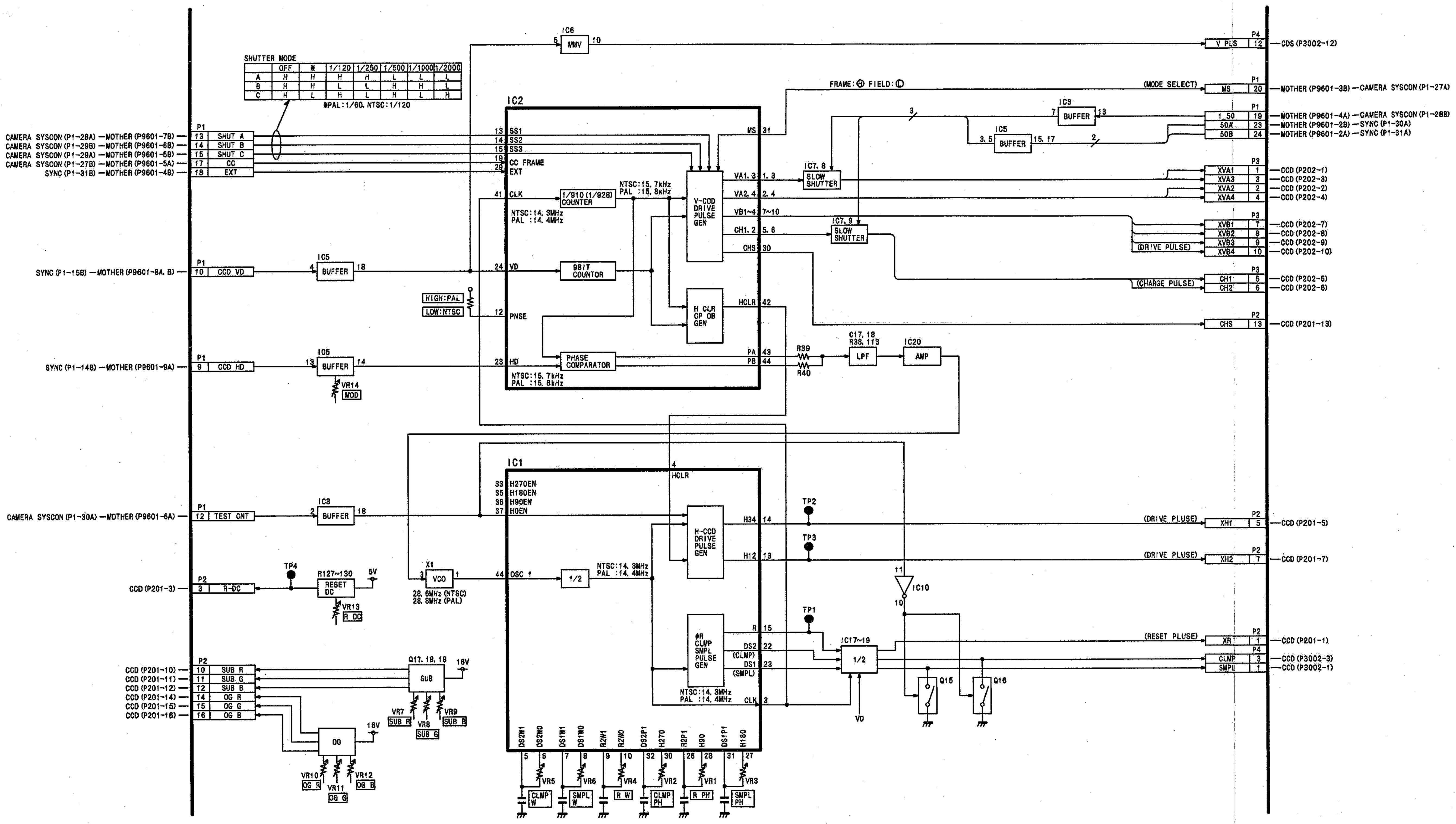
The width and phase of Sample Pulse are adjusted with **VR6** and **VR3.**

The width and Phase of Clamp Pulse are adjusted with **VR5** and **VR2.**

The width and Phase of Reset Pulse are adjusted with **VR4** and **VR1.**

DC voltage of Reset Pulse is adjusted with **VR13.**

PULSE BLOCK DIAGRAM

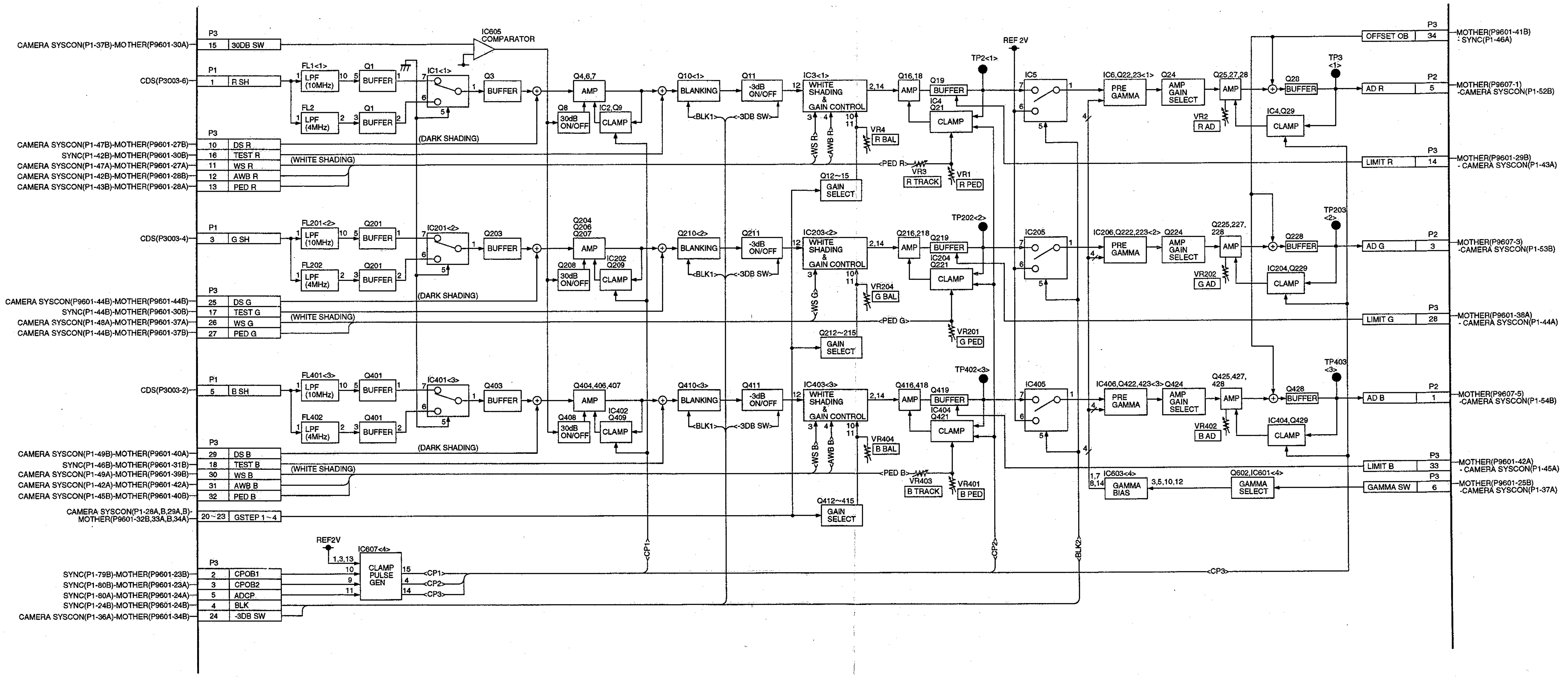

IC6
MMV
IC2
SS1
SS2
SS3
CC FRAME
EXT
CLK
1/910 (1/928) COUNTER
NTSC:14. 3MHz
PAL :14. 4MHz
NTSC:15. 7kHz
PAL :15. 8kHz
V-CCD DRIVE PULSE GEN
VD
9BIT COUNTOR
PNSE
HIGH:PAL
LOW:NTSC
H CLR CP OB GEN
HD
PHASE COMPARATOR
MS
VA1. 3
VA2. 4
VB1~4
CH1. 2
CHS
HCLR
PA
PB
R39
R40
C17. 18
R38. 113
LPF
IC20
AMP
FRAME: Ⓗ FIELD: Ⓛ
(MODE SELECT)
IC3
BUFFER
IC5
BUFFER
IC7. 8
SLOW SHUTTER
IC7. 9
SLOW SHUTTER
(DRIVE PULSE)
(CHARGE PULSE)
CAMERA SYSCON (P1-28A) —MOTHER (P9601-7B)
CAMERA SYSCON (P1-29B) —MOTHER (P9601-6B)
CAMERA SYSCON (P1-29A) —MOTHER (P9601-5B)
CAMERA SYSCON (P1-27B) —MOTHER (P9601-5A)
SYNC (P1-31B) —MOTHER (P9601-4B)
P1 13 SHUT A
14 SHUT B
15 SHUT C
17 CC
18 EXT
SYNC (P1-15B) —MOTHER (P9601-8A. B)
P1 10 CCD VD
SYNC (P1-14B) —MOTHER (P9601-9A)
P1 9 CCD HD
VR14
MOD
CAMERA SYSCON (P1-30A) —MOTHER (P9601-6A)
P1 12 TEST CNT
CCD (P201-3)
P2 3 R-DC
TP4
R127~130
RESET DC
5V
VR13
R DC
X1
VCO
28. 6MHz (NTSC)
28. 8MHz (PAL)
CCD (P201-10)
CCD (P201-11)
CCD (P201-12)
CCD (P201-14)
CCD (P201-15)
CCD (P201-16)
P2 10 SUB R
11 SUB G
12 SUB B
14 OG R
15 OG G
16 OG B
Q17. 18. 19
SUB
16V
VR7 SUB R
VR8 SUB G
VR9 SUB B
OG
VR10 OG R
VR11 OG G
VR12 OG B
IC1
H270EN
H180EN
H90EN
H0EN
OSC 1
1/2
HCLR
H-CCD DRIVE PULSE GEN
H34
H12
ϕR CLMP SMPL PULSE GEN
R
DS2 (CLMP)
DS1 (SMPL)
CLK
TP1
TP2
TP3
IC10
IC17~19
1/2
VD
Q15
Q16
DS2W1
DS2W0
DS1W1
DS1W0
R2W1
R2W0
DS2P1
H270
R2P1
H90
DS1P1
H180
VR5 CLMP W
VR6 SMPL W
VR4 R W
VR2 CLMP PH
VR1 R PH
VR3 SMPL PH
P4 V PLS 12 —CDS (P3002-12)
P1 MS 20 —MOTHER (P9601-3B) —CAMERA SYSCON (P1-27A)
P1 1_50 19 —MOTHER (P9601-4A) —CAMERA SYSCON (P1-28B)
50A 23 —MOTHER (P9601-2B) —SYNC (P1-30A)
50B 24 —MOTHER (P9601-2A) —SYNC (P1-31A)
P3 XVA1 1 —CCD (P202-1)
XVA3 3 —CCD (P202-3)
XVA2 2 —CCD (P202-2)
XVA4 4 —CCD (P202-4)
P3 XVB1 7 —CCD (P202-7)
XVB2 8 —CCD (P202-8)
XVB3 9 —CCD (P202-9)
XVB4 10 —CCD (P202-10)
P3 CH1 5 —CCD (P202-5)
CH2 6 —CCD (P202-6)
P2 CHS 13 —CCD (P201-13)
(DRIVE PLUSE) P2 XH1 5 —CCD (P201-5)
(DRIVE PLUSE) P2 XH2 7 —CCD (P201-7)
(RESET PLUSE) P2 XR 1 —CCD (P201-1)
P4 CLMP 3 —CCD (P3002-3)
SMPL 1 —CCD (P3002-1)

SHUTTER MODE

	OFF	*	1/120	1/250	1/500	1/1000	1/2000
A	H	H	H	H	L	L	L
B	H	H	L	L	H	H	L
C	H	L	H	L	H	L	H

*PAL:1/60. NTSC:1/120

PRE PROCESS BLOCK DIAGRAM


CAMERA SYSCON(P1-37B)-MOTHER(P9601-30A)
P3 15 30DB SW
CDS(P3003-6)
P1 1 R SH
FL1<1> LPF (10MHz)
FL2 LPF (4MHz)
Q1 BUFFER
IC1<1>
Q3 BUFFER
(DARK SHADING)
IC605 COMPARATOR
Q4,6,7 AMP
Q8 30dB ON/OFF
IC2,Q9 CLAMP
Q10<1> BLANKING
Q11 -3dB ON/OFF
<BLK1>
<-3DB SW>
IC3<1> WHITE SHADING & GAIN CONTROL
<WS R>
<AWB R>
VR4 R BAL
Q12~15 GAIN SELECT
<PED R>
VR3 R TRACK
VR1 R PED
Q16,18 AMP
Q19 BUFFER
IC4 Q21 CLAMP
TP2<1>
REF 2V
IC5
IC6,Q22,23<1> PRE GAMMA
Q24 AMP GAIN SELECT
Q25,27,28 AMP
VR2 R AD
Q28 BUFFER
IC4,Q29 CLAMP
TP3 <1>
OFFSET OB P3 34
MOTHER(P9601-41B) - SYNC(P1-46A)
AD R P2 5
MOTHER(P9607-1) -CAMERA SYSCON(P1-52B)
LIMIT R P3 14
MOTHER(P9601-29B) - CAMERA SYSCON(P1-43A)
CAMERA SYSCON(P1-47B)-MOTHER(P9601-27B) P3 10 DS R
SYNC(P1-42B)-MOTHER(P9601-30B) 16 TEST R
CAMERA SYSCON(P1-47A)-MOTHER(P9601-27A) 11 WS R
CAMERA SYSCON(P1-42B)-MOTHER(P9601-28B) 12 AWB R
CAMERA SYSCON(P1-43B)-MOTHER(P9601-28A) 13 PED R
(WHITE SHADING)
CDS(P3003-4)
P1 3 G SH
FL201<2> LPF (10MHz)
FL202 LPF (4MHz)
Q201 BUFFER
IC201<2>
Q203 BUFFER
Q204 Q206 Q207 AMP
Q208 30dB ON/OFF
IC202 Q209 CLAMP
Q210<2> BLANKING
Q211 -3dB ON/OFF
IC203<2> WHITE SHADING & GAIN CONTROL
<WS G>
VR204 G BAL
Q212~215 GAIN SELECT
<PED G>
VR201 G PED
Q216,218 AMP
Q219 BUFFER
IC204 Q221 CLAMP
TP202<2>
IC205
IC206,Q222,223<2> PRE GAMMA
Q224 AMP GAIN SELECT
Q225,227, 228 AMP
VR202 G AD
Q228 BUFFER
IC204,Q229 CLAMP
TP203 <2>
AD G P2 3
MOTHER(P9607-3) -CAMERA SYSCON(P1-53B)
LIMIT G P3 28
MOTHER(P9601-38A) - CAMERA SYSCON(P1-44A)
CAMERA SYSCON(P9601-44B)-MOTHER(P9601-44B) P3 25 DS G
SYNC(P1-44B)-MOTHER(P9601-30B) 17 TEST G
CAMERA SYSCON(P1-48A)-MOTHER(P9601-37A) 26 WS G
CAMERA SYSCON(P1-44B)-MOTHER(P9601-37B) 27 PED G
CDS(P3003-2)
P1 5 B SH
FL401<3> LPF (10MHz)
FL402 LPF (4MHz)
Q401 BUFFER
IC401<3>
Q403 BUFFER
Q404,406,407 AMP
Q408 30dB ON/OFF
IC402 Q409 CLAMP
Q410<3> BLANKING
Q411 -3dB ON/OFF
IC403<3> WHITE SHADING & GAIN CONTROL
<WS B>
<AWB B>
VR404 B BAL
Q412~415 GAIN SELECT
<PED B>
VR403 B TRACK
VR401 B PED
Q416,418 AMP
Q419 BUFFER
IC404 Q421 CLAMP
TP402<3>
IC405
IC406,Q422,423<3> PRE GAMMA
Q424 AMP GAIN SELECT
Q425,427, 428 AMP
VR402 B AD
Q428 BUFFER
IC404,Q429 CLAMP
TP403 <3>
AD B P2 1
MOTHER(P9607-5) -CAMERA SYSCON(P1-54B)
LIMIT B P3 33
MOTHER(P9601-42A) - CAMERA SYSCON(P1-45A)
IC603<4> GAMMA BIAS
1,7 8,14
3,5,10,12
Q602,IC601<4> GAMMA SELECT
GAMMA SW P3 6
MOTHER(P9601-25B) -CAMERA SYSCON(P1-37A)
CAMERA SYSCON(P1-49B)-MOTHER(P9601-40A) P3 29 DS B
SYNC(P1-46B)-MOTHER(P9601-31B) 18 TEST B
CAMERA SYSCON(P1-49A)-MOTHER(P9601-39B) 30 WS B
CAMERA SYSCON(P1-42A)-MOTHER(P9601-42A) 31 AWB B
CAMERA SYSCON(P1-45B)-MOTHER(P9601-40B) 32 PED B
CAMERA SYSCON(P1-28A,B,29A,B)-MOTHER(P9601-32B,33A,B,34A) 20~23 GSTEP 1~4
REF2V
IC607<4> CLAMP PULSE GEN
1,3,13
<CP1>
<CP2>
<CP3>
<BLK2>
SYNC(P1-79B)-MOTHER(P9601-23B) P3 2 CPOB1
SYNC(P1-80B)-MOTHER(P9601-23A) 3 CPOB2
SYNC(P1-80A)-MOTHER(P9601-24A) 5 ADCP
SYNC(P1-24B)-MOTHER(P9601-24B) 4 BLK
CAMERA SYSCON(P1-36A)-MOTHER(P9601-34B) 24 -3DB SW

Pre Process P.C.Board

This circuit processes Dark Shading, White Shading, Pre Gamma and so on.

R S/H supplied from CDS P.C.Board is input to LPF,**FL1.**

Dark Shading,**DS R,** is added to the output from **IC1.** When 30dB is selected in Gain, the signal is amplified at **Q4、6 and 7. TEST R** is a RAMP signal for test .

IC3 processes White Shading with **WS R** and Auto White Balance with **AWB R,** besides of Gain Control. **VR1** adjusts pedestal level. **VR3** adjusts pedestal tracking.

IC5 processes Blanking. **IC6、Q22** and **Q23** process Pre Gamma. **VR2** adjusts the level required before A/D conversion. Finally the signal is output to DSP P.C.Board as **AD R.**

G S/H supplied from CDS P.C.Board is input to LPF,**FL201.**

Dark Shading,**DS G,** is added to the output from **IC201.** When 30dB is selected in Gain, the signal is amplified at **Q204、206 and 207. TEST G** is a RAMP signal for test.

IC203 processes White Shading with **WS G** besides of Gain Control. **VR201** adjusts pedestal level.

IC205 processes Blanking. **IC206、Q222** and **Q223** process Pre Gamma. **VR202** adjusts the level required before A/D conversion. Finally the signal is output to DSP P.C.Board as **AD G.**

B S/H supplied from CDS P.C.Board is input to LPF,**FL401.**

Dark Shading,**DS B,** is added to the output from **IC401.** When 30dB is selected in Gain, the signal is amplified at **Q404、406 and 407. TEST B** is a RAMP signal for test.

IC403 processes White Shading with **WS B** and Auto White Balance with **AWB B,** besides of Gain Control. **VR401** adjusts pedestal level. **VR403** adjusts pedestal tracking.

IC405 processes Blanking. **IC406、Q422** and **Q423** process Pre Gamma. **VR402** adjusts the level required before A/D conversion. Finally the signal is output to DSP P.C.Board as **AD B.**

CCD P.C.Board

This Board has three CCDs and CCD drive circuits for RGB processes.

IC101 and **IC102** make the drive pulses for R CCD.

XVA1~4 generated in Pulse P.C.Board are input to **IC101**. Those pulses become V-CCD Drive Pulses for image area **(A1R~A4R)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V).

XVB1~4 generated in Pulse P.C.Board are input to **IC102.** Those pulses become V-CCD Drive Pulses for storage area **(B1R~B4R)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V). **A1R~A4R** and **B1R~B4R** are supplied to **IC103,R CCD**.

CH1 and **CH2** are charge pulses and added to V-CCD Drive Pulses for image area. **CHS** is shutter pulse and becomes a pulse of 21V in **IC101**. This is added to SUB voltage, **SUB R,** and supplied to **IC103, R CCD**. H-CCD Drive Pulses, **H1R** and **H2R,** are generated in **IC208** from **XH1** and **XH2** and supplied to **IC103, R CCD**. Reset Pulse is generated in **IC207** from **XR** and **R DC** and supplied to **IC103, R CCD**. The output signal from **R CCD** is supplied to CDS P.C.Board via connector **JR**.

IC201 and **IC202** make the drive pulses for G CCD.

XVA1~4 generated in Pulse P.C.Board are input to **IC201**. Those pulses become V-CCD Drive Pulses for image area **(A1G~A4G)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V).

XVB1~4 generated in Pulse P.C.Board are input to **IC202.** Those pulses become V-CCD Drive Pulses for storage area **(B1G~B4G)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V). **A1G~A4G** and **B1G~B4G** are supplied to **IC203,G CCD**.

CH1 and **CH2** are charge pulses and added to V-CCD Drive Pulses for image area. **CHS** is shutter pulse and becomes a pulse of 21V in **IC201**. This is added to SUB voltage, **SUB G,** and supplied to **IC203, G CCD**. H-CCD Drive Pulses, **H1G** and **H2G,** are generated in **IC208** from **XH1** and **XH2** and supplied to **IC203, G CCD**. Reset Pulse is generated in **IC207** from **XR** and **R DC** and supplied to **IC203, G CCD**. The output signal from **G CCD** is supplied to CDS P.C.Board via connector **JG**.

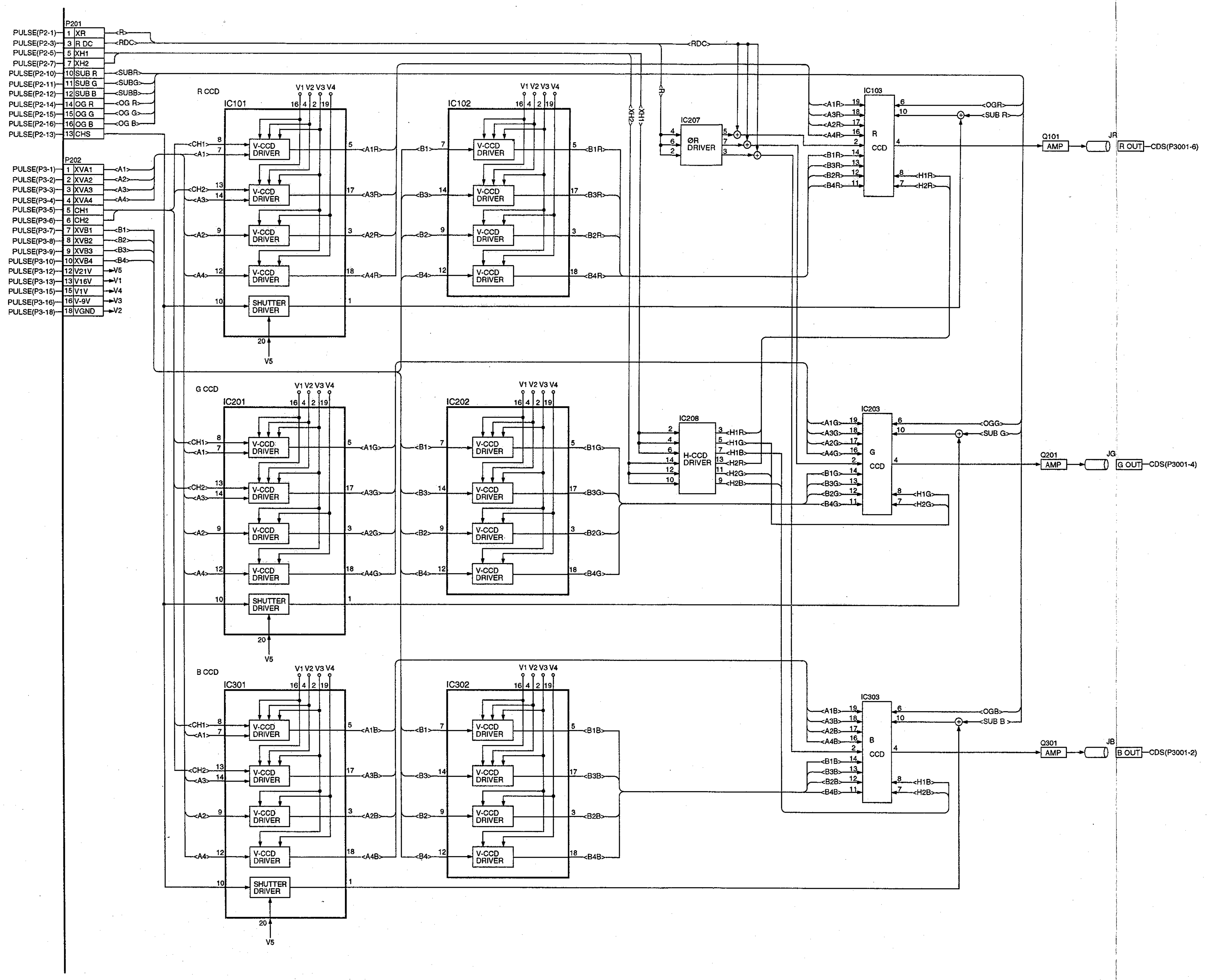
IC301 and **IC302** make the drive pulses for B CCD.

XVA1~4 generated in Pulse P.C.Board are input to **IC301**. Those pulses become V-CCD Drive Pulses for image area **(A1B~A4B)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V).

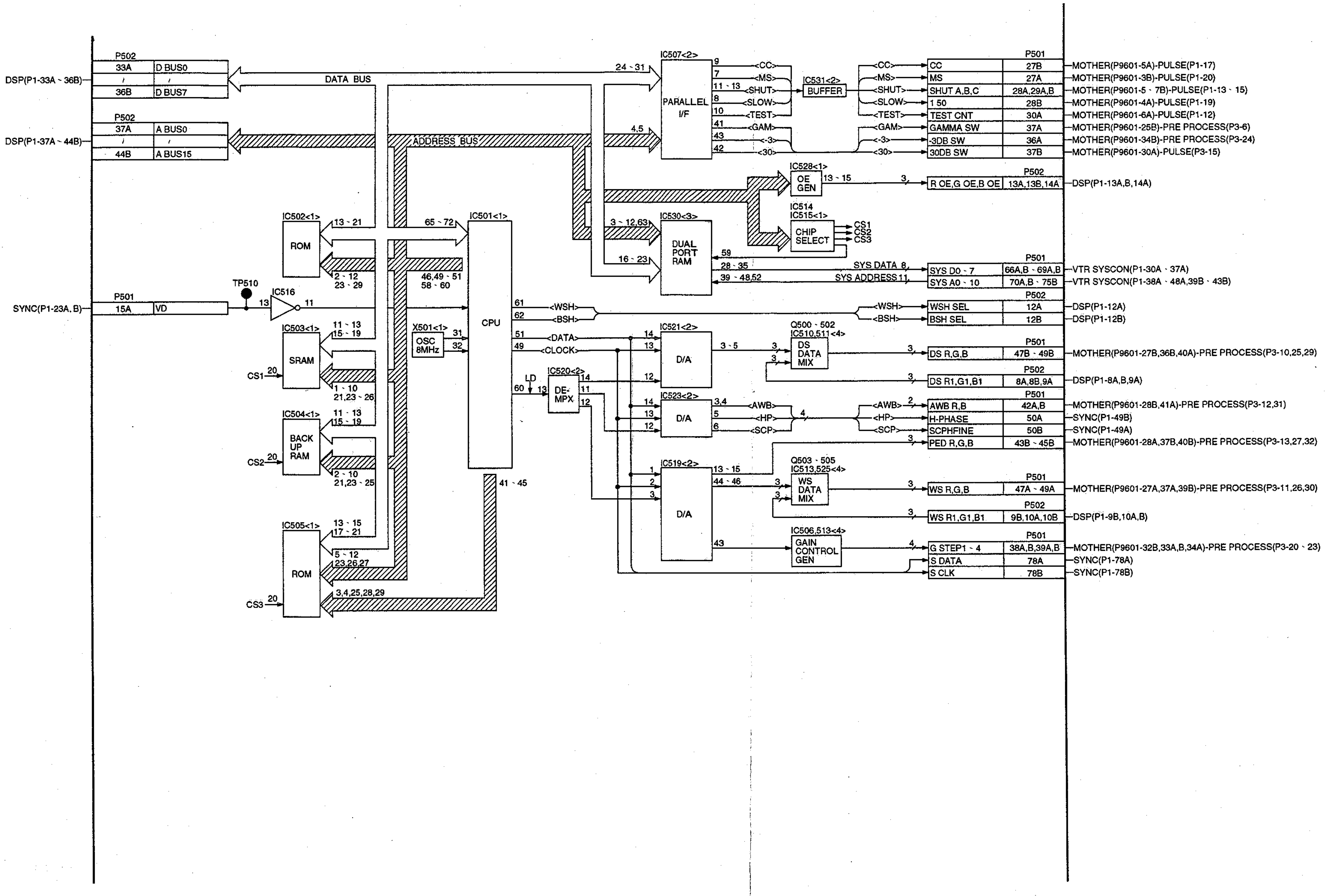
XVB1~4 generated in Pulse P.C.Board are input to **IC302.** Those pulses become V-CCD Drive Pulses for storage area **(B1B~B4B)** with **V1**(16V),**V2**(GND),**V3**(-9V) and **V4**(1V). **A1B~A4B** and **B1B~B4B** are supplied to **IC303,B CCD**.

CH1 and **CH2** are charge pulses and added to V-CCD Drive Pulses for image area. **CHS** is shutter pulse and becomes a pulse of 21V in **IC301**. This is added to SUB voltage, **SUB B,** and supplied to **IC303, B CCD**. H-CCD Drive Pulses, **H1B** and **H2B,** are generated in **IC208** from **XH1** and **XH2** and supplied to **IC303, B CCD**. Reset Pulse is generated in **IC207** from **XR** and **R DC** and supplied to **IC303, B CCD**. The output signal from **B CCD** is supplied to CDS P.C.Board via connector **JB**.

CCD BLOCK DIAGRAM


P201
PULSE(P2-1) 1 XR <R>
PULSE(P2-3) 3 R DC <RDC>
PULSE(P2-5) 5 XH1
PULSE(P2-7) 7 XH2
PULSE(P2-10) 10 SUB R <SUBR>
PULSE(P2-11) 11 SUB G <SUBG>
PULSE(P2-12) 12 SUB B <SUBB>
PULSE(P2-14) 14 OG R <OG R>
PULSE(P2-15) 15 OG G <OG G>
PULSE(P2-16) 16 OG B <OG B>
PULSE(P2-13) 13 CHS
P202
PULSE(P3-1) 1 XVA1 <A1>
PULSE(P3-2) 2 XVA2 <A2>
PULSE(P3-3) 3 XVA3 <A3>
PULSE(P3-4) 4 XVA4 <A4>
PULSE(P3-5) 5 CH1
PULSE(P3-6) 6 CH2
PULSE(P3-7) 7 XVB1 <B1>
PULSE(P3-8) 8 XVB2 <B2>
PULSE(P3-9) 9 XVB3 <B3>
PULSE(P3-10) 10 XVB4 <B4>
PULSE(P3-12) 12 V21V V5
PULSE(P3-13) 13 V16V V1
PULSE(P3-15) 15 V1V V4
PULSE(P3-16) 16 V-9V V3
PULSE(P3-18) 18 VGND V2
R CCD
G CCD
B CCD
IC101
IC102
IC201
IC202
IC301
IC302
V1 V2 V3 V4
16 4 2 19
<CH1>
<A1>
<CH2>
<A3>
<A2>
<A4>
V-CCD DRIVER
SHUTTER DRIVER
20
V5
<A1R>
<A3R>
<A2R>
<A4R>
<B1>
<B3>
<B2>
<B4>
<B1R>
<B3R>
<B2R>
<B4R>
<A1G>
<A3G>
<A2G>
<A4G>
<B1G>
<B3G>
<B2G>
<B4G>
<A1B>
<A3B>
<A2B>
<A4B>
<B1B>
<B3B>
<B2B>
<B4B>
<RDC>
<R>
<XH2>
<XH1>
IC207
ØR DRIVER
IC208
H-CCD DRIVER
<H1R>
<H1G>
<H1B>
<H2R>
<H2G>
<H2B>
IC103
R CCD
<OGR>
<SUB R>
IC203
G CCD
<OGG>
<SUB G>
IC303
B CCD
<OGB>
<SUB B>
Q101
AMP
JR
R OUT
CDS(P3001-6)
Q201
AMP
JG
G OUT
CDS(P3001-4)
Q301
AMP
JB
B OUT
CDS(P3001-2)

CAMERA SYSCON BLOCK DIAGRAM



DSP(P1-33A ~ 36B)
P502
33A
D BUS0
36B
D BUS7
DATA BUS
DSP(P1-37A ~ 44B)
37A
A BUS0
44B
A BUS15
ADDRESS BUS
SYNC(P1-23A, B)
P501
15A
VD
TP510
IC516
IC502<1>
ROM
13 ~ 21
2 ~ 12
23 ~ 29
IC503<1>
SRAM
11 ~ 13
15 ~ 19
1 ~ 10
21,23 ~ 26
CS1
IC504<1>
BACK UP RAM
CS2
2 ~ 10
21,23 ~ 25
IC505<1>
ROM
13 ~ 15
17 ~ 21
5 ~ 12
23,26,27
3,4,25,28,29
CS3
IC501<1>
CPU
65 ~ 72
46,49 ~ 51
58 ~ 60
X501<1>
OSC 8MHz
41 ~ 45
<WSH>
<BSH>
<DATA>
<CLOCK>
LD
IC520<2>
DE-MPX
IC507<2>
PARALLEL I/F
24 ~ 31
4,5
<CC>
<MS>
<SHUT>
<SLOW>
<TEST>
<GAM>
<-3>
<30>
IC531<2>
BUFFER
IC528<1>
OE GEN
13 ~ 15
IC514
IC515<1>
CHIP SELECT
CS1
CS2
CS3
IC530<3>
DUAL PORT RAM
3 ~ 12,63
16 ~ 23
28 ~ 35
39 ~ 48,52
SYS DATA 8
SYS ADDRESS 11
IC521<2>
D/A
Q500 ~ 502
IC510,511<4>
DS DATA MIX
IC523<2>
D/A
<AWB>
<HP>
<SCP>
IC519<2>
D/A
13 ~ 15
44 ~ 46
Q503 ~ 505
IC513,525<4>
WS DATA MIX
IC506,513<4>
GAIN CONTROL GEN
P501
CC 27B
MS 27A
SHUT A,B,C 28A,29A,B
1 50 28B
TEST CNT 30A
GAMMA SW 37A
-3DB SW 36A
30DB SW 37B
P502
R OE,G OE,B OE 13A,13B,14A
P501
SYS D0 ~ 7 66A,B ~ 69A,B
SYS A0 ~ 10 70A,B ~ 75B
P502
WSH SEL 12A
BSH SEL 12B
P501
DS R,G,B 47B ~ 49B
P502
DS R1,G1,B1 8A,8B,9A
P501
AWB R,B 42A,B
H-PHASE 50A
SCPHFINE 50B
PED R,G,B 43B ~ 45B
P501
WS R,G,B 47A ~ 49A
P502
WS R1,G1,B1 9B,10A,10B
P501
G STEP1 ~ 4 38A,B,39A,B
S DATA 78A
S CLK 78B
MOTHER(P9601-5A)-PULSE(P1-17)
MOTHER(P9601-3B)-PULSE(P1-20)
MOTHER(P9601-5 ~ 7B)-PULSE(P1-13 ~ 15)
MOTHER(P9601-4A)-PULSE(P1-19)
MOTHER(P9601-6A)-PULSE(P1-12)
MOTHER(P9601-25B)-PRE PROCESS(P3-6)
MOTHER(P9601-34B)-PRE PROCESS(P3-24)
MOTHER(P9601-30A)-PULSE(P3-15)
DSP(P1-13A,B,14A)
VTR SYSCON(P1-30A ~ 37A)
VTR SYSCON(P1-38A ~ 48A,39B ~ 43B)
DSP(P1-12A)
DSP(P1-12B)
MOTHER(P9601-27B,36B,40A)-PRE PROCESS(P3-10,25,29)
DSP(P1-8A,B,9A)
MOTHER(P9601-28B,41A)-PRE PROCESS(P3-12,31)
SYNC(P1-49B)
SYNC(P1-49A)
MOTHER(P9601-28A,37B,40B)-PRE PROCESS(P3-13,27,32)
MOTHER(P9601-27A,37A,39B)-PRE PROCESS(P3-11,26,30)
DSP(P1-9B,10A,B)
MOTHER(P9601-32B,33A,B,34A)-PRE PROCESS(P3-20 ~ 23)
SYNC(P1-78A)
SYNC(P1-78B)

Camera Syscon P.C.Board

This circuit which is composed of following ICs controls Camera unit and EVR.

IC501	SYSCON CPU
IC502	SYSCON ROM
IC504	Back-up RAM
IC507	Parallel I/F to change Mode
IC530	Dual Port RAM for communication with VTR SYSCON

IC521 is D/A converter for Dark Shading data. This is supplied to **DS DATA MIX** which is composed of **Q500** ~ **Q502**, **IC510** and **IC511**. The data is added to RGB of **DS R1,G1,B1** and output as **DS R,G,B**.

IC519 is D/A converter for White Shading data. This is supplied to **WS DATA MIX** which is composed of **Q503** ~ **Q505**, **IC513** and **IC525**. The data is added to RGB of **WS R1,G1,B1** and output as **WS R,G,B**.

The data of AWB, H phase and sub-carrier are D/A converted at **IC523**. Each of those is output as **AWB ,R B, H-PHASE** and **SCPHASE**.

DSP P.C.Board

DSP is the abbreviation of Digital Signal Processor and processes Blemish Compensation, Gamma, Knee, Masking, Detail and so on at **IC101** and **IC102.**

AD R,AD G and **AD B** supplied from Pre Process P.C.Board are A/D converted to 10bits of parallel signals at **IC4,IC5** and **IC6. VR1** adjusts the reference voltage for A/D conversion. R,G, and B converted to digital signal are supplied to **IC101.** On the other hand Dark Shading data is supplied to **IC301,SRAM,** via **IC302** and **IC305**. White Shading data is also supplied to **IC304,SRAM,** via **IC302** and **IC305.** Both are D/A converted at **IC303** and **IC306** and then supplied to Camera Syscon P.C.Board.

R、G、B input to **IC101** are processed with Blemish Compensation, Gamma, Knee and Masking. Then they are supplied to **IC102**. At the same time the detail signal made inside **IC101** are processed with Level Dependent, Dynamic Noise Suppress and Dynamic Detail at **IC102.**

1/2 pitch of CCD spatial offsets is compensated in **IC102.** Moreover Chroma Detail and Fresh(Skin) Detail are produced from R,G and B and then added to R,G and B as well as ordinary details mentioned above.

The multiplexers after 1/2 pitch of CCD spatial offsets compensation switch input signal or internal color bar.

After that Clipping and Blanking are performed.

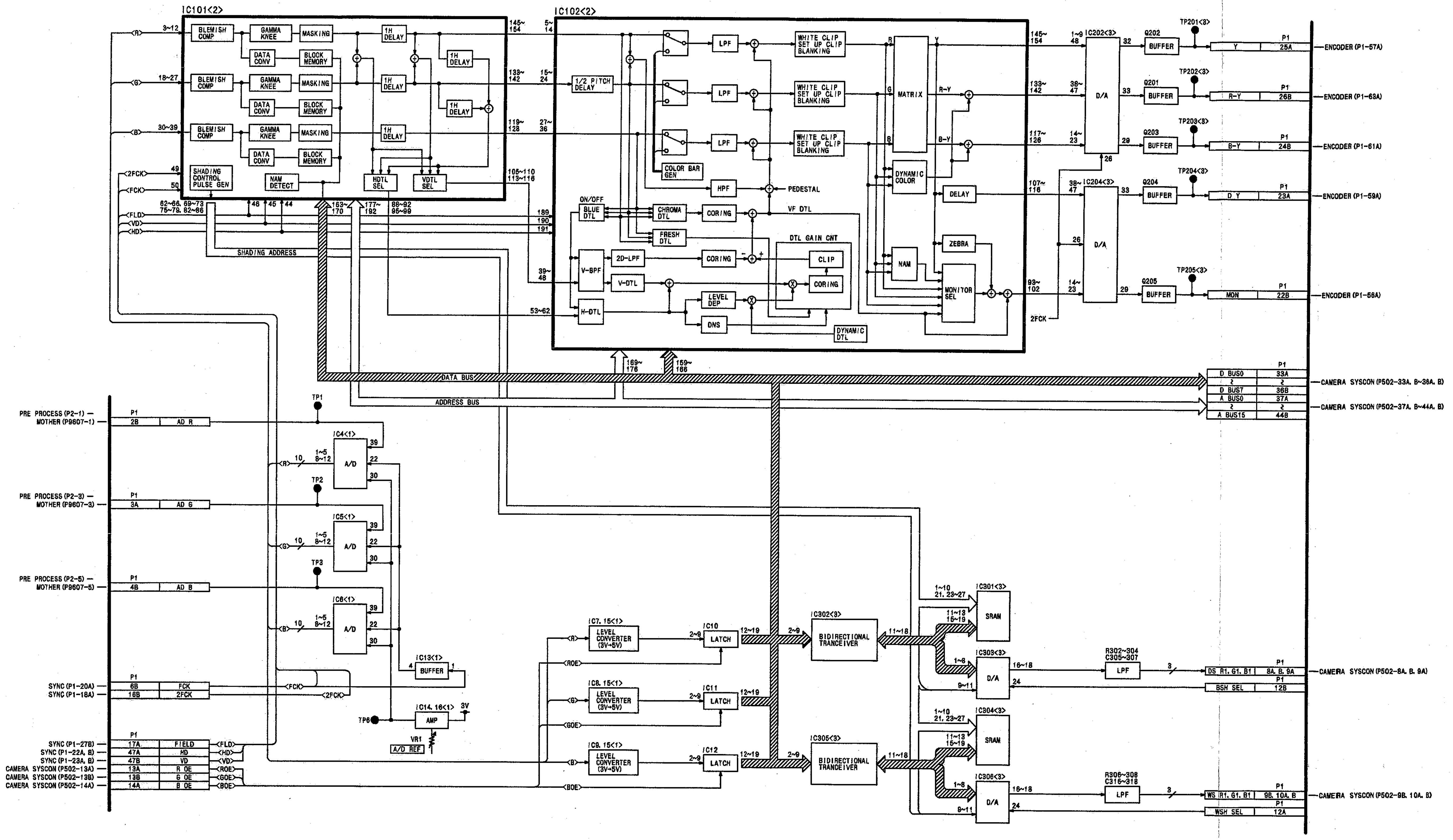
MATRIX converts **RGB** to **Y/R-Y/B-Y**.

Outputs from **145th~154th** pins are **Y, 133th~142nd** pins are **R-Y,** and **117th~126th** pins are **B-Y.** All of those are converted to analog signals at **IC202** and supplied to Encoder P.C.Board.

D Y output from **107th~116th** pins are delayed Y signal which is required to encode composite signal in Encoder P.C.Board.

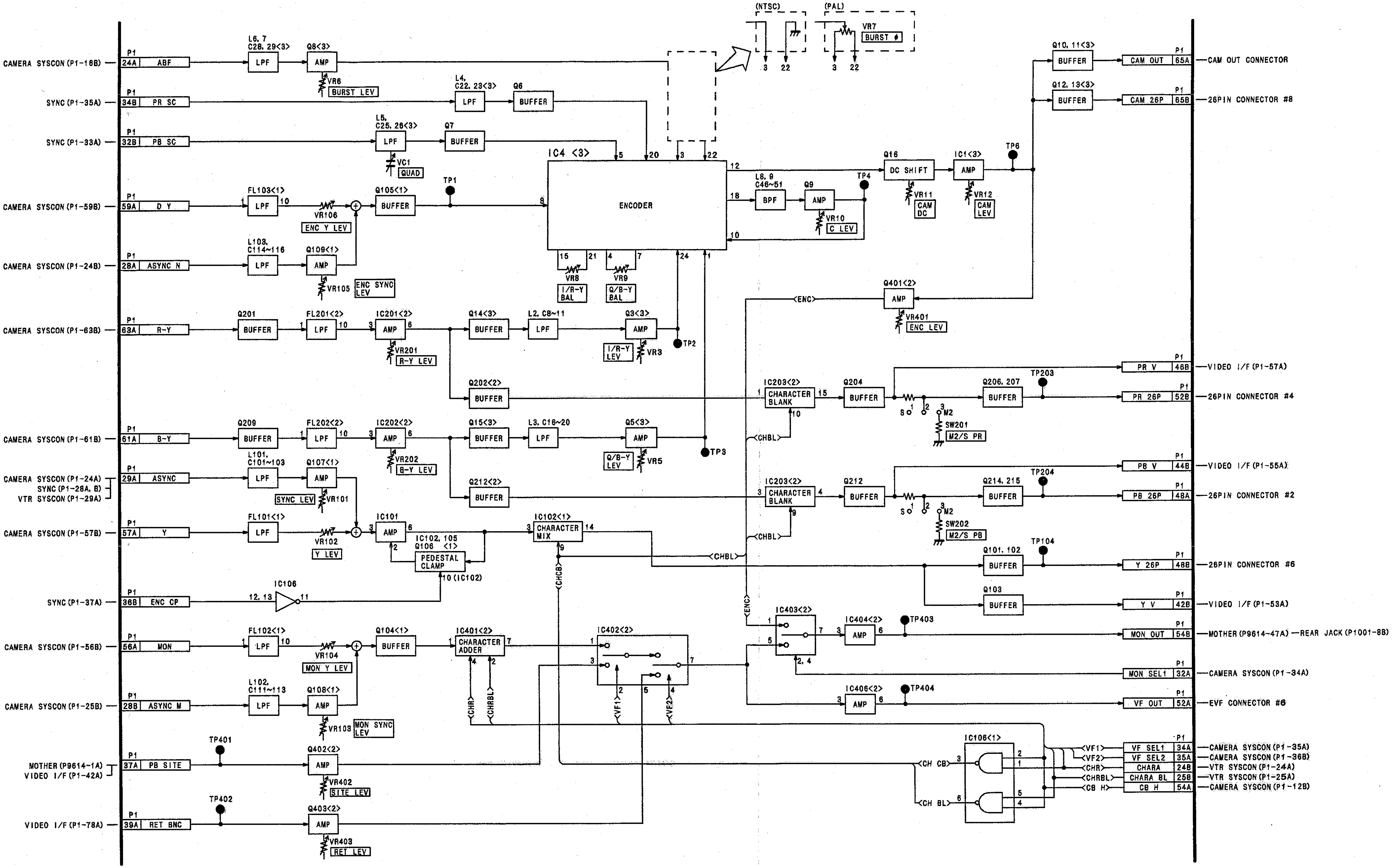
Outputs from **93th~102nd** pins are Y,R,G,B or NAM for EVF which have ZEBRA. This is converted to analog signal at **IC204** and supplied to Encoder P.C.Board.

DSP BLOCK DIAGRAM



IC101<2>
BLEMISH COMP
GAMMA KNEE
MASKING
DATA CONV
BLOCK MEMORY
1H DELAY
SHADING CONTROL PULSE GEN
NAM DETECT
HDTL SEL
VDTL SEL
SHADING ADDRESS
IC102<2>
1/2 PITCH DELAY
LPF
HPF
COLOR BAR GEN
WHITE CLIP SET UP CLIP BLANKING
MATRIX
DYNAMIC COLOR
DELAY
ZEBRA
NAM
MONITOR SEL
PEDESTAL
VF DTL
ON/OFF
BLUE DTL
CHROMA DTL
FRESH DTL
CORING
DTL GAIN CNT
CLIP
V-BPF
2D-LPF
V-DTL
H-DTL
LEVEL DEP
DNS
DYNAMIC DTL
R-Y
B-Y
2FCK
IC202<3>
IC204<3>
D/A
Q202
Q201
Q203
Q204
Q205
BUFFER
TP201<3>
TP202<3>
TP203<3>
TP204<3>
TP205<3>
P1
Y 25A —ENCODER (P1-57A)
R-Y 26B —ENCODER (P1-63A)
B-Y 24B —ENCODER (P1-61A)
D Y 23A —ENCODER (P1-59A)
MON 22B —ENCODER (P1-56A)
DATA BUS
ADDRESS BUS
D BUS0 33A
D BUS7 36B
A BUS0 37A
A BUS15 44B
—CAMERA SYSCON (P502-33A, B~36A, B)
—CAMERA SYSCON (P502-37A, B~44A, B)
PRE PROCESS (P2-1) — MOTHER (P9607-1) — 2B AD R
PRE PROCESS (P2-3) — MOTHER (P9607-3) — 3A AD G
PRE PROCESS (P2-5) — MOTHER (P9607-5) — 4B AD B
SYNC (P1-20A) — 6B FCK
SYNC (P1-18A) — 16B 2FCK
SYNC (P1-27B) — 17A FIELD
SYNC (P1-22A, B) — 47A HD
SYNC (P1-23A, B) — 47B VD
CAMERA SYSCON (P502-13A) — 13A R OE
CAMERA SYSCON (P502-13B) — 13B G OE
CAMERA SYSCON (P502-14A) — 14A B OE
TP1
TP2
TP3
TP6
IC4<1>
IC5<1>
IC6<1>
A/D
IC13<1>
BUFFER
IC14, 16<1>
AMP
3V
VR1
A/D REF
IC7, 15<1>
IC8, 15<1>
IC9, 15<1>
LEVEL CONVERTER (3V→5V)
IC10
IC11
IC12
LATCH
IC302<3>
IC305<3>
BIDIRECTIONAL TRANCEIVER
IC301<3>
IC304<3>
SRAM
IC303<3>
IC306<3>
D/A
R302~304 C305~307
R306~308 C316~318
LPF
DS R1, G1, B1 8A, B, 9A —CAMERA SYSCON (P502-8A, B, 9A)
BSH SEL 12B
WS R1, G1, B1 9B, 10A, B —CAMERA SYSCON (P502-9B, 10A, B)
WSH SEL 12A

ENCODER BLOCK DIAGRAM


CAMERA SYSCON (P1-16B)
SYNC (P1-35A)
SYNC (P1-33A)
CAMERA SYSCON (P1-59B)
CAMERA SYSCON (P1-24B)
CAMERA SYSCON (P1-63B)
CAMERA SYSCON (P1-61B)
CAMERA SYSCON (P1-24A)
SYNC (P1-28A, B)
VTR SYSCON (P1-29A)
CAMERA SYSCON (P1-57B)
SYNC (P1-37A)
CAMERA SYSCON (P1-56B)
CAMERA SYSCON (P1-25B)
MOTHER (P9614-1A)
VIDEO I/F (P1-42A)
VIDEO I/F (P1-78A)
P1
24A ABF
34B PR SC
32B PB SC
59A D Y
28A ASYNC N
63A R-Y
61A B-Y
29A ASYNC
57A Y
36B ENC CP
56A MON
28B ASYNC M
37A PB SITE
39A RET BNC
L6, 7
C28, 29<3>
LPF
Q8<3>
AMP
VR6
BURST LEV
L4,
C22, 23<3>
LPF
Q6
BUFFER
L5,
C25, 26<3>
LPF
Q7
BUFFER
VC1
QUAD
FL103<1>
LPF
VR106
ENC Y LEV
Q105<1>
BUFFER
TP1
L103,
C114~116
LPF
Q109<1>
AMP
VR105
ENC SYNC LEV
Q201
BUFFER
FL201<2>
LPF
IC201<2>
AMP
VR201
R-Y LEV
Q14<3>
BUFFER
L2, C8~11
LPF
Q3<3>
AMP
I/R-Y LEV
VR3
TP2
Q202<2>
BUFFER
Q209
BUFFER
FL202<2>
LPF
IC202<2>
AMP
VR202
B-Y LEV
Q15<3>
BUFFER
L3, C16~20
LPF
Q5<3>
AMP
Q/B-Y LEV
VR5
TP3
Q212<2>
BUFFER
L101,
C101~103
LPF
Q107<1>
AMP
SYNC LEV
VR101
FL101<1>
LPF
VR102
Y LEV
IC101
AMP
IC102, 105
Q106 <1>
PEDESTAL CLAMP
10 (IC102)
IC102<1>
CHARACTER MIX
IC106
12, 13
11
FL102<1>
LPF
VR104
MON Y LEV
Q104<1>
BUFFER
IC401<2>
CHARACTER ADDER
<CHR>
<CHRBL>
IC402<2>
<VF1>
<VF2>
<CHCB>
L102,
C111~113
LPF
Q108<1>
AMP
VR103
MON SYNC LEV
TP401
Q402<2>
AMP
VR402
SITE LEV
TP402
Q403<2>
AMP
VR403
RET LEV
(NTSC)
(PAL)
VR7
BURST ϕ
IC4 <3>
ENCODER
VR8
I/R-Y BAL
VR9
Q/B-Y BAL
L8, 9
C46~51
BPF
Q9
AMP
VR10
C LEV
TP4
Q16
DC SHIFT
VR11
CAM DC
IC1<3>
AMP
VR12
CAM LEV
TP6
Q10, 11<3>
BUFFER
Q12, 13<3>
BUFFER
65A CAM OUT
65B CAM 26P
Q401<2>
AMP
VR401
ENC LEV
<ENC>
IC203<2>
CHARACTER BLANK
<CHBL>
Q204
BUFFER
SO
M2
SW201
M2/S PR
Q206, 207
BUFFER
TP203
46B PR V
52B PR 26P
IC203<2>
CHARACTER BLANK
Q212
BUFFER
SW202
M2/S PB
Q214, 215
BUFFER
TP204
44B PB V
48A PB 26P
TP104
Q101, 102
BUFFER
48B Y 26P
Q103
BUFFER
42B Y V
IC403<2>
IC404<2>
AMP
TP403
54B MON OUT
32A MON SEL1
IC406<2>
AMP
TP404
52A VF OUT
IC106<1>
<CH CB>
<CH BL>
34A VF SEL1
35A VF SEL2
24B CHARA
25B CHARA BL
54A CB H
—CAM OUT CONNECTOR
—26PIN CONNECTOR #8
—VIDEO I/F (P1-57A)
—26PIN CONNECTOR #4
—VIDEO I/F (P1-55A)
—26PIN CONNECTOR #2
—26PIN CONNECTOR #6
—VIDEO I/F (P1-53A)
—MOTHER (P9614-47A) —REAR JACK (P1001-8B)
—CAMERA SYSCON (P1-34A)
—EVF CONNECTOR #6
—CAMERA SYSCON (P1-35A)
—CAMERA SYSCON (P1-36B)
—VTR SYSCON (P1-24A)
—VTR SYSCON (P1-25A)
—CAMERA SYSCON (P1-12B)

Encoder P.C.Board

Encoder converts inputs from DSP to composite and component signals.

IC4 is an encoder. **D** Y(Y for composite) is input to **8th** pin, **R-Y** to **24th** pin, and **B-Y** to **1st** pin.

VR106 adjusts the level of **D Y.** Sync. **ASYNC** N is added to **D Y. D Y** goes to **IC4. VR105** adjusts the level of sync.

R-Y is adjusted in level with **VR201** and supplied to **IC4.** On the other hand it is output as Pr signal **PR V**, **PR 26P. PR V** is to be recorded in AJ-D700. **PR 26P** is to be output via 26 pins connector(Option).

SW201 selects M2 level or β cam level for 26 pins connector.

B-Y is adjusted in level with **VR202** and supplied to **IC4.** On the other hand it is output as Pb signal **PB** V, **PB 26P. PB** V is to be recorded in AJ-D700. **PB 26P** is to be output via 26 pins connector(Option).

SW202 selects M2 level or β cam level for 26 pins connector.

Sub-carriers are supplied to **IC4** as **PR SC** and **PB SC. ABF** is Burst signal and is adjusted in level with **VR6.**

R-Y and B-Y are modulated to C signal at **IC4. VR10** adjusts the C level. C signal returns to **IC4** and encoded with Y. Mixed signal is output from **12th** pin. After DC(**VR11**) and level(**VR12**) are adjusted, composite signal has three ways; **CAM OUT, CAM 26P** for 26 pins connector, **MON OUT** for VIDEO OUT connector. **VR401** adjusts the level of **MON OUT.**

VR102 adjusts the level of ordinary **Y.** Then sync., **ASYNC,** is added to **Y. VR101** adjusts the level of sync. After pedestal is added at **IC101, Y** is output as **Y V** and **Y 26P. Y V** is to be recorded in AJ-D700. **Y 26P** is to be output via 26 pins connector(Option).

MON is Y,R,G,B or NAM for EVF and is adjusted in level with **VR104.** Sync.,**ASYNC M,** is added to that signal. Sync level is adjusted with **VR103. IC401** adds superimpose. **IC402** selects **PB SITE** for playback or **RET BNC** for Return. After that the signal is supplied to EVF as **VF OUT.** On the other hand **IC403** selects VF signal or composite signal for VIDEO OUT connector at **IC403.** The selected signal is supplied to Rear Jack P.C.Board as **MON OUT.**

VR402 adjusts the level of PB signal.

VR403 adjusts the level of RETURN input.

Sync. P.C.Board

This circuit is composed of **IC27** and **IC11**.

GL IN is input from GEN LOCK IN connector. Composite sync. separated at **IC34** is supplied to **98th** pin of **IC27** and **85th** pin of **IC11**. Burst signal is separated at **IC2** and **IC3** and supplied to **69th** pin of **IC27**. H SYNC. is separated from the sync. input from **98th** pin of **IC27**. Then H SYNC. is output from **101st** pin. This is adjusted in phase at **IC22** and input again from **43th** pin.

X4 located at left side of diagram generates reference 4FSC. H sync. is generated based on that 4FSC. This H sync. or **HR**, external input sync. input from **45th** pin is selected at **IC27**. Selected signal is output from **46th** pin as **HO**. **X1** located at top of diagram generates **2FCK** locked to **HO** and then supplied to **IC11**.

IC11 generates clocks which is used in camera unit and locked to that **2FCK**.

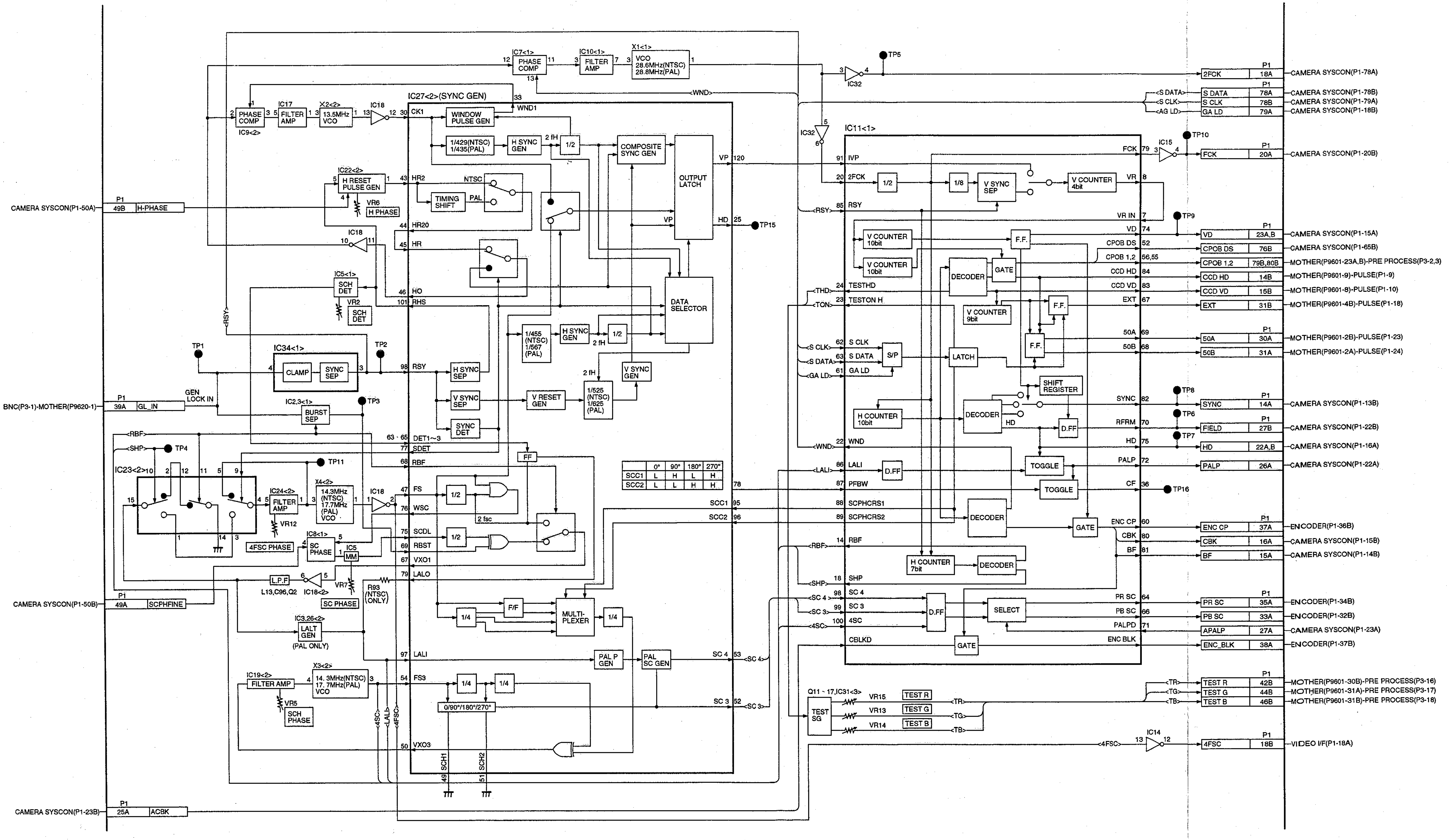
PLL located at top left of diagram which is composed of **IC9** of phase comparator and **X2** of 13.5MHz oscillator drives **IC27**.

PLL located at bottom left of diagram which is composed of **IC19** of phase comparator and **X3** of oscillator adjusts SCH.

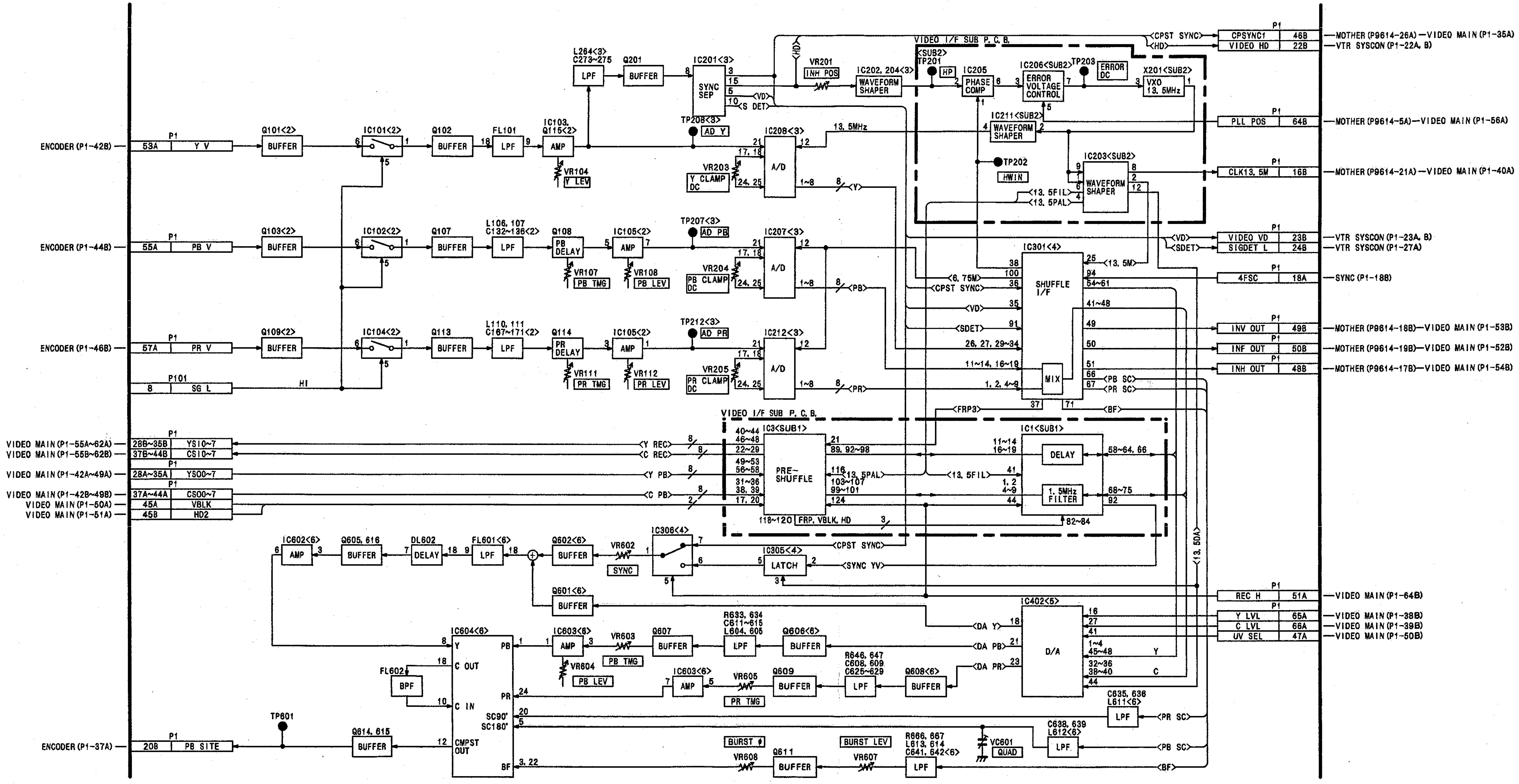
The signals at **95th** and **96th** pins of **IC27** are used for sub-carrier adjustment.

Q11～Q17 and **IC31** generate Ramp signal for testing which is adjusted in level with **VR13～VR15**.

CAMERA SYNC BLOCK DIAGRAM


IC7<1>
PHASE COMP
IC10<1>
FILTER AMP
X1<1>
VCO 28.6MHz(NTSC) 28.8MHz(PAL)
<WND>
TP5
IC32
IC27<2>(SYNC GEN)
PHASE COMP
IC9<2>
IC17
FILTER AMP
X2<2>
13.5MHz VCO
IC18
CK1
WINDOW PULSE GEN
WND1
1/429(NTSC) 1/435(PAL)
H SYNC GEN
2 fH
1/2
COMPOSITE SYNC GEN
OUTPUT LATCH
VP
HD
TP15
IC22<2>
H RESET PULSE GEN
HR2
NTSC
PAL
TIMING SHIFT
VR6
H PHASE
HR20
HR
IC18
IC5<1>
SCH DET
VR2
SCH DET
HO
RHS
DATA SELECTOR
1/455 (NTSC) 1/567 (PAL)
H SYNC GEN
<RSY>
TP1
IC34<1>
CLAMP
SYNC SEP
TP2
RSY
H SYNC SEP
V SYNC SEP
SYNC DET
V RESET GEN
1/525 (NTSC) 1/625 (PAL)
V SYNC GEN
CAMERA SYSCON(P1-50A)
P1
49B
H-PHASE
BNC(P3-1)-MOTHER(P9620-1)
39A
GL_IN
GEN LOCK IN
IC2,3<1>
BURST SEP
TP3
<RBF>
<SHP>
TP4
IC23<2>
TP11
IC24<2>
FILTER AMP
VR12
X4<2>
14.3MHz (NTSC) 17.7MHz (PAL) VCO
4FSC PHASE
IC8<1>
SC PHASE
IC5
MM
L.P.F
L13,C96,Q2
IC18<2>
VR7
R93 (NTSC) (ONLY)
SC PHASE
CAMERA SYSCON(P1-50B)
49A
SCPHFINE
IC3,26<2>
LALT GEN
(PAL ONLY)
IC19<2>
FILTER AMP
X3<2>
14. 3MHz(NTSC) 17. 7MHz(PAL) VCO
VR5
SCH PHASE
CAMERA SYSCON(P1-23B)
25A
ACBK
DET1~3
SDET
RBF
FF
FS
WSC
SCDL
RBST
VXO1
LALO
LALI
FS3
VXO3
1/2
2 fsc
1/4
F/F
MULTI-PLEXER
PAL P GEN
PAL SC GEN
0/90°/180°/270°
SCH1
SCH2
SC 4
SC 3
<SC 4>
<SC 3>
<4SC>
<LALI>
<4FSC>
SCC1
SCC2
0° | 90° | 180° | 270°
SCC1 | L | H | L | H
SCC2 | L | L | H | H
IC32
IC11<1>
FCK
IC15
TP10
IVP
2FCK
1/2
1/8
V SYNC SEP
V COUNTER 4bit
VR
RSY
VR IN
TP9
VD
CPOB DS
CPOB 1,2
CCD HD
CCD VD
EXT
V COUNTER 10bit
V COUNTER 10bit
F.F.
DECODER
GATE
TESTHD
TESTON H
V COUNTER 9bit
F.F.
F.F.
<THD>
<TON>
S CLK
S DATA
GA LD
S/P
LATCH
50A
50B
SHIFT REGISTER
H COUNTER 10bit
DECODER
HD
D.FF
SYNC
TP8
RFRM
TP6
HD
TP7
WND
<WND>
LALI
D.FF
TOGGLE
PALP
PFBW
TOGGLE
CF
TP16
SCPHCRS1
SCPHCRS2
DECODER
GATE
ENC CP
CBK
BF
RBF
H COUNTER 7bit
DECODER
SHP
SC 4
SC 3
4SC
D.FF
SELECT
PR SC
PB SC
PALPD
ENC BLK
CBLKD
GATE
Q11 ~ 17,IC31<3>
TEST SG
VR15
VR13
VR14
TEST R
TEST G
TEST B
<TR>
<TG>
<TB>
IC14
<4FSC>
<S DATA>
<S CLK>
<AG LD>
2FCK | 18A | CAMERA SYSCON(P1-78A)
S DATA | 78A | CAMERA SYSCON(P1-78B)
S CLK | 78B | CAMERA SYSCON(P1-79A)
GA LD | 79A | CAMERA SYSCON(P1-18B)
FCK | 20A | CAMERA SYSCON(P1-20B)
VD | 23A,B | CAMERA SYSCON(P1-15A)
CPOB DS | 76B | CAMERA SYSCON(P1-65B)
CPOB 1,2 | 79B,80B | MOTHER(P9601-23A,B)-PRE PROCESS(P3-2,3)
CCD HD | 14B | MOTHER(P9601-9)-PULSE(P1-9)
CCD VD | 15B | MOTHER(P9601-8)-PULSE(P1-10)
EXT | 31B | MOTHER(P9601-4B)-PULSE(P1-18)
50A | 30A | MOTHER(P9601-2B)-PULSE(P1-23)
50B | 31A | MOTHER(P9601-2A)-PULSE(P1-24)
SYNC | 14A | CAMERA SYSCON(P1-13B)
FIELD | 27B | CAMERA SYSCON(P1-22B)
HD | 22A,B | CAMERA SYSCON(P1-16A)
PALP | 26A | CAMERA SYSCON(P1-22A)
ENC CP | 37A | ENCODER(P1-36B)
CBK | 16A | CAMERA SYSCON(P1-15B)
BF | 15A | CAMERA SYSCON(P1-14B)
PR SC | 35A | ENCODER(P1-34B)
PB SC | 33A | ENCODER(P1-32B)
APALP | 27A | CAMERA SYSCON(P1-23A)
ENC_BLK | 38A | ENCODER(P1-37B)
TEST R | 42B | MOTHER(P9601-30B)-PRE PROCESS(P3-16)
TEST G | 44B | MOTHER(P9601-31A)-PRE PROCESS(P3-17)
TEST B | 46B | MOTHER(P9601-31B)-PRE PROCESS(P3-18)
4FSC | 18B | VIDEO I/F(P1-18A)

VIDEO I/F BLOCK DIAGRAM


ENCODER (P1-42B)
ENCODER (P1-44B)
ENCODER (P1-46B)
ENCODER (P1-37A)
VIDEO MAIN (P1-55A~62A)
VIDEO MAIN (P1-55B~62B)
VIDEO MAIN (P1-42A~49A)
VIDEO MAIN (P1-42B~49B)
VIDEO MAIN (P1-50A)
VIDEO MAIN (P1-51A)
P1
53A Y V
55A PB V
57A PR V
P101
8 SG L
28B~35B YSI0~7
37B~44B CSI0~7
28A~35A YSO0~7
37A~44A CSO0~7
45A VBLK
45B HD2
20B PB SITE
Q101<2> BUFFER
Q103<2> BUFFER
Q109<2> BUFFER
IC101<2>
IC102<2>
IC104<2>
HI
Q102 BUFFER
Q107 BUFFER
Q113 BUFFER
FL101 LPF
L106, 107 C132~136<2> LPF
L110, 111 C167~171<2> LPF
IC103, Q115<2> AMP
VR104 Y LEV
Q108 PB DELAY
Q114 PR DELAY
VR107 PB TMG
VR111 PR TMG
IC105<2> AMP
VR108 PB LEV
VR112 PR LEV
L264<3> C273~275 LPF
Q201 BUFFER
IC201<3> SYNC SEP
<VD>
<S DET>
<HD>
TP208<3> AD Y
TP207<3> AD PB
TP212<3> AD PR
VR203 Y CLAMP DC
VR204 PB CLAMP DC
VR205 PR CLAMP DC
IC208<3> A/D
IC207<3> A/D
IC212<3> A/D
13. 5MHz
<Y>
<PB>
<PR>
VIDEO I/F SUB P. C. B.
<SUB2>
TP201 HP
VR201 INH POS
IC202, 204<3> WAVEFORM SHAPER
IC205 PHASE COMP
IC206<SUB2> ERROR VOLTAGE CONTROL
TP203 ERROR DC
X201<SUB2> VXO 13. 5MHz
IC211<SUB2> WAVEFORM SHAPER
TP202 HWIN
IC203<SUB2> WAVEFORM SHAPER
<13. 5FIL>
<13. 5PAL>
<CPST SYNC>
<HD>
P1 CPSYNC1 46B
VIDEO HD 22B
PLL POS 64B
CLK13. 5M 16B
VIDEO VD 23B
SIGDET L 24B
4FSC 18A
INV OUT 49B
INF OUT 50B
INH OUT 48B
REC H 51A
Y LVL 65A
C LVL 66A
UV SEL 47A
MOTHER (P9614-26A) — VIDEO MAIN (P1-35A)
VTR SYSCON (P1-22A, B)
MOTHER (P9614-5A) — VIDEO MAIN (P1-56A)
MOTHER (P9614-21A) — VIDEO MAIN (P1-40A)
VTR SYSCON (P1-23A, B)
VTR SYSCON (P1-27A)
SYNC (P1-18B)
MOTHER (P9614-18B) — VIDEO MAIN (P1-53B)
MOTHER (P9614-19B) — VIDEO MAIN (P1-52B)
MOTHER (P9614-17B) — VIDEO MAIN (P1-54B)
VIDEO MAIN (P1-64B)
VIDEO MAIN (P1-38B)
VIDEO MAIN (P1-39B)
VIDEO MAIN (P1-50B)
IC301<4> SHUFFLE I/F
MIX
<VD>
<SDET>
<6. 75M>
<CPST SYNC>
<13. 5M>
26, 27, 29~34
11~14, 16~19
1, 2, 4~9
54~61
41~48
<PB SC>
<PR SC>
<FRP3>
<BF>
IC3<SUB1> PRE-SHUFFLE
<Y REC>
<C REC>
<Y PB>
<C PB>
40~44 46~48
22~29
49~53 56~58
31~36 38, 39
17, 20
118~120 FRP, VBLK, HD
89, 92~98
103~107 99~101
IC1<SUB1> DELAY
1. 5MHz FILTER
<13. 5FIL>
58~64, 66
68~75 92
82~84
<13. 5DA>
IC306<4>
IC305<4> LATCH
<CPST SYNC>
<SYNC YV>
IC602<6> AMP
Q605, 616 BUFFER
DL602 DELAY
FL601<6> LPF
Q602<6> BUFFER
VR602 SYNC
Q601<6> BUFFER
IC402<5> D/A
<DA Y>
<DA PB>
<DA PR>
IC604<6>
Y
C OUT
C IN
CMPST OUT
PB
PR
SC90°
SC180°
BF
FL602 BPF
IC603<6> AMP
VR603 PB TMG
VR604 PB LEV
Q607 BUFFER
R633, 634 C611~615 L604, 605 LPF
Q606<6> BUFFER
VR605 PR TMG
Q609 BUFFER
R646, 647 C608, 609 C625~629 LPF
Q608<6> BUFFER
C635, 636 L611<6> LPF
C638, 639 L612<6> LPF
TP601
Q614, 615 BUFFER
BURST φ
VR606
Q611 BUFFER
BURST LEV
VR607
R666, 667 L613, 614 C641, 642<6> LPF
VC601 QUAD

Video I/F P.C.Board

VIDEO I/F is the interface between camera unit and VTR unit.

Y V is input from Encoder. **IC101** selects **Y V** or special signal for factory. **IC101** is switched by **SG L** which is always high. After **VR104** adjusts the level, Y is converted to digital signal at **IC208**. DC level of clamp depends on **VR203**.

Sync. is separated from Y at **IC201**. PLL is composed of **IC205** of phase comparator, **X201** of 13.5MHz oscillator and **IC301**. This PLL generates the reference clock locked to input signal.

PB V is input from Encoder. **IC102** selects **PB V** or special signal for factory. After **VR107** adjusts the timing and **VR108** adjusts the level, Pb is converted to digital signal at **IC207**. DC level of clamp depends on **VR204**.

PR V is input from Encoder. **IC104** selects **PR V** or special signal for factory. After **VR111** adjusts the timing and **VR112** adjusts the level, Pr is converted to digital signal at **IC212**. DC level of clamp depends on **VR205**.

Y, Pb and **Pr** converted to 8bits of digital signal are supplied to **IC301**. Pb and Pr are mixed and supplied to **IC1** which is a filter on Video I/F sub P.C.Board as **YSI** and **CSI**. Each of those is 8bits of digital signal. **IC3,** Pre-shuffle on Video I/F sub P.C.Board, assigns data allocation because chroma data is thinned in Shuffle IC of Video Main circuit.

IC402 is a D/A converter where playback signal is mainly processed. Pb level is adjusted with **VR604**. **Y** level and **C** level are adjusted with EVR in the D/A converter. **IC604** is an encoder. **Pb timing** are adjusted with **VR603** and **Pr timing** are adjusted with **VR605**.

INH OUT is the pulse locked to input signal, which has the frequency of H. **INV OUT** is the pulse locked to input signal, which has the frequency of V. **INF OUT** is the pulse locked to input signal, which has the frequency of frame.

S DET output from **IC201** detection signal which is LOW when sync. is detected in external input.

VTR Syscon P.C.Board

This circuit is composed of CPU, Parallel I/O, Time Code and Character Generator.

Inputs from the operation panel are **ZEBRA, PLAY, STOP, FF, REW, EJECT, START, RET, SHUT, AWB** and **ABB SWs**. Those signals are supplied to **IC1** of CPU, via **IC201** of Parallel I/O.

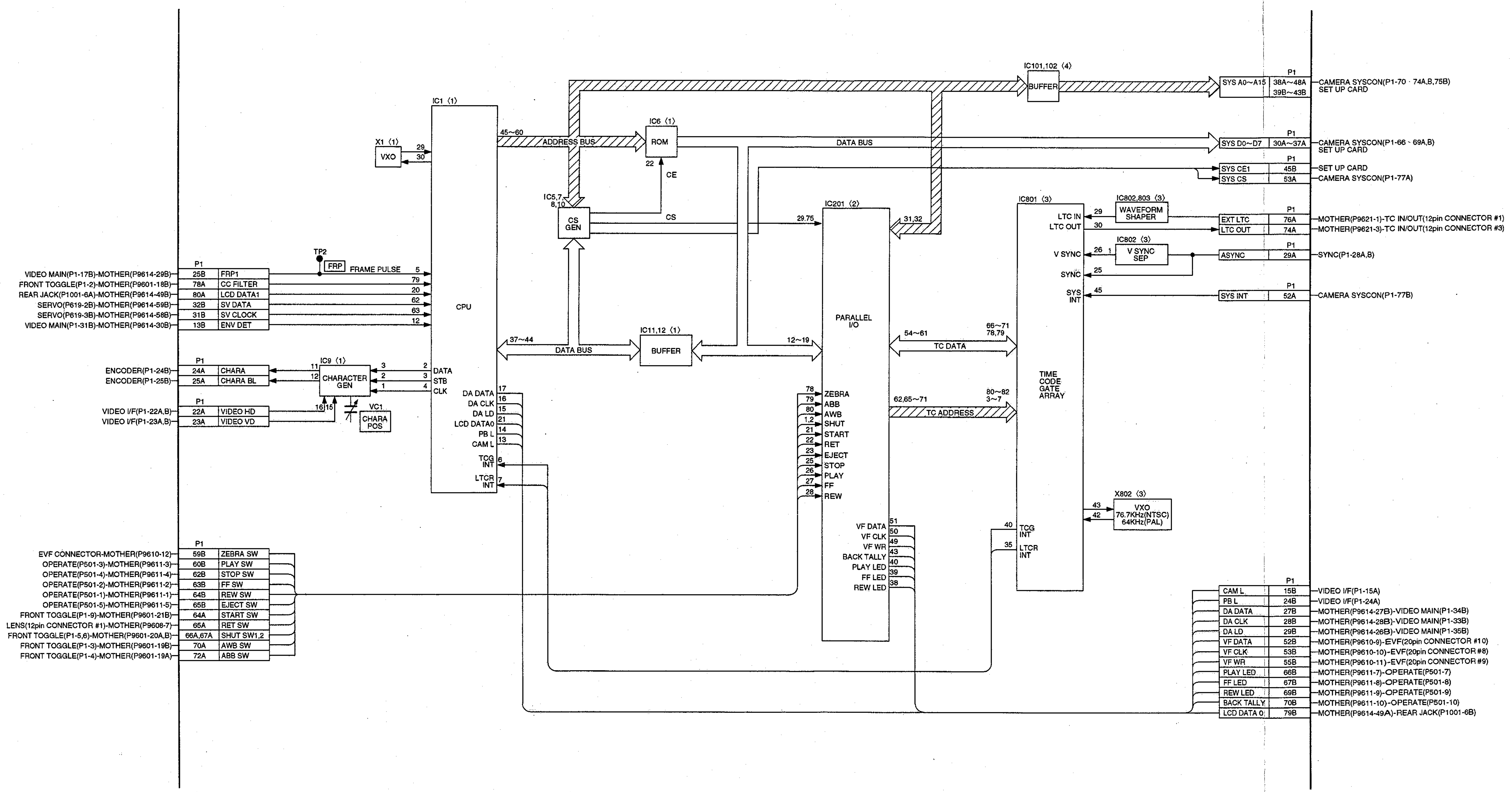
VTR Syscon and Camera Syscon communicate by **SYS A0～A15** and **SYS D0～D7**. **SYS A0～A15** are address lines. **SYS D0～D7** are data lines.

IC9 generates character. The character is supplied to Encoder P.C.Board.

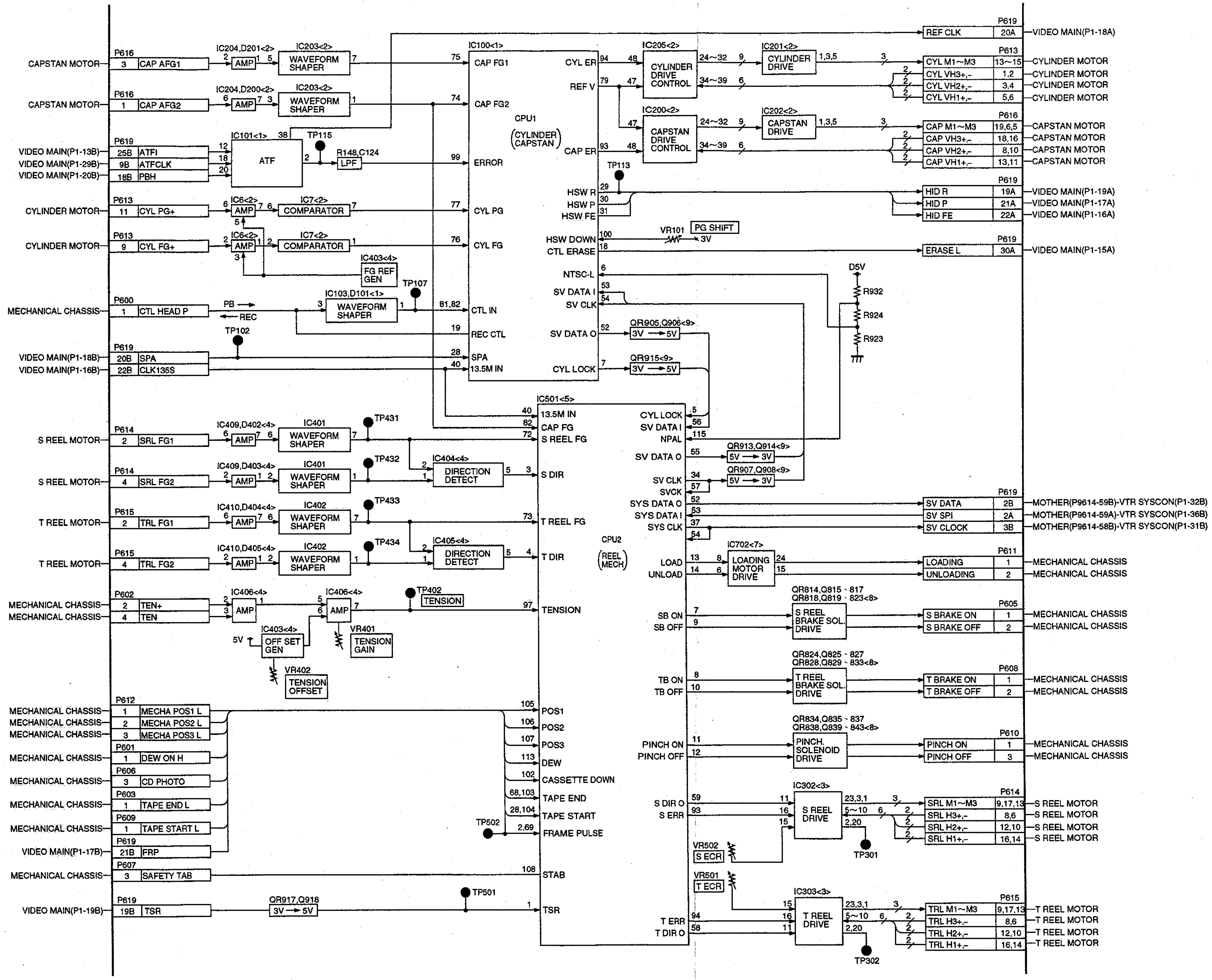
IC801 is time code gate array which includes time code reader and generator. **29th** pin and **30th** pin are IN/OUT for external TC, which are supplied to 12 pins Multi Connector.

IC6 is Syscon ROM.

VTR SYSCON BLOCK DIAGRAM


IC1 (1)
CPU
X1 (1)
VXO
IC6 (1)
ROM
CE
ADDRESS BUS
DATA BUS
IC5,7,8,10
CS GEN
CS
IC11,12 (1)
BUFFER
IC101,102 (4)
BUFFER
IC201 (2)
PARALLEL I/O
IC801 (3)
TIME CODE GATE ARRAY
IC802,803 (3)
WAVEFORM SHAPER
IC802 (3)
V SYNC SEP
X802 (3)
VXO 76.7KHz(NTSC) 64KHz(PAL)
IC9 (1)
CHARACTER GEN
VC1
CHARA POS
TP2
FRP
FRAME PULSE
TC DATA
TC ADDRESS
LTC IN
LTC OUT
V SYNC
SYNC
SYS INT
TCG INT
LTCR INT
DATA
STB
CLK
DA DATA
DA CLK
DA LD
LCD DATA0
PB L
CAM L
ZEBRA
ABB
AWB
SHUT
START
RET
EJECT
STOP
PLAY
FF
REW
VF DATA
VF CLK
VF WR
BACK TALLY
PLAY LED
FF LED
REW LED
P1
VIDEO MAIN(P1-17B)-MOTHER(P9614-29B) 25B FRP1
FRONT TOGGLE(P1-2)-MOTHER(P9601-18B) 78A CC FILTER
REAR JACK(P1001-6A)-MOTHER(P9614-49B) 80A LCD DATA1
SERVO(P619-2B)-MOTHER(P9614-59B) 32B SV DATA
SERVO(P619-3B)-MOTHER(P9614-58B) 31B SV CLOCK
VIDEO MAIN(P1-31B)-MOTHER(P9614-30B) 13B ENV DET
ENCODER(P1-24B) 24A CHARA
ENCODER(P1-25B) 25A CHARA BL
VIDEO I/F(P1-22A,B) 22A VIDEO HD
VIDEO I/F(P1-23A,B) 23A VIDEO VD
EVF CONNECTOR-MOTHER(P9610-12) 59B ZEBRA SW
OPERATE(P501-3)-MOTHER(P9611-3) 60B PLAY SW
OPERATE(P501-4)-MOTHER(P9611-4) 62B STOP SW
OPERATE(P501-2)-MOTHER(P9611-2) 63B FF SW
OPERATE(P501-1)-MOTHER(P9611-1) 64B REW SW
OPERATE(P501-5)-MOTHER(P9611-5) 65B EJECT SW
FRONT TOGGLE(P1-9)-MOTHER(P9601-21B) 64A START SW
LENS(12pin CONNECTOR #1)-MOTHER(P9608-7) 65A RET SW
FRONT TOGGLE(P1-5,6)-MOTHER(P9601-20A,B) 66A,67A SHUT SW1,2
FRONT TOGGLE(P1-3)-MOTHER(P9601-19B) 70A AWB SW
FRONT TOGGLE(P1-4)-MOTHER(P9601-19A) 72A ABB SW
SYS A0~A15 38A~48A 39B~43B CAMERA SYSCON(P1-70・74A,B,75B) SET UP CARD
SYS D0~D7 30A~37A CAMERA SYSCON(P1-66・69A,B) SET UP CARD
SYS CE1 45B SET UP CARD
SYS CS 53A CAMERA SYSCON(P1-77A)
EXT LTC 76A MOTHER(P9621-1)-TC IN/OUT(12pin CONNECTOR #1)
LTC OUT 74A MOTHER(P9621-3)-TC IN/OUT(12pin CONNECTOR #3)
ASYNC 29A SYNC(P1-28A,B)
SYS INT 52A CAMERA SYSCON(P1-77B)
CAM L 15B VIDEO I/F(P1-15A)
PB L 24B VIDEO I/F(P1-24A)
DA DATA 27B MOTHER(P9614-27B)-VIDEO MAIN(P1-34B)
DA CLK 28B MOTHER(P9614-28B)-VIDEO MAIN(P1-33B)
DA LD 29B MOTHER(P9614-26B)-VIDEO MAIN(P1-35B)
VF DATA 52B MOTHER(P9610-9)-EVF(20pin CONNECTOR #10)
VF CLK 53B MOTHER(P9610-10)-EVF(20pin CONNECTOR #8)
VF WR 55B MOTHER(P9610-11)-EVF(20pin CONNECTOR #9)
PLAY LED 66B MOTHER(P9611-7)-OPERATE(P501-7)
FF LED 67B MOTHER(P9611-8)-OPERATE(P501-8)
REW LED 69B MOTHER(P9611-9)-OPERATE(P501-9)
BACK TALLY 70B MOTHER(P9611-10)-OPERATE(P501-10)
LCD DATA 0 79B MOTHER(P9614-49A)-REAR JACK(P1001-6B)

SERVO BLOCK DIAGRAM



CAPSTAN MOTOR
P616 3 CAP AFG1
CAPSTAN MOTOR
P616 1 CAP AFG2
VIDEO MAIN(P1-13B)
VIDEO MAIN(P1-29B)
VIDEO MAIN(P1-20B)
P619 25B ATFI
9B ATFCLK
18B PBH
CYLINDER MOTOR
P613 11 CYL PG+
CYLINDER MOTOR
P613 9 CYL FG+
MECHANICAL CHASSIS
P600 1 CTL HEAD P
VIDEO MAIN(P1-18B)
VIDEO MAIN(P1-16B)
P619 20B SPA
22B CLK135S
S REEL MOTOR
P614 2 SRL FG1
S REEL MOTOR
P614 4 SRL FG2
T REEL MOTOR
P615 2 TRL FG1
T REEL MOTOR
P615 4 TRL FG2
MECHANICAL CHASSIS
MECHANICAL CHASSIS
P602 2 TEN+
4 TEN
MECHANICAL CHASSIS
MECHANICAL CHASSIS
MECHANICAL CHASSIS
P612 1 MECHA POS1 L
2 MECHA POS2 L
3 MECHA POS3 L
MECHANICAL CHASSIS
P601 1 DEW ON H
MECHANICAL CHASSIS
P606 3 CD PHOTO
MECHANICAL CHASSIS
P603 1 TAPE END L
MECHANICAL CHASSIS
P609 1 TAPE START L
VIDEO MAIN(P1-17B)
P619 21B FRP
MECHANICAL CHASSIS
P607 3 SAFETY TAB
VIDEO MAIN(P1-19B)
P619 19B TSR
IC204,D201<2> AMP
IC203<2> WAVEFORM SHAPER
IC204,D200<2> AMP
IC203<2> WAVEFORM SHAPER
IC101<1> ATF
TP115
R148,C124 LPF
IC6<2> AMP
IC7<2> COMPARATOR
IC6<2> AMP
IC7<2> COMPARATOR
IC403<4> FG REF GEN
TP107
IC103,D101<1> WAVEFORM SHAPER
PB
REC
TP102
IC409,D402<4> AMP
IC401 WAVEFORM SHAPER
TP431
IC409,D403<4> AMP
IC401 WAVEFORM SHAPER
TP432
IC404<4> DIRECTION DETECT
IC410,D404<4> AMP
IC402 WAVEFORM SHAPER
TP433
IC410,D405<4> AMP
IC402 WAVEFORM SHAPER
TP434
IC405<4> DIRECTION DETECT
IC406<4> AMP
IC406<4> AMP
TP402 TENSION
5V
IC403<4> OFF SET GEN
VR401 TENSION GAIN
VR402 TENSION OFFSET
TP502
TP501
QR917,Q918 3V → 5V
IC100<1>
CAP FG1
CAP FG2
CPU1 (CYLINDER CAPSTAN)
ERROR
CYL PG
CYL FG
CTL IN
REC CTL
SPA
13.5M IN
CYL ER
REF V
CAP ER
TP113
HSW R
HSW P
HSW FE
HSW DOWN
CTL ERASE
NTSC-L
SV DATA I
SV CLK
SV DATA O
CYL LOCK
VR101 PG SHIFT 3V
QR905,Q906<9> 3V → 5V
QR915<9> 3V → 5V
D5V
R932
R924
R923
IC501<5>
13.5M IN
CAP FG
S REEL FG
S DIR
T REEL FG
T DIR
CPU2 (REEL MECH)
TENSION
POS1
POS2
POS3
DEW
CASSETTE DOWN
TAPE END
TAPE START
FRAME PULSE
STAB
TSR
CYL LOCK
SV DATA I
NPAL
SV DATA O
SV CLK
SVCK
SYS DATA O
SYS DATA I
SYS CLK
LOAD
UNLOAD
SB ON
SB OFF
TB ON
TB OFF
PINCH ON
PINCH OFF
S DIR O
S ERR
T ERR
T DIR O
QR913,Q914<9> 5V → 3V
QR907,Q908<9> 5V → 3V
IC205<2> CYLINDER DRIVE CONTROL
IC201<2> CYLINDER DRIVE
IC200<2> CAPSTAN DRIVE CONTROL
IC202<2> CAPSTAN DRIVE
IC702<7> LOADING MOTOR DRIVE
QR814,Q815 ~ 817 QR818,Q819 ~ 823<8> S REEL BRAKE SOL. DRIVE
QR824,Q825 ~ 827 QR828,Q829 ~ 833<8> T REEL BRAKE SOL. DRIVE
QR834,Q835 ~ 837 QR838,Q839 ~ 843<8> PINCH. SOLENOID DRIVE
IC302<3> S REEL DRIVE
TP301
VR502 S ECR
VR501 T ECR
IC303<3> T REEL DRIVE
TP302
P619 REF CLK 20A
P613 CYL M1~M3 13~15
CYL VH3+,- 1,2
CYL VH2+,- 3,4
CYL VH1+,- 5,6
P616 CAP M1~M3 19,6,5
CAP VH3+,- 18,16
CAP VH2+,- 8,10
CAP VH1+,- 13,11
P619 HID R 19A
HID P 21A
HID FE 22A
P619 ERASE L 30A
P619 SV DATA 2B
SV SPI 2A
SV CLOCK 3B
P611 LOADING 1
UNLOADING 2
P605 S BRAKE ON 1
S BRAKE OFF 2
P608 T BRAKE ON 1
T BRAKE OFF 2
P610 PINCH ON 1
PINCH OFF 3
P614 SRL M1~M3 9,17,13
SRL H3+,- 8,6
SRL H2+,- 12,10
SRL H1+,- 16,14
P615 TRL M1~M3 9,17,13
TRL H3+,- 8,6
TRL H2+,- 12,10
TRL H1+,- 16,14
VIDEO MAIN(P1-18A)
CYLINDER MOTOR
CYLINDER MOTOR
CYLINDER MOTOR
CYLINDER MOTOR
CAPSTAN MOTOR
CAPSTAN MOTOR
CAPSTAN MOTOR
CAPSTAN MOTOR
VIDEO MAIN(P1-19A)
VIDEO MAIN(P1-17A)
VIDEO MAIN(P1-16A)
VIDEO MAIN(P1-15A)
MOTHER(P9614-59B)-VTR SYSCON(P1-32B)
MOTHER(P9614-59A)-VTR SYSCON(P1-36B)
MOTHER(P9614-58B)-VTR SYSCON(P1-31B)
MECHANICAL CHASSIS
MECHANICAL CHASSIS
MECHANICAL CHASSIS
MECHANICAL CHASSIS
MECHANICAL CHASSIS
MECHANICAL CHASSIS
MECHANICAL CHASSIS
MECHANICAL CHASSIS
S REEL MOTOR
S REEL MOTOR
S REEL MOTOR
S REEL MOTOR
T REEL MOTOR
T REEL MOTOR
T REEL MOTOR
T REEL MOTOR

Servo P.C.Board

This circuit has two CPUs. **CPU1** controls cylinder and capstan. **CPU2** controls reel and mechanism.

CAP AFG1 and **CAP AFG2** are capstan FGs. Those are supplied to **IC100** of **CPU1**. **CAP M1～M3** drive the capstan. **CAP VH1～VH3** are fed back to **CPU1**.

CYL FG+ is cylinder FG. **CYL PG+** is cylinder PG. Those are supplied to **IC100** of **CPU1**. **CYL M1～M3** drive the cylinder. **CYL VH1～VH3** are fed back to **CPU1**.

HID R is R/P HSW. **HID P** is PB HSW. Played back CTL is input as **CTL HEAD P.** Recording CTL is also output as **CTL HEAD P. VR101** adjusts PG shifter which shifts HSW timing.

SRL FG1 and **SRL FG2** are S-reel FGs. Those are supplied to **IC501** of **CPU2**. **SRL M1～M3** drive the S-reel. **SRL H1～H3** are fed back to **CPU2**.

TRL FG1 and **TRL FG2** are T-reel FGs. Those are supplied to **IC501** of **CPU2**. **TRL M1～M3** drive the T-reel. **TRL H1～H3** are fed back to **CPU2**.

IC504 generates reference voltages which are comparated with error voltages, **S ERR** and **T ERR**. Reference voltages depend on **VR501** and **VR502**.

TEN+ and **TEN-** are input from tension sensor. **VR401** adjusts tension gain. **VR402** adjusts tension offset.

Abbreviations

ER, ERR	ERROR
DIR	DIRECTION
SV	SERVO
SB	S-REEL BRAKE
TB	T-REEL BRAKE
POS	POSITION

RF P.C.Board

(For recording) Input is **HSE**.(Top left) **EXT CW** is CW which is input from connector P2 when measuring C/N ratio. **IC8** selects **HSE** or **EXT CW**. **VR200** adjusts the duty of REC data at **IC208**. **Q208** and **Q209** are recording amplifiers for L ch. **REC CUR L** adjusts recording current(L ch). **REC FRE L** adjusts frequency characteristics(L ch). **Q202~Q205** switch mode REC or PB in L ch. **RP HEAD L P** and **N** are output to drum.

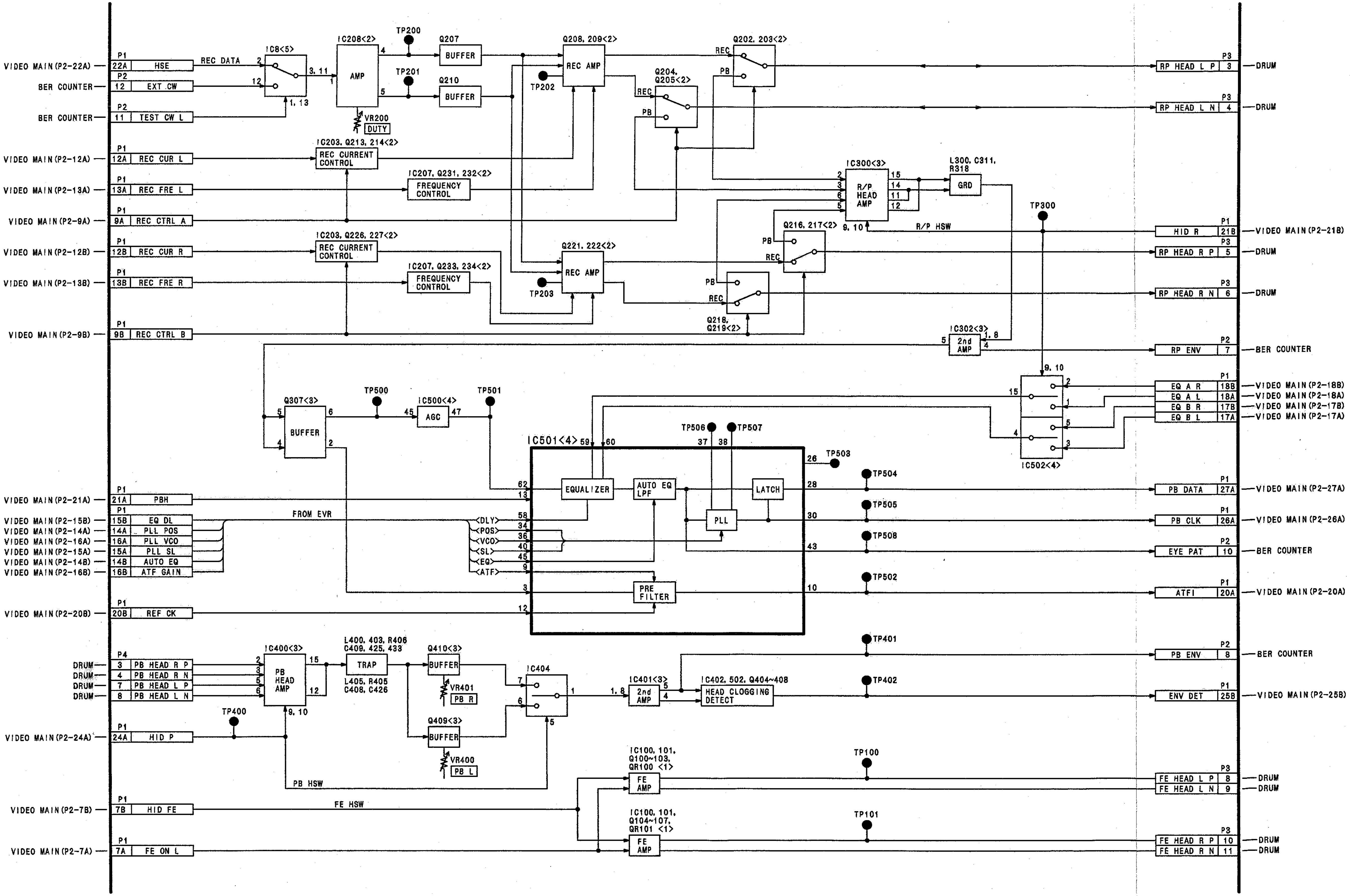
Q221 and **Q222** are recording amplifiers for R ch. **REC CUR R** adjusts recording current(R ch). **REC FRE R** adjusts frequency characteristics(R ch). **Q216~Q219** switch mode REC or PB in R ch. **RP HEAD R P** and **N** are output to drum.

(For playback) **RP HEAD L P** and **N** are input from drum for L ch and supplied to **IC300** of R/P Head Amp via **Q202~Q205**. **RP HEAD R P** and **N** are input from drum for R ch and supplied to **IC300** of R/P Head Amp via **Q226~Q219**. L ch and R ch are multiplexed at **IC300** by **HID R** which is R/P HSW. Both channels data are supplied to **IC501** and equalized by EVR data which are **EQ DL**, **PLL POS**, **PLL SL**, **AUTO EQ**, **EQ α R**, **EQ α L**, **EQ β R** and **EQ β L**. Outputs from **IC501** are **PB DATA** and **PB CLK**.

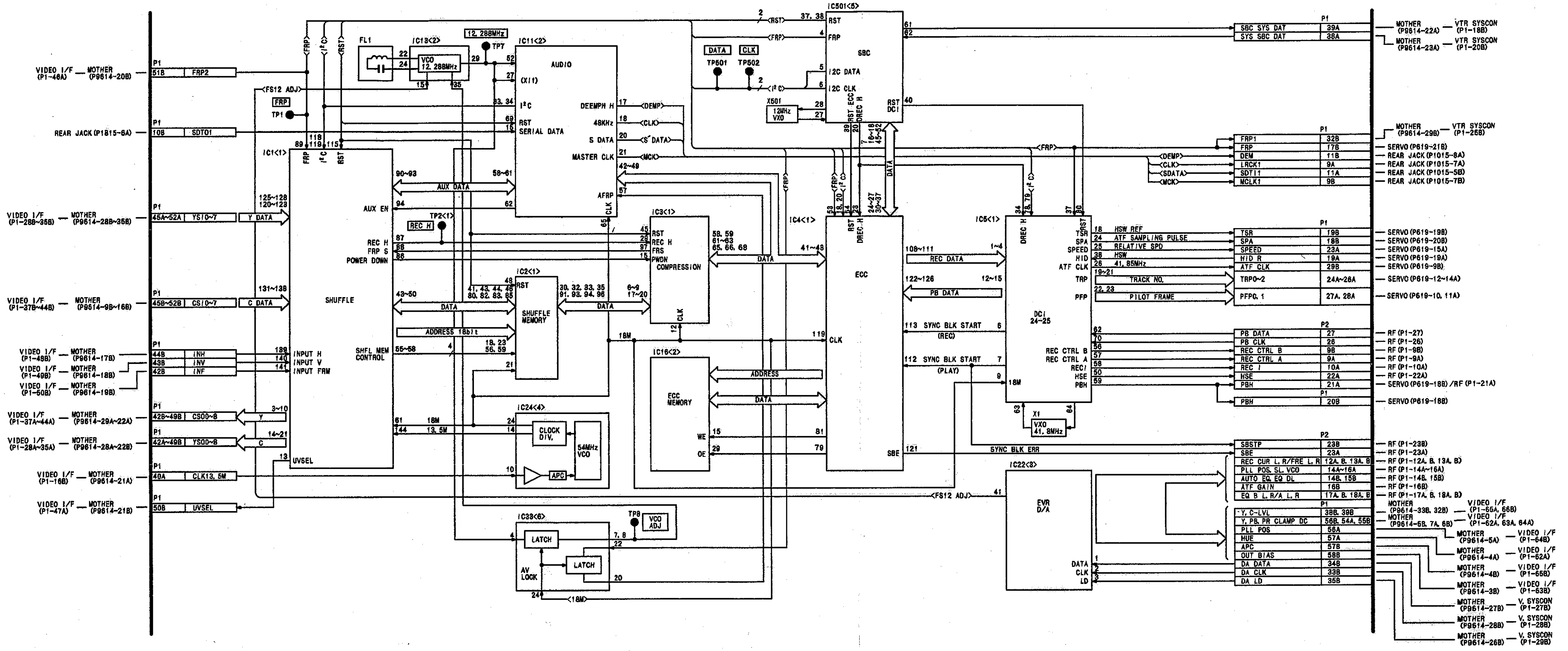
PB HEAD R P and N and **PB HEAD L P** and N are supplied to **IC400** which multiplexes R ch and L ch by **HID P** of PB HSW. Monitoring those signals detects head clogging. Information of head clogging is supplied to VIDEO MAIN P.C.Board as **ENV DET**. **VR400** and **VR401** adjusts detection levels. **TRAP** traps the frequency of the current of Flying Erase Head.

RP ENV, **PB ENV** and **EYE PAT** are available at BNCs of B.E.R.Counter.

RF BLOCK DIAGRAM


VIDEO MAIN(P2-22A)
BER COUNTER
BER COUNTER
VIDEO MAIN(P2-12A)
VIDEO MAIN(P2-13A)
VIDEO MAIN(P2-9A)
VIDEO MAIN(P2-12B)
VIDEO MAIN(P2-13B)
VIDEO MAIN(P2-9B)
VIDEO MAIN(P2-21A)
VIDEO MAIN(P2-15B)
VIDEO MAIN(P2-14A)
VIDEO MAIN(P2-16A)
VIDEO MAIN(P2-15A)
VIDEO MAIN(P2-14B)
VIDEO MAIN(P2-16B)
VIDEO MAIN(P2-20B)
DRUM
DRUM
DRUM
DRUM
VIDEO MAIN(P2-24A)
VIDEO MAIN(P2-7B)
VIDEO MAIN(P2-7A)
P1 22A HSE
P2 12 EXT CW
P2 11 TEST CW L
P1 12A REC CUR L
P1 13A REC FRE L
P1 9A REC CTRL A
P1 12B REC CUR R
P1 13B REC FRE R
P1 9B REC CTRL B
P1 21A PBH
P1 15B EQ DL
14A PLL POS
16A PLL VCO
15A PLL SL
14B AUTO EQ
16B ATF GAIN
P1 20B REF CK
P4 3 PB HEAD R P
4 PB HEAD R N
7 PB HEAD L P
8 PB HEAD L N
P1 24A HID P
P1 7B HID FE
P1 7A FE ON L
REC DATA
IC8<5>
IC208<2>
AMP
TP200
TP201
Q207 BUFFER
Q210 BUFFER
VR200 DUTY
Q208, 209<2> REC AMP
TP202
Q202, 203<2>
Q204, Q205<2>
REC
PB
IC203, Q213, 214<2> REC CURRENT CONTROL
IC207, Q231, 232<2> FREQUENCY CONTROL
IC203, Q226, 227<2> REC CURRENT CONTROL
IC207, Q233, 234<2> FREQUENCY CONTROL
Q221, 222<2> REC AMP
TP203
Q216, 217<2>
Q218, Q219<2>
IC300<3> R/P HEAD AMP
L300, C311, R318 GRD
R/P HSW
TP300
IC302<3> 2nd AMP
IC502<4>
Q307<3> BUFFER
TP500
IC500<4> AGC
TP501
IC501<4>
EQUALIZER
AUTO EQ LPF
LATCH
PLL
PRE FILTER
TP506
TP507
TP503
TP504
TP505
TP508
TP502
FROM EVR
<DLY>
<POS>
<VCO>
<SL>
<EQ>
<ATF>
IC400<3> PB HEAD AMP
L400, 403, R406 C409, 425, 433 TRAP
L405, R405 C408, C426
Q410<3> BUFFER
VR401 PB R
Q409<3> BUFFER
VR400 PB L
IC404
TP400
IC401<3> 2nd AMP
IC402, 502, Q404~408 HEAD CLOGGING DETECT
TP401
TP402
PB HSW
FE HSW
IC100, 101, Q100~103, QR100 <1> FE AMP
IC100, 101, Q104~107, QR101 <1> FE AMP
TP100
TP101
P3 RP HEAD L P 3
P3 RP HEAD L N 4
P1 HID R 21B
P3 RP HEAD R P 5
P3 RP HEAD R N 6
P2 RP ENV 7
P1 EQ A R 18B
EQ A L 18A
EQ B R 17B
EQ B L 17A
P1 PB DATA 27A
P1 PB CLK 26A
P2 EYE PAT 10
P1 ATFI 20A
P2 PB ENV 8
P1 ENV DET 25B
P3 FE HEAD L P 8
FE HEAD L N 9
P3 FE HEAD R P 10
FE HEAD R N 11
DRUM
DRUM
VIDEO MAIN(P2-21B)
DRUM
DRUM
BER COUNTER
VIDEO MAIN(P2-18B)
VIDEO MAIN(P2-18A)
VIDEO MAIN(P2-17B)
VIDEO MAIN(P2-17A)
VIDEO MAIN(P2-27A)
VIDEO MAIN(P2-26A)
BER COUNTER
VIDEO MAIN(P2-20A)
BER COUNTER
VIDEO MAIN(P2-25B)
DRUM
DRUM
DRUM
DRUM

VIDEO MAIN BLOCK DIAGRAM



VIDEO I/F (P1-46A) — MOTHER (P9614-20B)
P1 51B FRP2
REAR JACK (P1815-6A)
P1 10B SDTO1
VIDEO I/F (P1-28B~35B) — MOTHER (P9614-28B~35B)
P1 45A~52A YS I 0~7
Y DATA
VIDEO I/F (P1-37B~44B) — MOTHER (P9614-9B~16B)
P1 45B~52B CS I 0~7
C DATA
VIDEO I/F (P1-48B) — MOTHER (P9614-17B)
VIDEO I/F (P1-49B) — MOTHER (P9614-18B)
VIDEO I/F (P1-50B) — MOTHER (P9614-19B)
P1 44B INH
43B INV
42B INF
VIDEO I/F (P1-37A~44A) — MOTHER (P9614-29A~22A)
P1 42B~49B CS00~8
Y
VIDEO I/F (P1-28A~35A) — MOTHER (P9614-28A~22B)
P1 42A~49B YS00~8
C
VIDEO I/F (P1-16B) — MOTHER (P9614-21A)
P1 40A CLK13.5M
VIDEO I/F (P1-47A) — MOTHER (P9614-21B)
P1 50B UVSEL
<FRP>
<I²C>
<RST>
<FS12 ADJ>
FRP
TP1
IC1<1>
SHUFFLE
INPUT H
INPUT V
INPUT FRM
UVSEL
AUX EN
REC H
FRP S
POWER DOWN
SHFL MEM CONTROL
AUX DATA
DATA
ADDRESS 18bit
TP2<1>
REC H
18M
13.5M
FL1
IC13<2>
VCO 12.288MHz
12.288MHz
TP7
IC11<2>
AUDIO
(X I 1)
I²C
RST
SERIAL DATA
DEEMPH H
48KHz
S DATA
MASTER CLK
AFRP
CLK
<DEMP>
<CLK>
<S DATA>
<MCK>
IC2<1>
SHUFFLE MEMORY
IC24<4>
CLOCK DIV.
54MHz VCO
APC
IC33<6>
LATCH
LATCH
AV LOCK
TP8
VCO ADJ
<18M>
IC3<1>
RST
REC H
FRS
PWDN
COMPRESSION
CLK
IC16<2>
ECC MEMORY
WE
OE
ADDRESS
DATA
IC501<5>
RST
FRP
SBC
I2C DATA
I2C CLK
RST ECC
DREC H
RST DCI
DATA
CLK
TP501
TP502
X501
12MHz VXO
IC4<1>
ECC
CLK
SBE
RST
DREC H
IC5<1>
DCI 24~25
DREC H
RST
TSR
SPA
SPEED
HID
ATF CLK
TRP
PFP
REC CTRL B
REC CTRL A
REC I
HSE
PBH
18M
X1
VXO 41.8MHz
REC DATA
PB DATA
113 SYNC BLK START (REC)
112 SYNC BLK START (PLAY)
SYNC BLK ERR
HSW REF
ATF SAMPLING PULSE
RELATIVE SPD
HSW
41.85MHz
TRACK NO.
PILOT FRAME
IC22<3>
EVR D/A
DATA
CLK
LD
P1 SBC SYS DAT 39A
SYS SBC DAT 38A
MOTHER (P9614-22A) — VTR SYSCON (P1-18B)
MOTHER (P9614-23A) — VTR SYSCON (P1-20B)
P1 FRP1 32B
FRP 17B
DEM 11B
LRCK1 9A
SDTI1 11A
MCLK1 9B
MOTHER (P9614-29B) — VTR SYSCON (P1-25B)
SERVO (P619-21B)
REAR JACK (P1015-8A)
REAR JACK (P1015-7A)
REAR JACK (P1015-5B)
REAR JACK (P1015-7B)
P1 TSR 19B
SPA 18B
SPEED 23A
HID R 19A
ATF CLK 29B
TRPO~2 24A~26A
PFPO, 1 27A, 28A
SERVO (P619-19B)
SERVO (P619-20B)
SERVO (P619-15A)
SERVO (P619-19A)
SERVO (P619-9B)
SERVO (P619-12~14A)
SERVO (P619-10, 11A)
P2 PB DATA 27
PB CLK 26
REC CTRL B 9B
REC CTRL A 9A
REC I 10A
HSE 22A
PBH 21A
P1 PBH 20B
RF (P1-27)
RF (P1-26)
RF (P1-9B)
RF (P1-9A)
RF (P1-10A)
RF (P1-22A)
SERVO (P619-18B) /RF (P1-21A)
SERVO (P619-18B)
P2 SBSTP 23B
SBE 23A
REC CUR L, R/FRE L, R 12A, B, 13A, B
PLL POS, SL, VCO 14A~16A
AUTO EQ, EQ DL 14B, 15B
ATF GAIN 16B
EQ B L, R/A L, R 17A, B, 18A, B
RF (P1-23B)
RF (P1-23A)
RF (P1-12A, B, 13A, B)
RF (P1-14A~16A)
RF (P1-14B, 15B)
RF (P1-16B)
RF (P1-17A, B, 18A, B)
P1 Y, C-LVL 38B, 39B
Y, PB, PR CLAMP DC 56B, 54A, 55B
PLL POS 56A
HUE 57A
APC 57B
OUT BIAS 58B
DA DATA 34B
DA CLK 33B
DA LD 35B
MOTHER (P9614-33B, 32B) — VIDEO I/F (P1-65A, 66B)
MOTHER (P9614-6B, 7A, 6B) — VIDEO I/F (P1-62A, 63A, 64A)
MOTHER (P9614-5A) — VIDEO I/F (P1-64B)
MOTHER (P9614-4A) — VIDEO I/F (P1-62A)
MOTHER (P9614-4B) — VIDEO I/F (P1-65B)
MOTHER (P9614-3B) — VIDEO I/F (P1-63B)
MOTHER (P9614-27B) — V. SYSCON (P1-27B)
MOTHER (P9614-28B) — V. SYSCON (P1-28B)
MOTHER (P9614-26B) — V. SYSCON (P1-29B)

Video Main P.C.Board

This circuit processes shuffling, compression, ECC and 24-25 conversion for recording. In addition to this it makes a reverse process for playback.

(For recording) The Y to be recorded is input to **IC1**, SHUFFLE, as **YSI0~7**. The C to be recorded is also input to **IC1**, SHUFFLE, as **CSI0~7**. **IC2** is a shuffling memory. **IC24** supplies the clocks for **IC1**. Both signals of VIDEO are shuffled and supplied to **IC3** to be compressed.

Audio serial data, **SDTO1,** is supplied from AUDIO LCD P.C Board to **IC11** via Rear Jack P.C.Board.

IC13, VCO, generates master clock for audio. **IC33** compensates the timing between video and audio. Audio signal is shuffled at **IC3**. Video data is compressed at **IC3**. Both are multiplexed and supplied to ECC of **IC4**. Video data is deshuffled at **IC4**. ECC codes are added to video and audio data, which are supplied to **IC5**. When playback, audio signal is separated **IC11** and output as **S DATA**.

IC5 is DCI which means the IC for digital signal processing. DCI makes two kinds of pilot signal for ATF by 24-25 conversion. One has the frequency of 465kHz, the other has the frequency of 697.5kHz.

HSE is the data to be recorded. **REC CTRL A** and **B** switch recording currents ON/OFF in RF circuit.

(For Playback) During playback the same circuit works the opposite process to recording. Input signal from RF Board is **PB DATA** which is supplied to **DCI**.

(Others) **IC22** is D/A converter for EVR data. **IC501** is **SBC** which receives sub code data from VTR Syscon P.C.Board and adds it to video data.

Audio LCD P.C.Board

This circuit has three kinds of audio inputs.

CH1 IN H and **CH1 IN C** are supplied to **RY101** where attenuater ON/OFF is switched. **CH2 IN H** and **CH2 IN C** are supplied to **RY201** where attenuater ON/OFF is switched. **F MIC IN H** and **F MIC IN C** are inputs from front microphone. When phantom microphone is used, 48V is supplied based on **SW 12V**. All of those are supplied to **IC1** of MIC AMP where gains are controlled by **IC603**, Audio CPU.

CH1 is output from the **24th** pin of **IC1**. **SW701** switches balance or unbalance output for 26pin connector. **IC15** of HPF cuts the wind noise. **IC4** switches the HPF ON/OFF. **VR101** coarsely adjusts the level. **FRONT VR** which comes from the VR in front of camera recorder also adjusts CH1 recording level. **IC105** switches the mode. **VR102** adjusts recording level. **IC6** and **Q4** of TEST SG generate 1kHz of tone signal. The level of test tone is adjusted with **VR2**. **IC105** switches test tone or input audio. The signal to be recorded is A/D converted at **IC8** and supplied to Video Main P.C.Board via Rear Jack P.C.Board as **SDTO1**.

CH2 is output from the **13th** pin of **IC1**. **IC15** of HPF cuts the wind noise. **IC4** switches the HPF ON/OFF. **VR201** coarsely adjusts the level. **IC205** switches the mode. **VR202** adjusts recording level. **IC205** switches test tone or input audio.

The audio signal for output is input as **SDTI1** from Video Main P.C.Board via Rear Jack P.C.Board. It is D/A converted at **IC8** and supplied to MIX AMP and MONITOR SELECT. **IC6** and **IC10** of MIX AMP mixes CH1 and CH2. **IC11** selects CH1, CH2 or MIX as monitor outputs L ch and R ch. Selected signal or cue audio is selected at **IC12**. Monitor outputs are supplied as **MON VR IN L** and **R** to ALARM/MONITOR P.C.Board. They return as **MON VR OUT L** and **R** with alarm, **ALARM VR OUT**. **HP OUT L** and **R** are for headphone. **SP OUT** is for speaker.

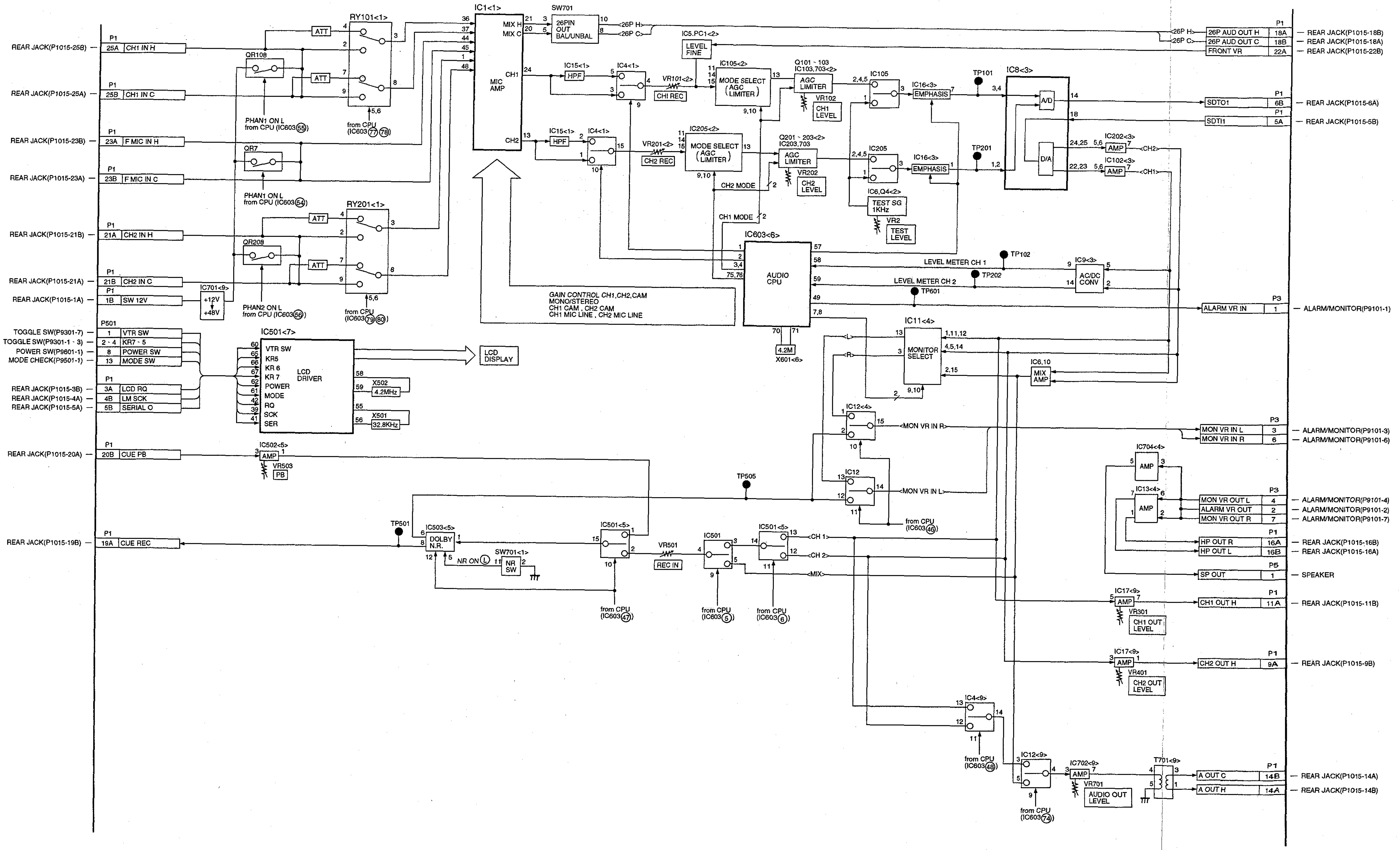
IC17 adjusts CH1 OUT level and CH2 OUT level with **VR301** and **VR401**. Those outputs, **CH1 OUT H** and **CH2 OUT H**, are supplied to 12pin multi connector.

IC501 selects recording signal for CUE audio. **VR501** adjusts recording level in CUE audio. **VR503** adjusts playback level in CUE audio.

A OUT H and **C** are supplied to Rear Jack P.C.Board for AUDIO OUT. **VR701** adjusts the level.

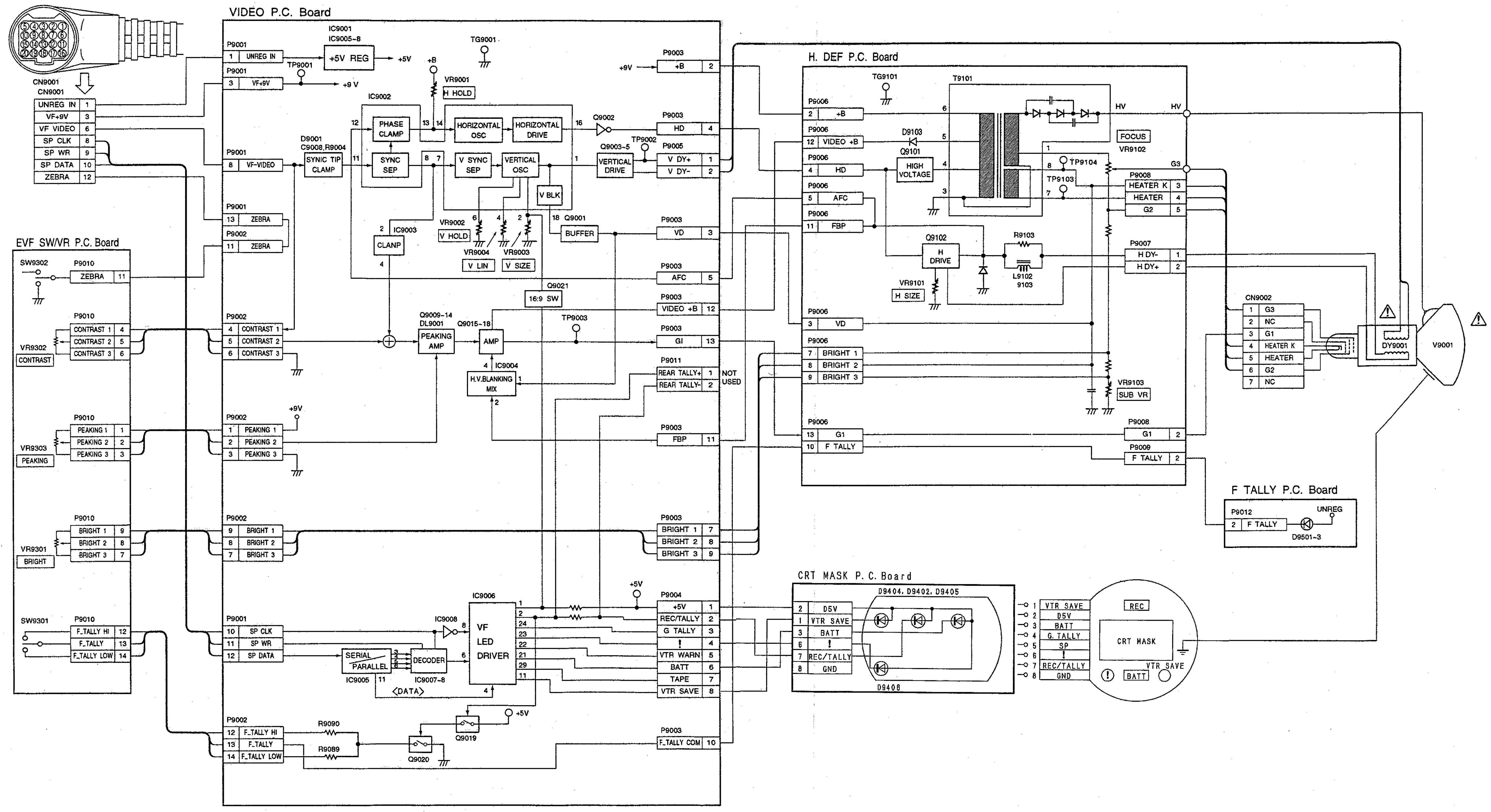
IC501 drives LCD.

AUDIO LCD BLOCK DIAGRAM



REAR JACK(P1015-25B)
REAR JACK(P1015-25A)
REAR JACK(P1015-23B)
REAR JACK(P1015-23A)
REAR JACK(P1015-21B)
REAR JACK(P1015-21A)
REAR JACK(P1015-1A)
TOGGLE SW(P9301-7)
TOGGLE SW(P9301-1・3)
POWER SW(P9601-1)
MODE CHECK(P9501-1)
REAR JACK(P1015-3B)
REAR JACK(P1015-4A)
REAR JACK(P1015-5A)
REAR JACK(P1015-20A)
REAR JACK(P1015-19B)
P1
25A CH1 IN H
25B CH1 IN C
23A F MIC IN H
23B F MIC IN C
21A CH2 IN H
21B CH2 IN C
1B SW 12V
P501
1 VTR SW
2・4 KR7・5
8 POWER SW
13 MODE SW
3A LCD RQ
4B LM SCK
5B SERIAL O
20B CUE PB
19A CUE REC
QR108
PHAN1 ON L
from CPU (IC603 (55))
QR7
PHAN1 ON L
from CPU (IC603 (54))
QR209
PHAN2 ON L
from CPU (IC603 (56))
RY101<1>
RY201<1>
ATT
from CPU (IC603 (77)(78))
from CPU (IC603 (79)(80))
IC701<9>
+12V
+48V
IC1<1>
MIX H
MIX C
MIC AMP
CH1
CH2
SW701
26PIN OUT BAL/UNBAL
<26P H>
<26P C>
IC5,PC1<2>
LEVEL FINE
IC15<1>
HPF
IC4<1>
VR101<2>
CH1 REC
VR201<2>
CH2 REC
IC105<2>
MODE SELECT (AGC LIMITER)
IC205<2>
MODE SELECT (AGC LIMITER)
Q101 ~ 103
IC103,703<2>
AGC LIMITER
VR102
CH1 LEVEL
Q201 ~ 203<2>
IC203,703
AGC LIMITER
VR202
CH2 LEVEL
CH2 MODE
CH1 MODE
IC105
IC205
IC16<3>
EMPHASIS
IC6,Q4<2>
TEST SG 1KHz
VR2
TEST LEVEL
TP101
TP201
IC8<3>
A/D
D/A
IC202<3>
AMP
<CH2>
IC102<3>
AMP
<CH1>
GAIN CONTROL CH1,CH2,CAM
MONO/STEREO
CH1 CAM , CH2 CAM
CH1 MIC LINE , CH2 MIC LINE
IC603<6>
AUDIO CPU
4.2M
X601<6>
TP102
LEVEL METER CH 1
TP202
LEVEL METER CH 2
TP601
IC9<3>
AC/DC CONV
IC501<7>
VTR SW
KR5
KR 6
KR 7
POWER
MODE
RQ
SCK
SER
LCD DRIVER
LCD DISPLAY
X502
4.2MHz
X501
32.8KHz
IC11<4>
MONITOR SELECT
<L>
<R>
IC6,10
MIX AMP
IC12<4>
<MON VR IN R>
IC12
<MON VR IN L>
from CPU (IC603 (46))
IC502<5>
AMP
VR503
PB
TP505
TP501
IC503<5>
DOLBY N.R.
NR ON (L)
SW701<1>
NR SW
IC501<5>
VR501
REC IN
IC501
from CPU (IC603 (47))
from CPU (IC603 (5))
from CPU (IC603 (6))
<CH 1>
<CH 2>
<MIX>
IC704<4>
AMP
IC13<4>
AMP
IC17<9>
AMP
VR301
CH1 OUT LEVEL
IC17<9>
AMP
VR401
CH2 OUT LEVEL
IC4<9>
from CPU (IC603 (48))
IC12<9>
from CPU (IC603 (74))
IC702<9>
AMP
VR701
AUDIO OUT LEVEL
T701<9>
P1
26P AUD OUT H 18A
26P AUD OUT C 18B
FRONT VR 22A
SDTO1 6B
SDTI1 5A
P3
ALARM VR IN 1
MON VR IN L 3
MON VR IN R 6
MON VR OUT L 4
ALARM VR OUT 2
MON VR OUT R 7
HP OUT R 16A
HP OUT L 16B
P5
SP OUT 1
CH1 OUT H 11A
CH2 OUT H 9A
A OUT C 14B
A OUT H 14A
— REAR JACK(P1015-18B)
— REAR JACK(P1015-18A)
— REAR JACK(P1015-22B)
— REAR JACK(P1015-6A)
— REAR JACK(P1015-5B)
— ALARM/MONITOR(P9101-1)
— ALARM/MONITOR(P9101-3)
— ALARM/MONITOR(P9101-6)
— ALARM/MONITOR(P9101-4)
— ALARM/MONITOR(P9101-2)
— ALARM/MONITOR(P9101-7)
— REAR JACK(P1015-16B)
— REAR JACK(P1015-16A)
— SPEAKER
— REAR JACK(P1015-11B)
— REAR JACK(P1015-9B)
— REAR JACK(P1015-14A)
— REAR JACK(P1015-14B)

EVF BLOCK DIAGRAM



VIDEO P.C. Board
CN9001
UNREG IN 1
VF+9V 3
VF VIDEO 6
SP CLK 8
SP WR 9
SP DATA 10
ZEBRA 12
P9001
UNREG IN
VF+9V
VF-VIDEO
ZEBRA
P9002
ZEBRA
IC9001
IC9005-8
+5V REG
+5V
+9V
TP9001
TG9001
+B
VR9001
H HOLD
IC9002
PHASE CLAMP
HORIZONTAL OSC
HORIZONTAL DRIVE
SYNC SEP
V SYNC SEP
VERTICAL OSC
V BLK
D9001
C9008,R9004
SYNIC TIP CLAMP
Q9002
Q9003-5
VERTICAL DRIVE
TP9002
P9003
+B
HD
P9005
V DY+
V DY-
Q9001
BUFFER
VD
AFC
IC9003
CLANP
VR9002
V HOLD
VR9004
V LIN
VR9003
V SIZE
Q9021
16:9 SW
VIDEO +B
GI
Q9009-14
DL9001
PEAKING AMP
Q9015-18
AMP
TP9003
IC9004
H.V.BLANKING MIX
P9011
REAR TALLY+
REAR TALLY-
NOT USED
FBP
EVF SW/VR P.C. Board
SW9302
P9010
ZEBRA
VR9302
CONTRAST
CONTRAST 1
CONTRAST 2
CONTRAST 3
VR9303
PEAKING
PEAKING 1
PEAKING 2
PEAKING 3
VR9301
BRIGHT
BRIGHT 1
BRIGHT 2
BRIGHT 3
SW9301
F_TALLY HI
F_TALLY
F_TALLY LOW
SP CLK
SP WR
SP DATA
IC9008
IC9006
VF LED DRIVER
SERIAL PARALLEL
IC9005
DECODER
IC9007-8
〈DATA〉
P9004
+5V
REC/TALLY
G TALLY
!
VTR WARN
BATT
TAPE
VTR SAVE
R9090
R9089
Q9019
Q9020
F_TALLY COM
H. DEF P.C. Board
TG9101
T9101
P9006
+B
VIDEO +B
HD
AFC
FBP
D9103
Q9101
HIGH VOLTAGE
HV
FOCUS
VR9102
G3
TP9104
TP9103
P9008
HEATER K
HEATER
G2
Q9102
H DRIVE
R9103
L9102
9103
VR9101
H SIZE
P9007
H DY-
H DY+
VD
BRIGHT 1
BRIGHT 2
BRIGHT 3
VR9103
SUB VR
G1
F TALLY
P9009
CN9002
G3
NC
G1
HEATER K
HEATER
G2
NC
DY9001
V9001
F TALLY P.C. Board
P9012
F TALLY
UNREG
D9501-3
CRT MASK P.C.Board
D9404, D9402, D9405
D5V
VTR SAVE
BATT
!
REC/TALLY
GND
D9408
VTR SAVE
D5V
BATT
G.TALLY
SP
!
REC/TALLY
GND
REC
CRT MASK
VTR SAVE
BATT

SECTION 2

SCHEMATIC DIAGRAMS

Schematic Diagrams

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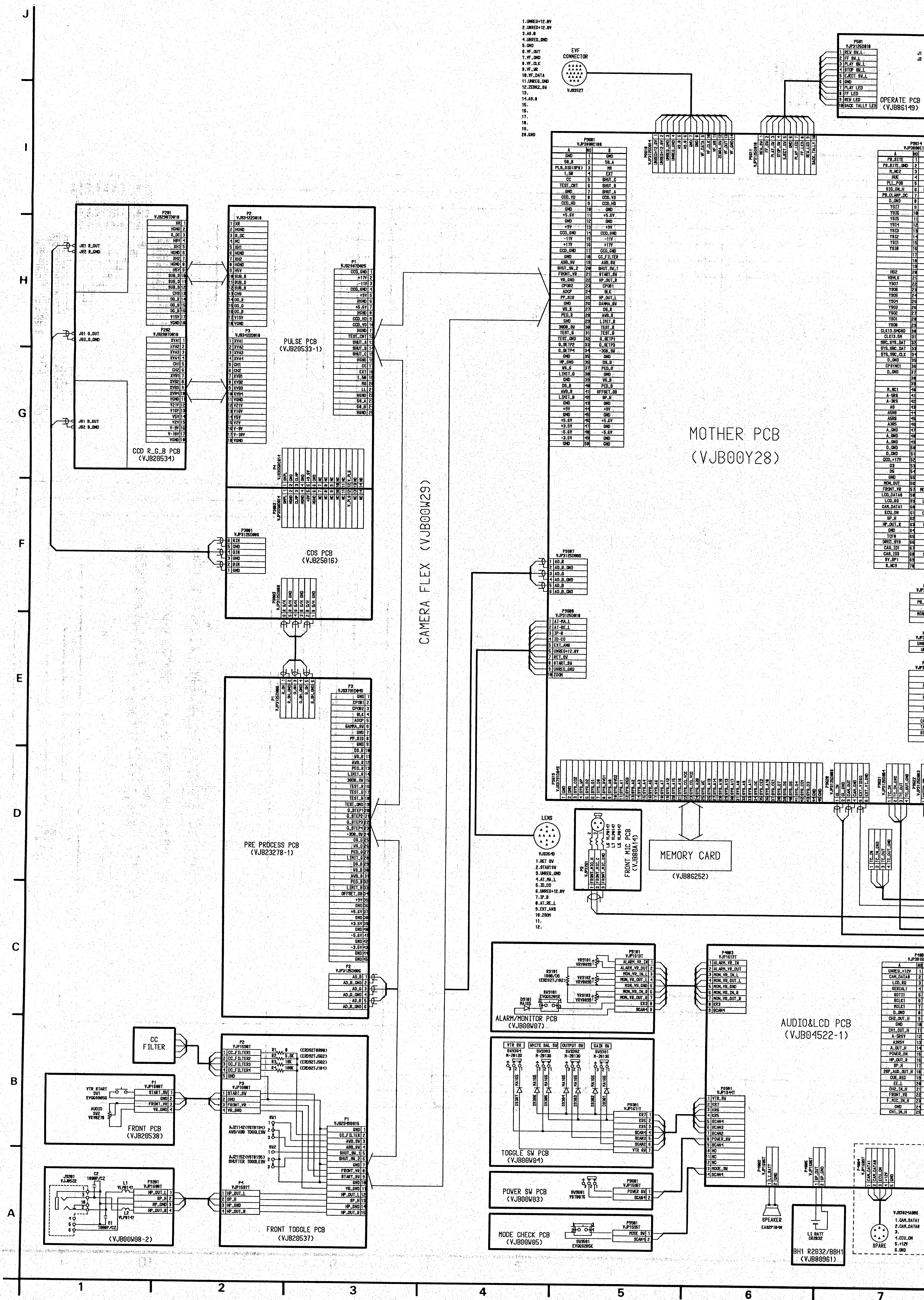
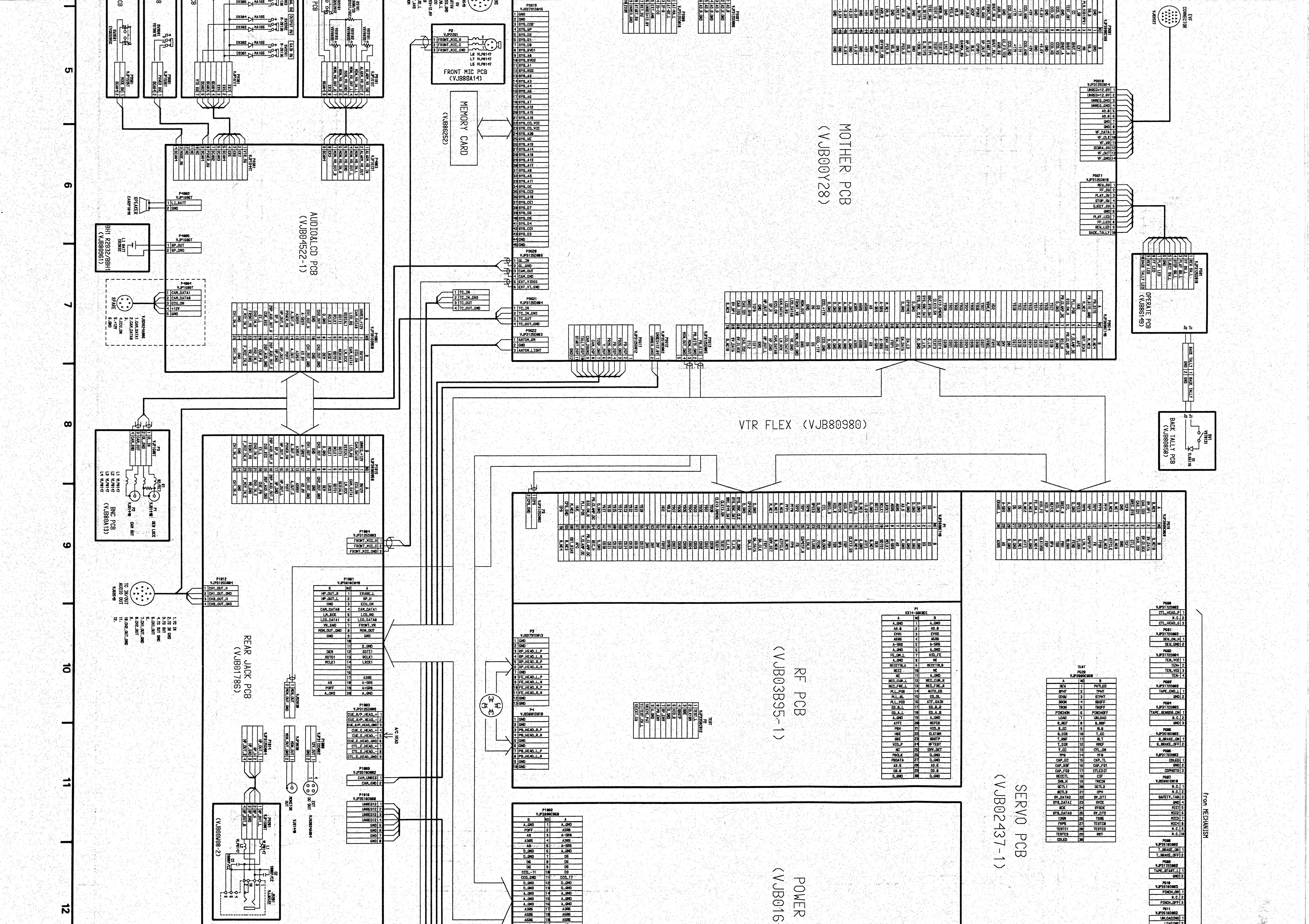
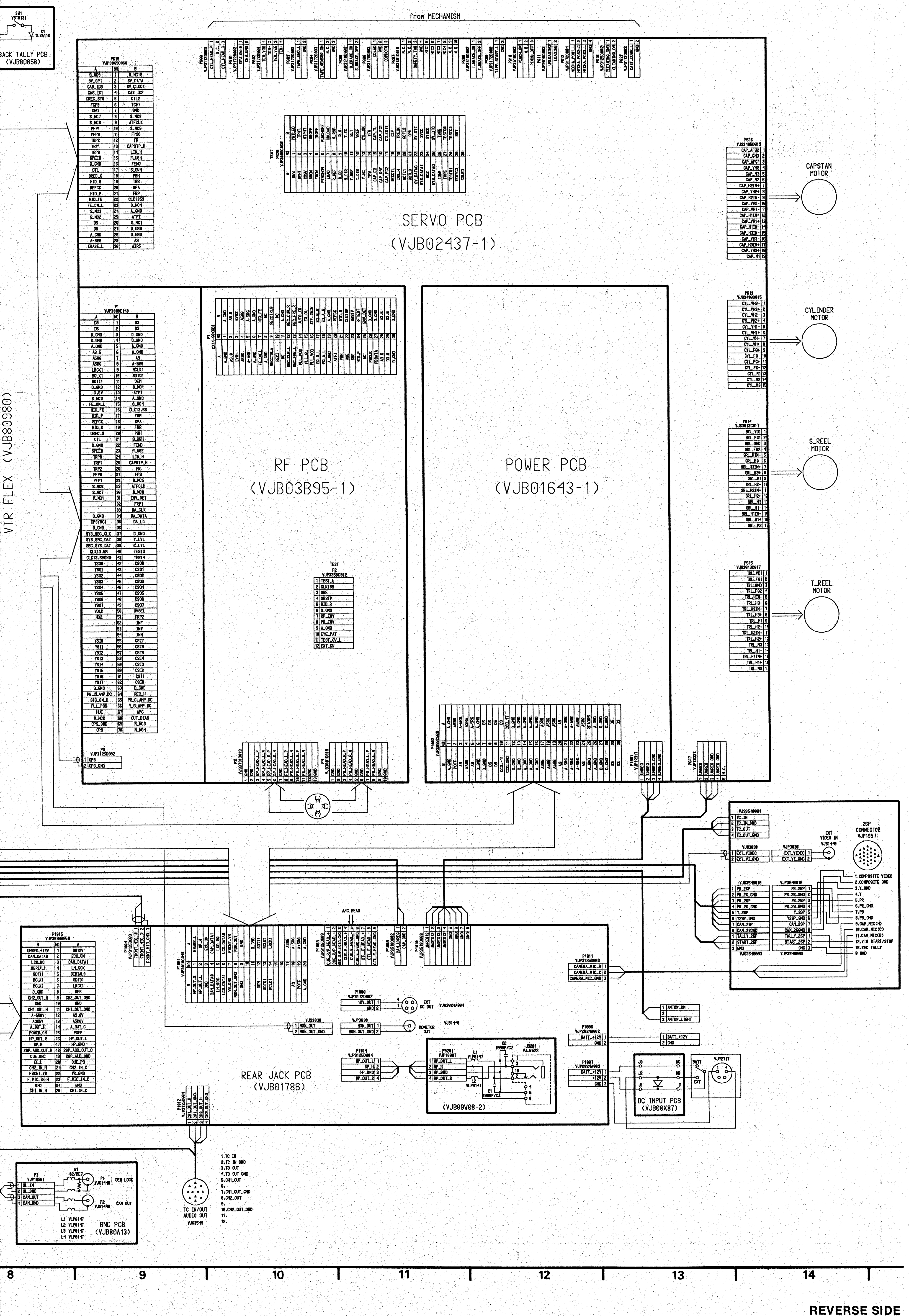
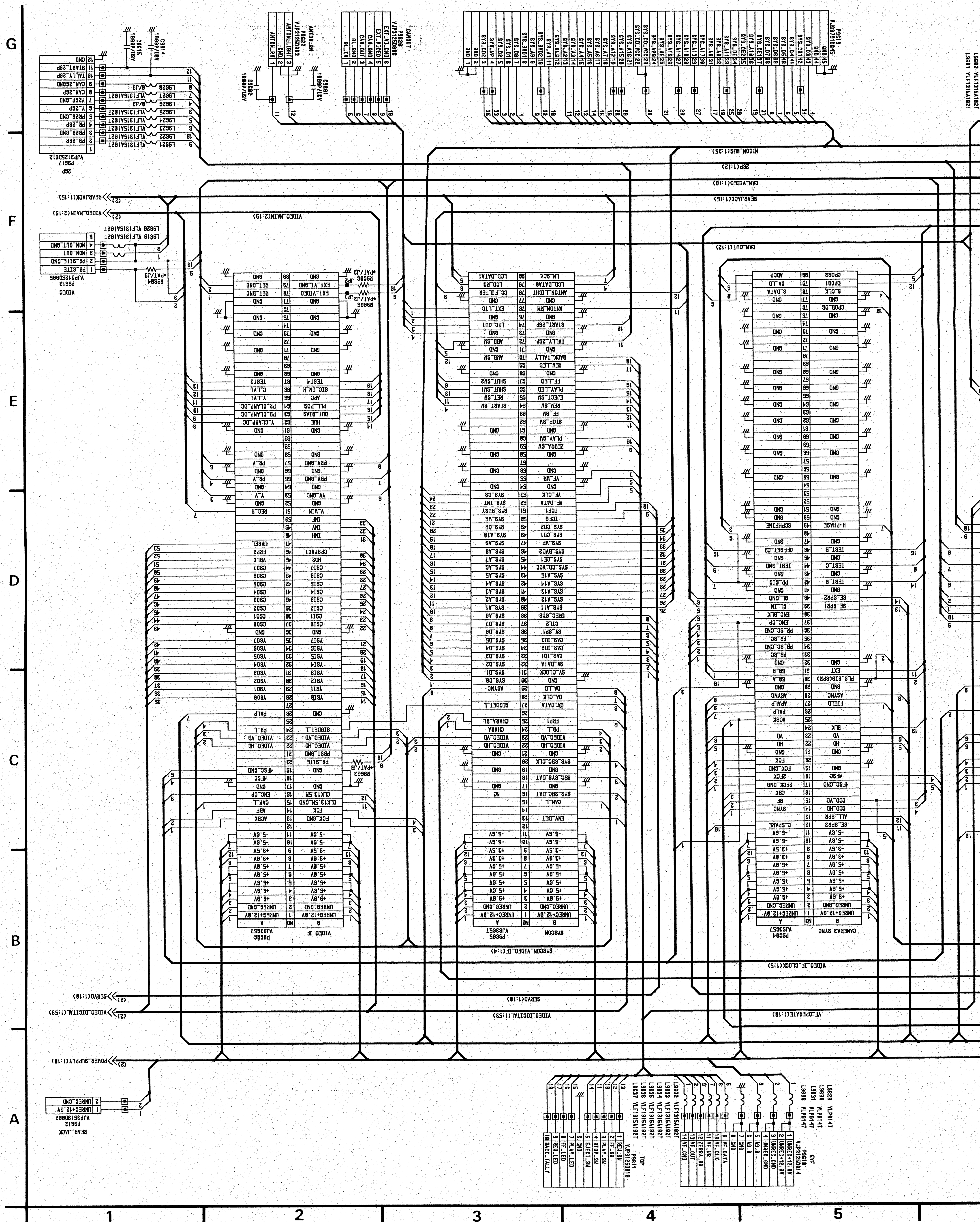
INTERCONNECTION SCHEMATIC DIAGRAM

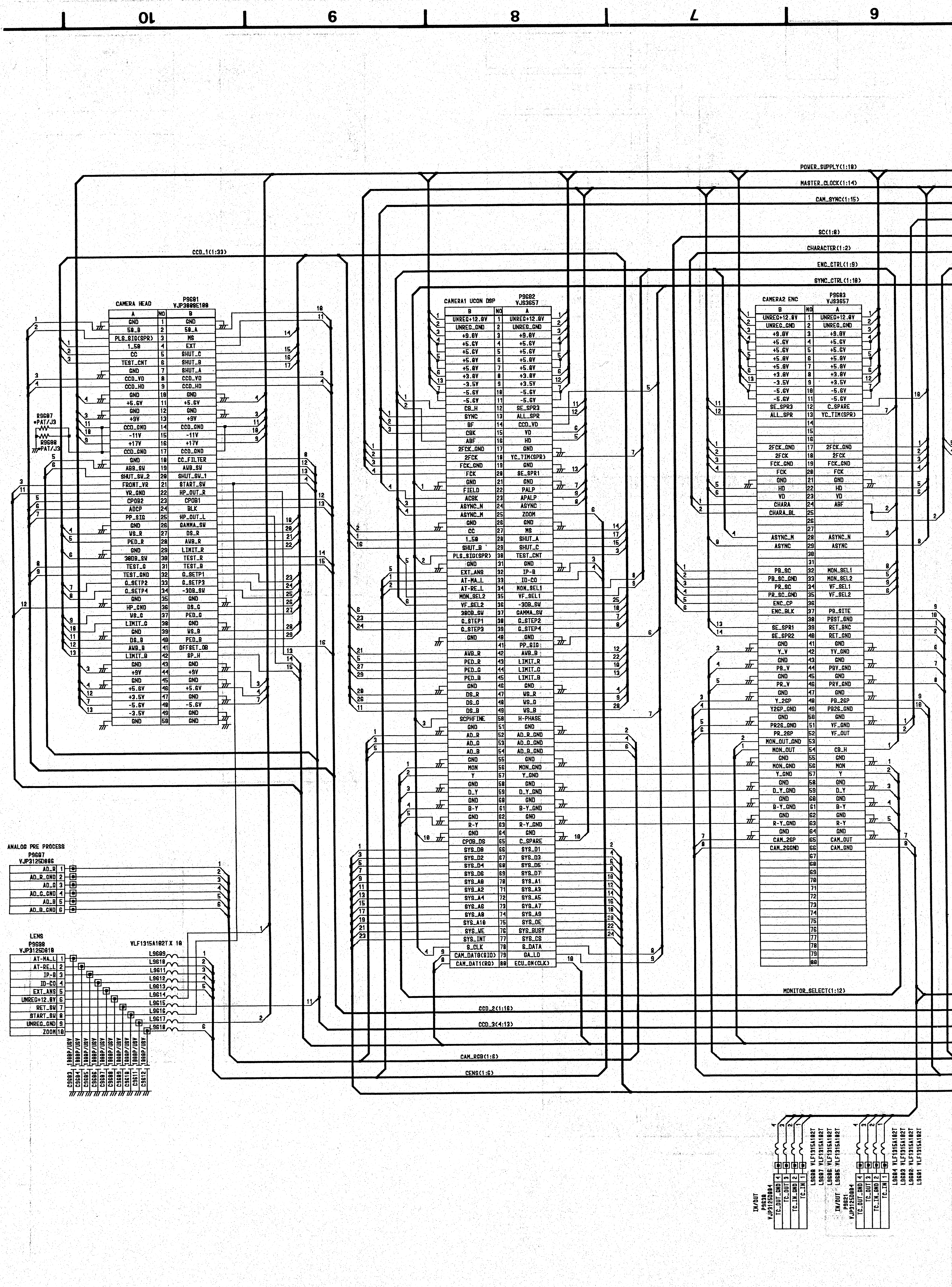

CCD R_G_B PCB
(VJB20534)
PULSE PCB
(VJB20533-1)
CDS PCB
(VJB25016)
PRE PROCESS PCB
(VJB23278-1)
CAMERA FLEX (VJB00W29)
MOTHER PCB
(VJB00Y28)
EVF CONNECTOR
OPERATE PCB
(VJB86149)
CC FILTER
FRONT PCB
(VJB20538)
(VJB00W08-2)
FRONT TOGGLE PCB
(VJB20537)
LENS
FRONT MIC PCB
(VJB80A14)
MEMORY CARD
(VJB86252)
ALARM/MONITOR PCB
(VJB00W07)
TOGGLE SW PCB
(VJB00W04)
POWER SW PCB
(VJB00W03)
MODE CHECK PCB
(VJB00W05)
AUDIO&LCD PCB
(VJB04522-1)
SPEAKER
BH1 R2032/BBH1
(VJB80961)
SPARE
A
B
C
D
E
F
G
H
I
J
1
2
3
4
5
6
7


MOTHER PCB (VJB00Y28)
VTR FLEX (VJB80980)
AUDIO&LCD PCB (VJB04522-1)
REAR JACK PCB (VJB01786)
RF PCB (VJB03B95-1)
SERVO PCB (VJB02437-1)
POWER (VJB016
FRONT MIC PCB (VJB80A14)
MEMORY CARD (VJB86252)
BNC PCB (VJB80A13)
OPERATE PCB (VJB86149)
BACK TALLY PCB (VJB80850)
BH1 R2032/BBH1 (VJB80961)
(VJB80V08-2)
EVF CONNECTOR
SPEAKER
SPARE
from MECHANISM
5
6
7
8
9
10
11
12

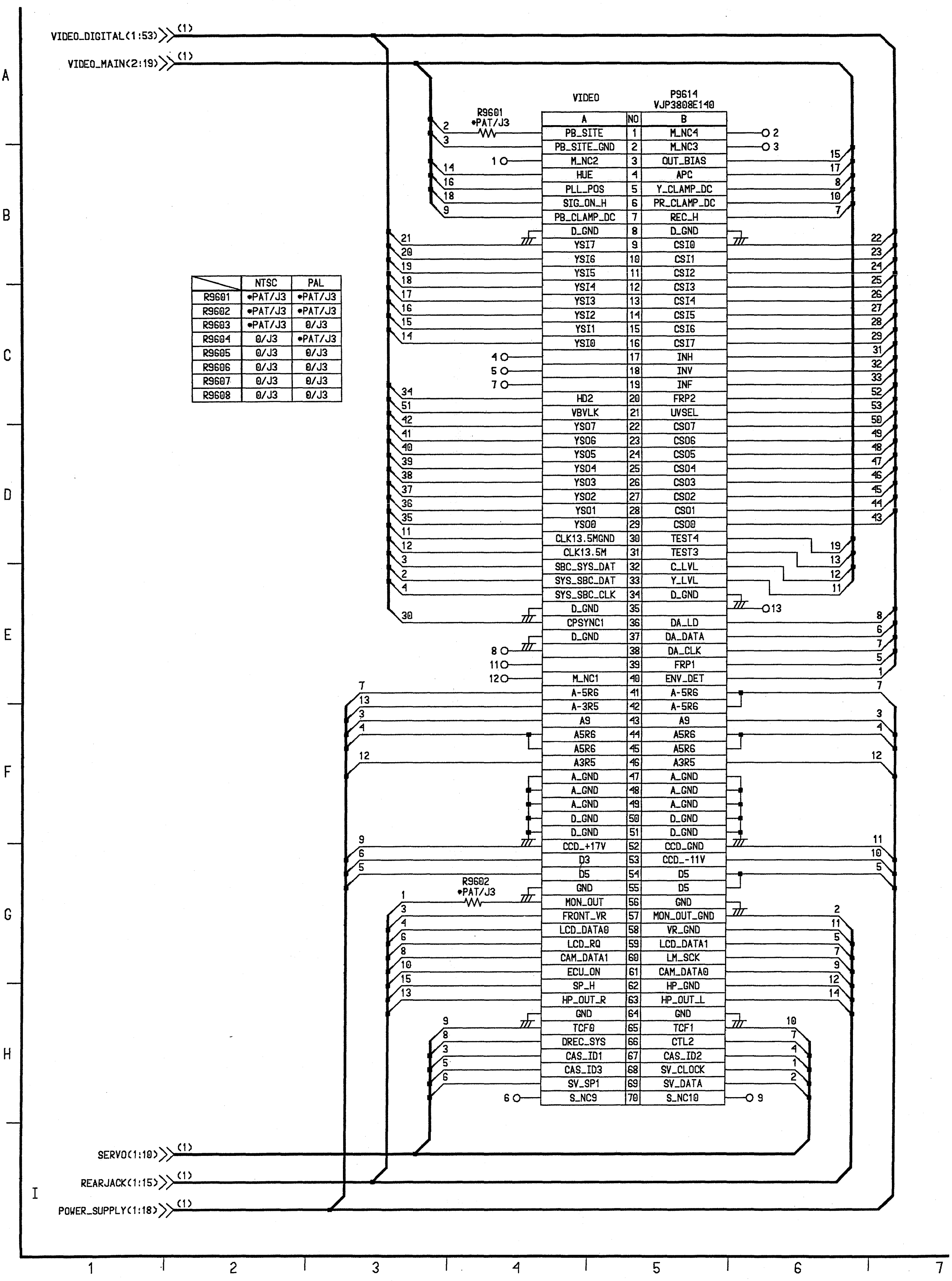

from MECHANISM
BACK TALLY PCB
(VJB80858)
SERVO PCB
(VJB02437-1)
RF PCB
(VJB03B95-1)
POWER PCB
(VJB01643-1)
VTR FLEX (VJB80980)
CAPSTAN MOTOR
CYLINDER MOTOR
S_REEL MOTOR
T_REEL MOTOR
REAR JACK PCB
(VJB01786)
(VJB80W08-2)
DC INPUT PCB
(VJB80X87)
BNC PCB
(VJB80A13)
GEN LOCK
CAM OUT
TC IN/OUT
AUDIO OUT
26P CONNECTOR
VJP1957
EXT VIDEO IN
EXT DC OUT
MONITOR OUT
A/C HEAD
BATT
EXT
8
9
10
11
12
13
14

MOTHER (1/2) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
1
2
3
4
5
REAR_JACK P9612 VJP35180002
UNREG+12.8V
UNREG_GND
POWER_SUPPLY(1:18)
VIDEO_DIGITAL(1:53)
SERVO(1:18)
VF_OPERATE(1:18)
VIDEO_IF_CLOCK(1:5)
SYSCON_VIDEO_IF(1:4)
VIDEO_MAIN(2:19)
REARJACK(1:15)
CAM_VIDEO(1:18)
2SP(1:12)
MICON_BUS(1:35)
CAM_OUT(1:12)
VIDEO IF P9686 VJS3657
SYSCON P9685 VJS3657
CAMERA3 SYNC P9684 VJS3657
VIDEO P9613 VJP3125D805
PB_SITE
PB_SITE_GND
MON_OUT
MON_OUT_GND
2SP P9617 VJP3125D812
ANTON_RM P9622 VJP3125D803
CAMOUT P9628 VJP3125D806
P9619 VJS3791D845
EVF P9618 VJP3125D814
TOP P9611 VJP3125D818
C9614 1000P/U6V
C9615 1000P/U6V
C9681 1000P/U6V
C9682 1000P/U6V
R9684 *PAT/J3
R9685 *PAT/J3
R9686 *PAT/J3
R9683 *PAT/J3
L9619 VLF1315A182T
L9620 VLF1315A182T
L9629 VLP8147
L9630 VLP8147
L9631 VLP8147
L9638 VLP8147
L9681 VLF1315A182T
L9682 VLF1315A182T


10
9
8
7
6
POWER_SUPPLY(1:18)
MASTER_CLOCK(1:14)
CAM_SYNC(1:15)
SC(1:8)
CHARACTER(1:2)
ENC_CTRL(1:9)
SYNC_CTRL(1:10)
CCD_1(1:33)
CCD_2(1:16)
CCD_3(4:13)
CAM_RGB(1:6)
CENS(1:6)
MONITOR_SELECT(1:12)
CAMERA HEAD
P9601
VJP3000E100
A NO B
GND 1 GND
50_B 2 50_A
PLS_SIG(SPR) 3 MS
1_50 4 EXT
CC 5 SHUT_C
TEST_CNT 6 SHUT_B
GND 7 SHUT_A
CCD_VD 8 CCD_VD
CCD_HD 9 CCD_HD
GND 10 GND
+5.6V 11 +5.6V
GND 12 GND
+9V 13 +9V
CCD_GND 14 CCD_GND
-11V 15 -11V
+17V 16 +17V
CCD_GND 17 CCD_GND
GND 18 CC_FILTER
ABB_SW 19 AWB_SW
SHUT_SW_2 20 SHUT_SW_1
FRONT_VR 21 START_SW
VR_GND 22 HP_OUT_R
CPOB2 23 CPOB1
ADCP 24 BLK
PP_SIG 25 HP_OUT_L
GND 26 GAMMA_SW
VS_R 27 DS_R
PED_R 28 AWB_R
GND 29 LIMIT_R
30DB_SW 30 TEST_R
TEST_G 31 TEST_B
TEST_GND 32 G_SETP1
G_SETP2 33 G_SETP3
G_SETP4 34 -3DB_SW
GND 35 GND
HP_GND 36 DS_G
VS_G 37 PED_G
LIMIT_G 38 GND
GND 39 WS_B
DS_B 40 PED_B
AWB_B 41 OFFSET_OB
LIMIT_B 42 SP_H
GND 43 GND
+9V 44 +9V
GND 45 GND
+5.6V 46 +5.6V
+3.5V 47 GND
-5.6V 48 -5.6V
-3.5V 49 GND
GND 50 GND
R9607
•PAT/J3
R9608
•PAT/J3
CAMERA1 UCON DSP
P9602
VJS3657
B NO A
UNREG+12.0V 1 UNREG+12.0V
UNREG_GND 2 UNREG_GND
+9.0V 3 +9.0V
+5.6V 4 +5.6V
+5.6V 5 +5.6V
+5.0V 6 +5.0V
+5.0V 7 +5.0V
+3.0V 8 +3.0V
-3.5V 9 +3.5V
-5.6V 10 -5.6V
-5.6V 11 -5.6V
CB_H 12 SE_SPR3
SYNC 13 ALL_SPR
BF 14 CCD_VD
CBK 15 VD
ABF 16 HD
2FCK_GND 17 GND
2FCK 18 YC_TIM(SPR)
FCK_GND 19 GND
FCK 20 SE_SPR1
GND 21 GND
FIELD 22 PALP
ACBK 23 APALP
ASYNC_N 24 ASYNC
ASYNC_M 25 ZOOM
GND 26 GND
CC 27 MS
1_50 28 SHUT_A
SHUT_B 29 SHUT_C
PLS_SIG(SPR) 30 TEST_CNT
GND 31 GND
EXT_ANS 32 IP-B
AT-MA_L 33 ID-CO
AT-RE_L 34 MON_SEL1
MON_SEL2 35 VF_SEL1
VF_SEL2 36 -3DB_SW
30DB_SW 37 GAMMA_SW
G_STEP1 38 G_STEP2
G_STEP3 39 G_STEP4
GND 40 GND
41 PP_SIG
AWB_R 42 AWB_B
PED_R 43 LIMIT_R
PED_G 44 LIMIT_G
PED_B 45 LIMIT_B
GND 46 GND
DS_R 47 WS_R
DS_G 48 WS_G
DS_B 49 WS_B
SCPHFINE 50 H-PHASE
GND 51 GND
AD_R 52 AD_R_GND
AD_G 53 AD_G_GND
AD_B 54 AD_B_GND
GND 55 GND
MON 56 MON_GND
Y 57 Y_GND
GND 58 GND
D_Y 59 D_Y_GND
GND 60 GND
B-Y 61 B-Y_GND
GND 62 GND
R-Y 63 R-Y_GND
GND 64 GND
CPOB_DS 65 C_SPARE
SYS_D0 66 SYS_D1
SYS_D2 67 SYS_D3
SYS_D4 68 SYS_D5
SYS_D6 69 SYS_D7
SYS_A0 70 SYS_A1
SYS_A2 71 SYS_A3
SYS_A4 72 SYS_A5
SYS_A6 73 SYS_A7
SYS_A8 74 SYS_A9
SYS_A10 75 SYS_OE
SYS_WE 76 SYS_BUSY
SYS_INT 77 SYS_CS
S_CLK 78 S_DATA
CAM_DAT0(SIO) 79 GA_LD
CAM_DAT1(RO) 80 ECU_ON(CLK)
CAMERA2 ENC
P9603
VJS3657
B NO A
UNREG+12.0V 1 UNREG+12.0V
UNREG_GND 2 UNREG_GND
+9.0V 3 +9.0V
+5.6V 4 +5.6V
+5.6V 5 +5.6V
+5.0V 6 +5.0V
+5.0V 7 +5.0V
+3.0V 8 +3.0V
-3.5V 9 +3.5V
-5.6V 10 -5.6V
-5.6V 11 -5.6V
SE_SPR3 12 C_SPARE
ALL_SPR 13 YC_TIM(SPR)
14
15
16
2FCK_GND 17 2FCK_GND
2FCK 18 2FCK
FCK_GND 19 FCK_GND
FCK 20 FCK
GND 21 GND
HD 22 HD
VD 23 VD
CHARA 24 ABF
CHARA_BL 25
26
27
ASYNC_M 28 ASYNC_N
ASYNC 29 ASYNC
30
31
PB_SC 32 MON_SEL1
PB_SC_GND 33 MON_SEL2
PR_SC 34 VF_SEL1
PR_SC_GND 35 VF_SEL2
ENC_CP 36
ENC_BLK 37 PB_SITE
38 PBST_GND
SE_SPR1 39 RET_BNC
SE_SPR2 40 RET_GND
GND 41 GND
Y_V 42 YV_GND
GND 43 GND
PB_V 44 PBV_GND
GND 45 GND
PR_V 46 PRV_GND
GND 47 GND
Y_26P 48 PB_26P
Y26P_GND 49 PB26_GND
GND 50 GND
PR26_GND 51 VF_GND
PR_26P 52 VF_OUT
MON_OUT_GND 53
MON_OUT 54 CB_H
GND 55 GND
MON_GND 56 MON
Y_GND 57 Y
GND 58 GND
D_Y_GND 59 D_Y
GND 60 GND
B-Y_GND 61 B-Y
GND 62 GND
R-Y_GND 63 R-Y
GND 64 GND
CAM_26P 65 CAM_OUT
CAM_26GND 66 CAM_GND
67
68
69
70
71
72
73
74
75
76
77
78
79
80
ANALOG PRE PROCESS
P9607
VJP3125D006
AD_R 1
AD_R_GND 2
AD_G 3
AD_G_GND 4
AD_B 5
AD_B_GND 6
LENS
P9608
VJP3125D010
AT-MA_L 1
AT-RE_L 2
IP-B 3
ID-CO 4
EXT_ANS 5
UNREG+12.0V 6
RET_SW 7
START_SW 8
UNREG_GND 9
ZOOM 10
VLF1315A102T X 10
L9609
L9610
L9611
L9612
L9613
L9614
L9615
L9616
L9617
L9618
1000P/USV
C9603
C9604
C9605
C9606
C9607
C9608
C9609
C9610
C9611
C9612
IN/OUT
P9630
VJP3125D004
TC_OUT_GND 4
TC_OUT 3
TC_IN_GND 2
TC_IN 1
L9608 VLF1315A102T
L9607 VLF1315A102T
L9606 VLF1315A102T
L9605 VLF1315A102T
IN/OUT
P9621
VJP3125D004
TC_OUT_GND 4
TC_OUT 3
TC_IN_GND 2
TC_IN 1
L9604 VLF1315A102T
L9603 VLF1315A102T
L9602 VLF1315A102T
L9601 VLF1315A102T

MOTHER (2/2) SCHEMATIC DIAGRAM


VIDEO_DIGITAL(1:53) (1)
VIDEO_MAIN(2:19) (1)
SERVO(1:10) (1)
REARJACK(1:15) (1)
POWER_SUPPLY(1:18) (1)
R9601 *PAT/J3
R9602 *PAT/J3
VIDEO
P9614
VJP3808E140
A | NO | B
PB_SITE 1 M_NC4
PB_SITE_GND 2 M_NC3
M_NC2 3 OUT_BIAS
HUE 4 APC
PLL_POS 5 Y_CLAMP_DC
SIG_ON_H 6 PR_CLAMP_DC
PB_CLAMP_DC 7 REC_H
D_GND 8 D_GND
YSI7 9 CSI0
YSI6 10 CSI1
YSI5 11 CSI2
YSI4 12 CSI3
YSI3 13 CSI4
YSI2 14 CSI5
YSI1 15 CSI6
YSI0 16 CSI7
17 INH
18 INV
19 INF
HD2 20 FRP2
VBVLK 21 UVSEL
YSO7 22 CSO7
YSO6 23 CSO6
YSO5 24 CSO5
YSO4 25 CSO4
YSO3 26 CSO3
YSO2 27 CSO2
YSO1 28 CSO1
YSO0 29 CSO0
CLK13.5MGND 30 TEST4
CLK13.5M 31 TEST3
SBC_SYS_DAT 32 C_LVL
SYS_SBC_DAT 33 Y_LVL
SYS_SBC_CLK 34 D_GND
D_GND 35
CPSYNC1 36 DA_LD
D_GND 37 DA_DATA
38 DA_CLK
39 FRP1
M_NC1 40 ENV_DET
A-5R6 41 A-5R6
A-3R5 42 A-5R6
A9 43 A9
A5R6 44 A5R6
A5R6 45 A5R6
A3R5 46 A3R5
A_GND 47 A_GND
A_GND 48 A_GND
A_GND 49 A_GND
D_GND 50 D_GND
D_GND 51 D_GND
CCD_+17V 52 CCD_GND
D3 53 CCD_-11V
D5 54 D5
GND 55 D5
MON_OUT 56 GND
FRONT_VR 57 MON_OUT_GND
LCD_DATA0 58 VR_GND
LCD_RQ 59 LCD_DATA1
CAM_DATA1 60 LM_SCK
ECU_ON 61 CAM_DATA0
SP_H 62 HP_GND
HP_OUT_R 63 HP_OUT_L
GND 64 GND
TCF0 65 TCF1
DREC_SYS 66 CTL2
CAS_ID1 67 CAS_ID2
CAS_ID3 68 SV_CLOCK
SV_SP1 69 SV_DATA
S_NC9 70 S_NC10
A
B
C
D
E
F
G
H
I
1
2
3
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6
7

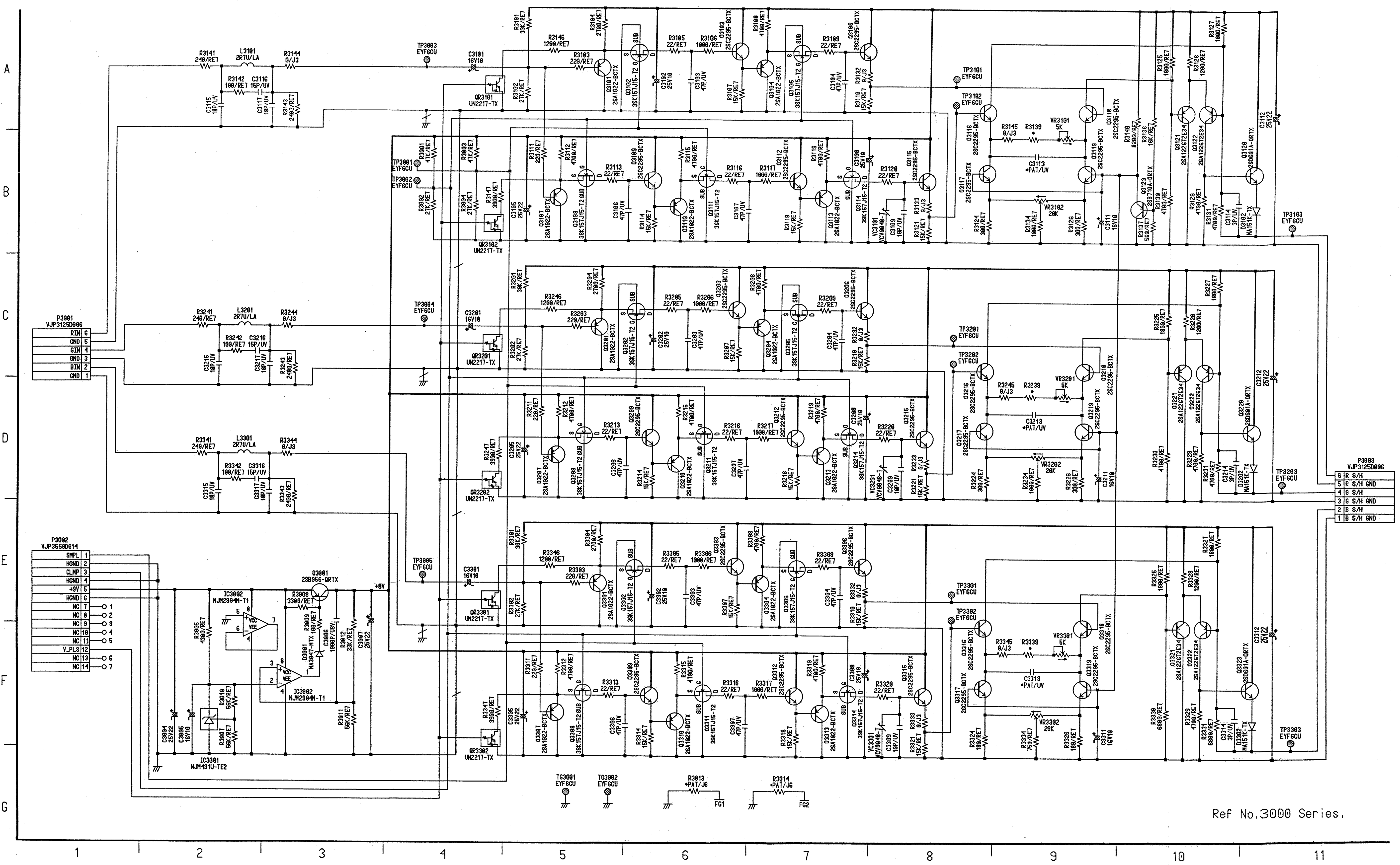
	NTSC	PAL
R9601	*PAT/J3	*PAT/J3
R9602	*PAT/J3	*PAT/J3
R9603	*PAT/J3	0/J3
R9604	0/J3	*PAT/J3
R9605	0/J3	0/J3
R9606	0/J3	0/J3
R9607	0/J3	0/J3
R9608	0/J3	0/J3

CDS (1/2) COMPARISON CHART BETWEEN MODELS

============ ============ ============ ============

REF	NTSC	PAL	ON
R3139	3900/RE7	1800/RE7	3900/RE7
R3239	6200/RE7	3000/RE7	6200/RE7
R3339	1800/RE7	1000/RE7	1800/RE7

CDS (2/2) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
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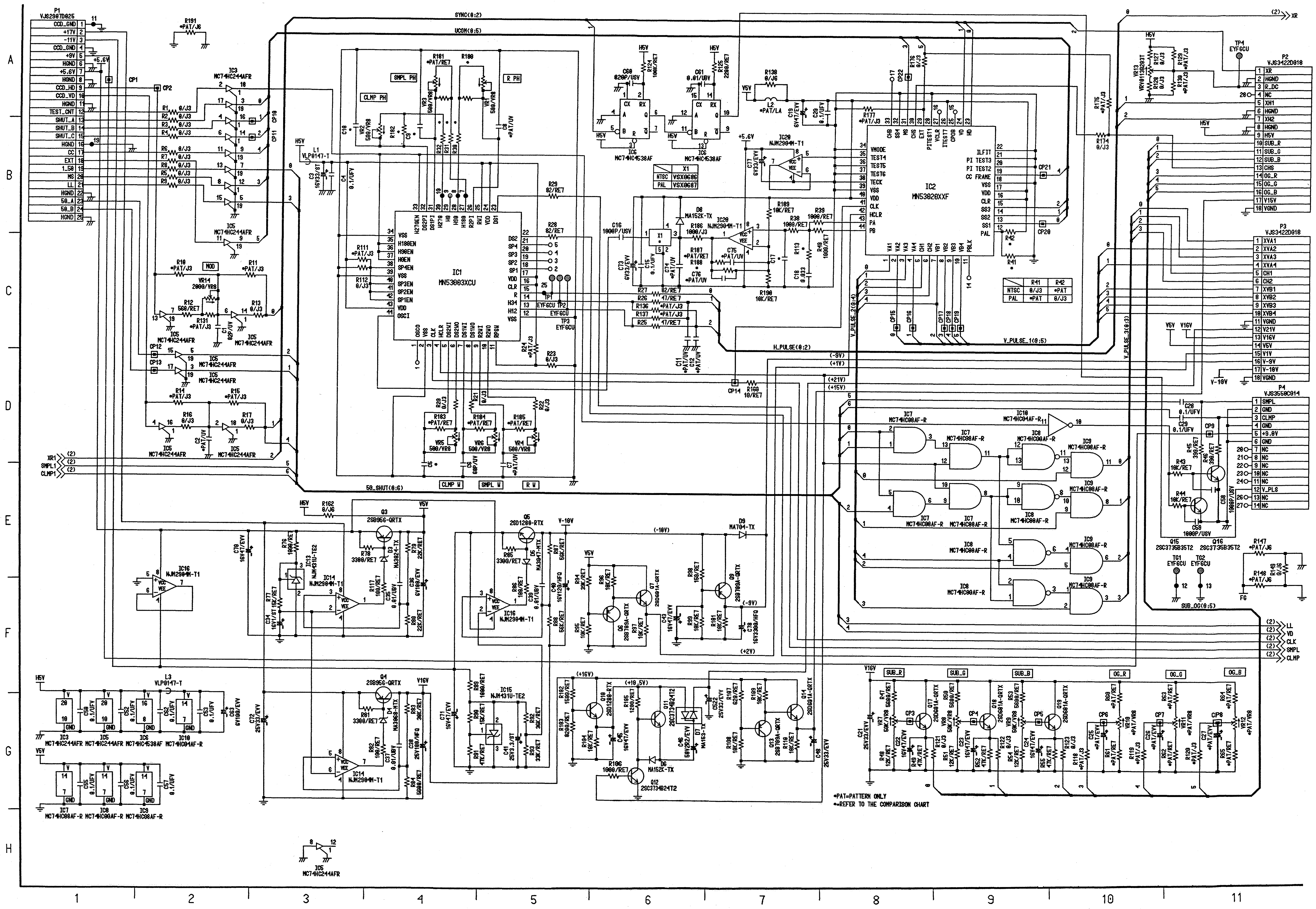
9
10
11
P3001
VJP3125D006
RIN 6
GND 5
GIN 4
GND 3
BIN 2
GND 1
P3002
VJP3550D014
SMPL 1
HGND 2
CLMP 3
HGND 4
+9V 5
HGND 6
NC 7
NC 8
NC 9
NC 10
NC 11
V_PLS 12
NC 13
NC 14
P3003
VJP3125D006
6 R S/H
5 R S/H GND
4 G S/H
3 G S/H GND
2 B S/H
1 B S/H GND
R3141 240/RE7
L3101 2R7U/LA
R3144 0/J3
R3241 240/RE7
L3201 2R7U/LA
R3244 0/J3
R3341 240/RE7
L3301 2R7U/LA
R3344 0/J3
TP3003 EYF6CU
TP3004 EYF6CU
TP3005 EYF6CU
TP3101 EYF6CU
TP3102 EYF6CU
TP3103 EYF6CU
TP3201 EYF6CU
TP3202 EYF6CU
TP3203 EYF6CU
TP3301 EYF6CU
TP3302 EYF6CU
TP3303 EYF6CU
TP3001 EYF6CU
TP3002 EYF6CU
QR3101 UN2217-TX
QR3102 UN2217-TX
QR3201 UN2217-TX
QR3202 UN2217-TX
QR3301 UN2217-TX
QR3302 UN2217-TX
IC3001 NJM431U-TE2
IC3002 NJM2904M-T1
Q3001 2SB956-QRTX
D3001 MA3047-HTX
+8V
TG3001 EYF6CU
TG3002 EYF6CU
R3013 *PAT/J6
R3014 *PAT/J6
FG1
FG2
Ref No.3000 Series.

PULSE (1/4) SCHEMATIC DIAGRAM


P1
VJS2907D025
CCD_GND
+17V
-11V
+9V
HGND
+5.6V
CCD_HD
CCD_VD
TEST_CNT
SHUT_A
SHUT_B
SHUT_C
CC
EXT
L_50
MS
LL
50_A
50_B
R191
*PAT/J6
IC3
MC74HC244AFR
IC5
MC74HC244AFR
CP1
CP2
SYNC(0:2)
UCON(0:5)
SMPL PH
CLMP PH
R PH
IC1
MN53003XCU
IC2
MN53020XXF
IC6
MC74HC4538AF
IC29
NJM2904M-T1
NTSC
PAL
X1
VSX0686
VSX0687
IC7
MC74HC08AF-R
IC8
MC74HC08AF-R
IC9
MC74HC08AF-R
IC10
MC74HC04AF-R
IC13
NJM431U-TE2
IC14
NJM2904M-T1
IC15
NJM431U-TE2
IC16
NJM2904M-T1
Q3
2SB956-QRTX
Q4
2SB956-QRTX
Q5
2SD1280-RTX
Q7
2SD601A-QRTX
Q9
2SB709A-QRTX
Q12
2SC3734B24T2
Q15
2SC3735B35T2
Q16
2SC3735B35T2
Q17
Q18
Q19
2SD601A-QRTX
P2
VJS3422D018
P3
VJS3422D018
P4
VJS3558C014
TP4
EYF6CU
XR
H_PULSE(0:2)
V_PULSE_1(0:5)
V_PULSE_2(0:4)
V_PULSE_3(0:3)
SUB_OG(0:5)
50_SHUT(0:6)
CLMP W
SMPL W
R W
SUB_R
SUB_G
SUB_B
OG_R
OG_G
OG_B
LL
VD
CLK
SMPL
CLMP
XR
SMPL
CLMP
*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART
A
B
C
D
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F
G
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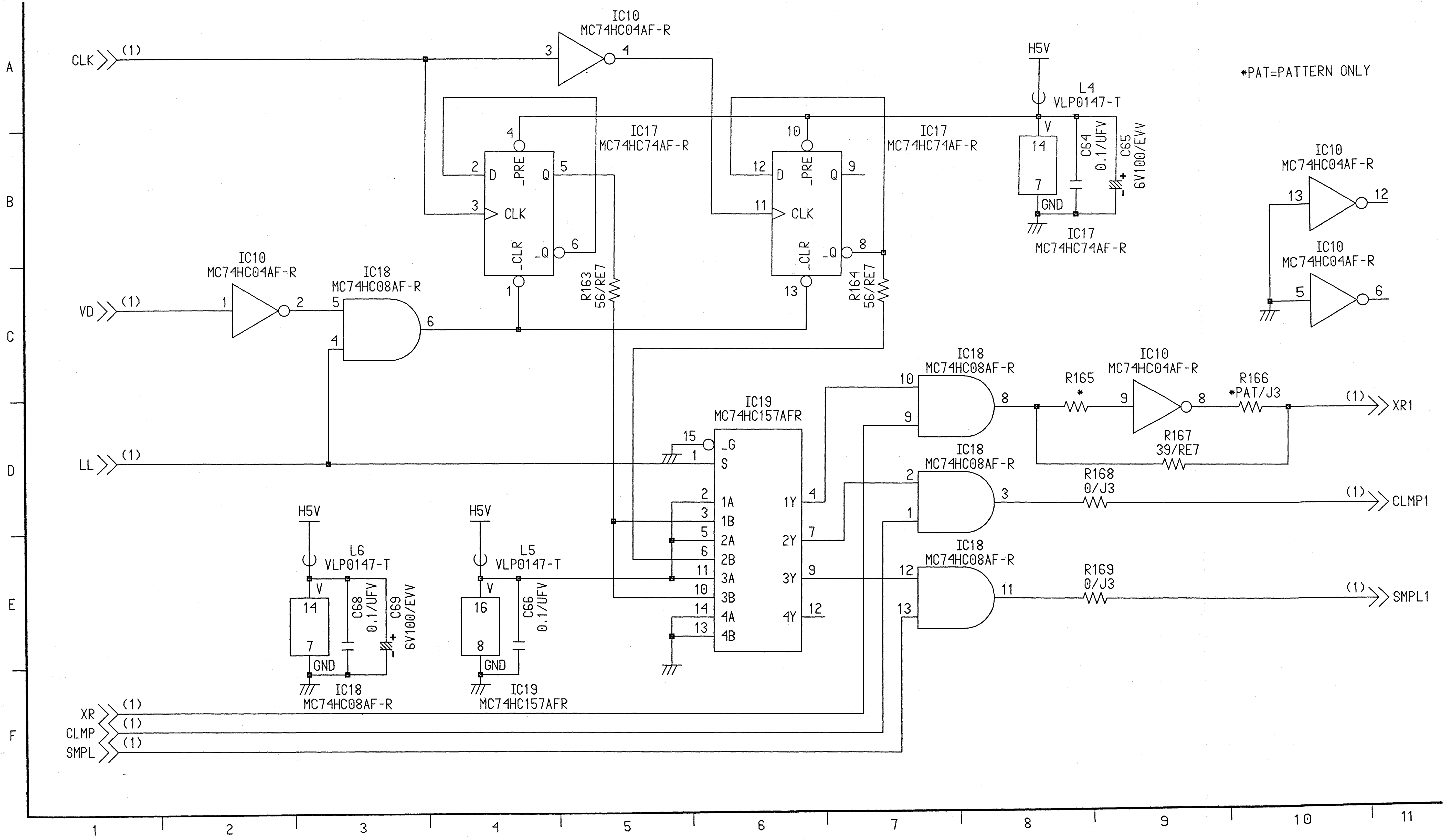
REVERSE SIDE

CDS

PULSE (2/4) SCHEMATIC DIAGRAM


*PAT=PATTERN ONLY
CLK (1)
VD (1)
LL (1)
XR (1)
CLMP (1)
SMPL (1)
(1) XR1
(1) CLMP1
(1) SMPL1
IC10 MC74HC04AF-R
IC17 MC74HC74AF-R
IC18 MC74HC08AF-R
IC19 MC74HC157AFR
D
_PRE
Q
CLK
_CLR
_Q
_G
S
1A
1B
2A
2B
3A
3B
4A
4B
1Y
2Y
3Y
4Y
H5V
L4 VLP0147-T
L5 VLP0147-T
L6 VLP0147-T
C64 0.1/UFV
C65 6V100/EVV
C66 0.1/UFV
C68 0.1/UFV
C69 6V100/EVV
R163 56/RE7
R164 56/RE7
R165 *
R166 *PAT/J3
R167 39/RE7
R168 0/J3
R169 0/J3
V
GND
A
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PULSE (3/4) COMPARISON CHART 1 BETWEEN MODELS

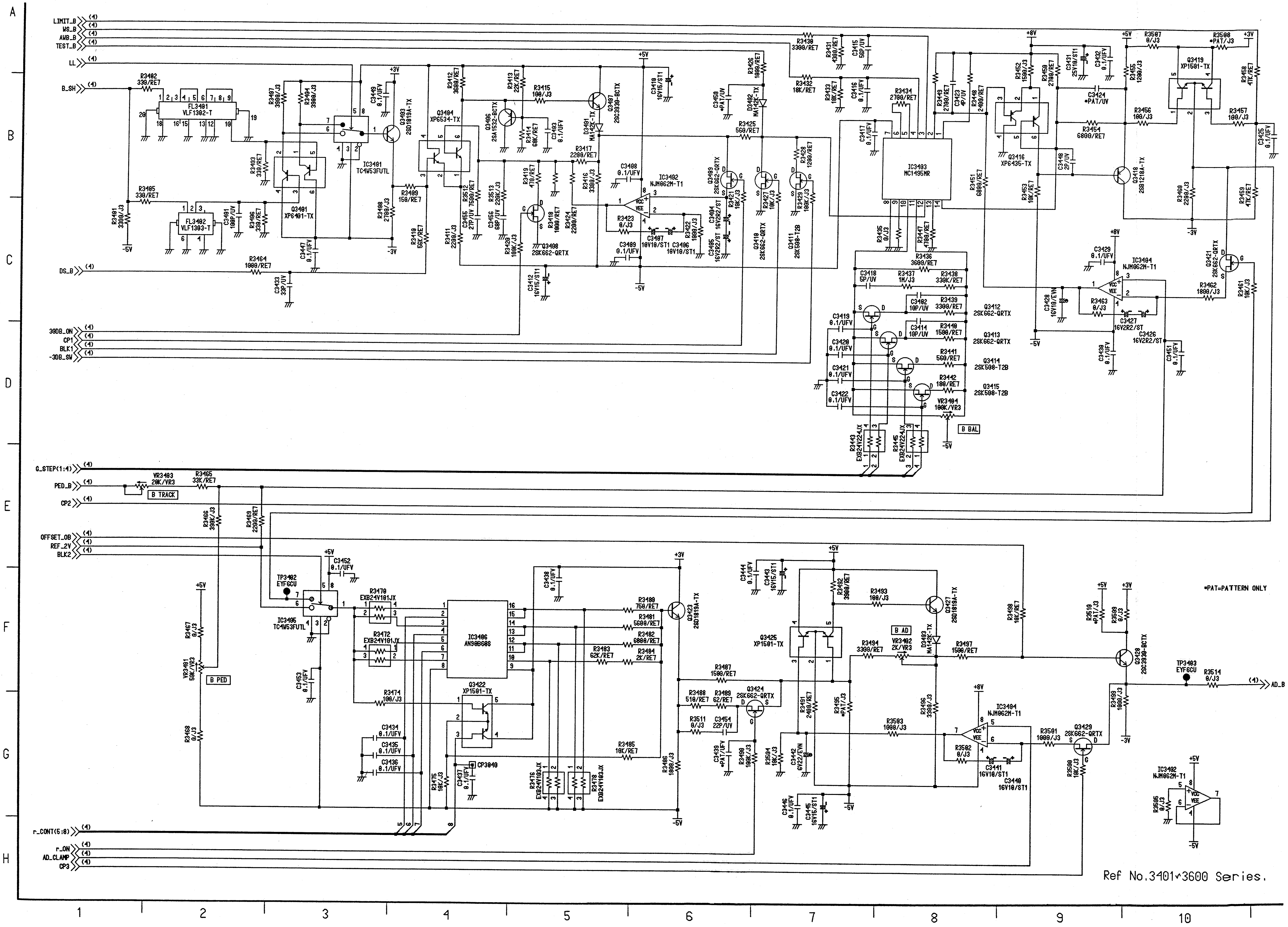
REF	NTSC	PAL	ON
C10	*PAT/UV	10P/UV	10P/UV
C11	*PAT/UV	*PAT/UV	56P/UV
C12	*PAT/UV	*PAT/UV	56P/UV
C17	470P/UV	68P/UV	470P/UV
C2	*PAT/UV	*PAT/UV	56P/UV
C25	*PAT/EVV	*PAT/EVV	16V10/EVV
C26	*PAT/EVV	*PAT/EVV	16V10/EVV
C27	*PAT/EVV	*PAT/EVV	16V10/EVV
C5	68P/UV	82P/UV	68P/UV
C7	*PAT/UV	*PAT/UV	33P/UV
C74	*PAT/UV	*PAT/UV	33P/UV
C75	*PAT/UV	*PAT/UV	33P/UV
C76	*PAT/UV	*PAT/UV	33P/UV
C8	*PAT/UV	*PAT/UV	33P/UV
C9	33P/UV	39P/UV	33P/UV
L2	*PAT/LA	*PAT/LA	33U/LA
R10	*PAT/J3	*PAT/J3	0/J3
R11	*PAT/J3	*PAT/J3	0/J3
R111	*PAT/J3	*PAT/J3	0/J3
R113	3300/RE7	470K/J3	3300/RE7
R118	*PAT/J3	*PAT/J3	0/J3
R119	*PAT/J3	*PAT/J3	0/J3
R120	*PAT/J3	*PAT/J3	0/J3
R129	*PAT/RE7	*PAT/RE7	22K/RE7
R130	*PAT/RE7	*PAT/RE7	22K/RE7
R131	*PAT/J3	*PAT/J3	0/J3
R136	*PAT/J3	*PAT/J3	0/J3
R137	*PAT/J3	*PAT/J3	0/J3
R14	*PAT/J3	*PAT/J3	0/J3
R147	*PAT/J6	*PAT/J6	0/J6
R148	*PAT/J6	*PAT/J6	0/J6
R15	*PAT/J3	*PAT/J3	0/J3
R165	*PAT/J3	0/J3	0/J3
R166	*PAT/J3	*PAT/J3	0/J3
R175	*PAT/J3	*PAT/J3	0/J3
R177	*PAT/J3	*PAT/J3	0/J3
R180	*PAT/RE7	470/RE7	470/RE7
R181	*PAT/RE7	*PAT/RE7	270/RE7
R182	*PAT/RE7	1800/RE7	1800/RE7
R183	*PAT/RE7	*PAT/RE7	270/RE7
R184	*PAT/RE7	*PAT/RE7	270/RE7
R185	*PAT/RE7	*PAT/RE7	510/RE7
R187	*PAT/RE7	*PAT/RE7	22K/RE7

REVERSE SIDE
PULSE 2/4

PULSE (4/4) COMPARISON CHART 2 BETWEEN MODELS

REF	NTSC	PAL	ON
R188	22K/RE7	10K/RE7	22K/RE7
R191	*PAT/J6	*PAT/J6	0/J6
R24	*PAT/J3	*PAT/J3	0/J3
R30	0/J3	100/RE7	0/J3
R31	0/J3	100/RE7	0/J3
R32	0/J3	100/RE7	0/J3
R41	0/J3	*PAT/J3	0/J3
R42	*PAT/J3	0/J3	0/J3
R60	*PAT/RE7	*PAT/RE7	15K/RE7
R61	*PAT/RE7	*PAT/RE7	3300/RE7
R62	*PAT/RE7	*PAT/RE7	3300/RE7
R63	*PAT/RE7	*PAT/RE7	15K/RE7
R64	*PAT/RE7	*PAT/RE7	15K/RE7
R65	*PAT/RE7	*PAT/RE7	3300/RE7
VR10	*PAT/VR8	*PAT/VR8	20K/VR8
VR11	*PAT/VR8	*PAT/VR8	20K/VR8
VR12	*PAT/VR8	*PAT/VR8	20K/VR8
X1	VSX0686	VSX0687	VSX0686

PRE PROCESS (3/4) SCHEMATIC DIAGRAM



A
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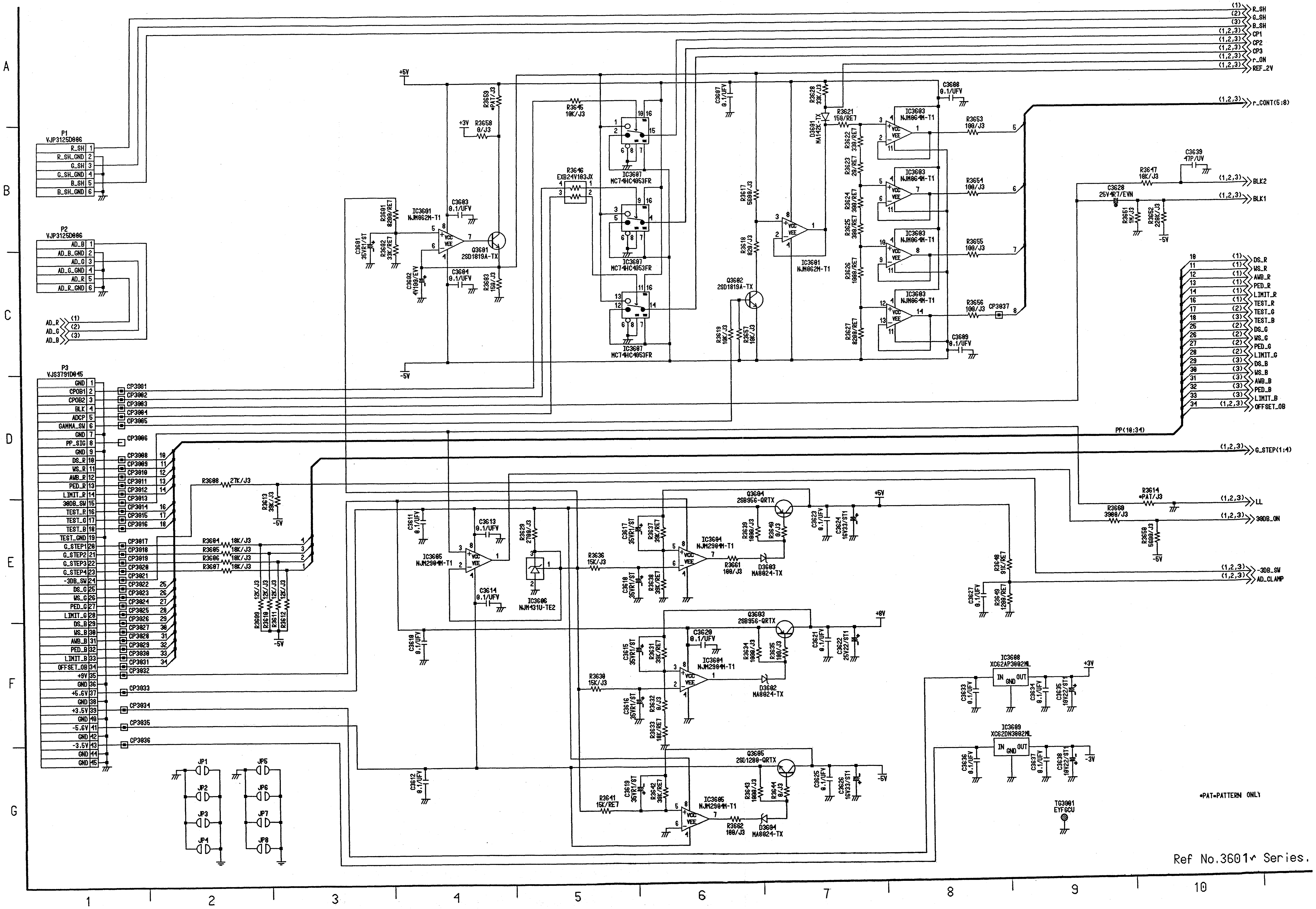
LIMIT_B
WS_B
AWB_B
TEST_B
LL
B_SH
DS_B
30DB_ON
CP1
BLK1
-30DB_SW
G_STEP(1:4)
PED_B
CP2
OFFSET_OB
REF_2V
BLK2
r_CONT(5:8)
r_ON
AD_CLAMP
CP3
AD_B
FL3401
VLF1302-T
FL3402
VLF1303-T
IC3401
TC4W53FUTL
IC3402
NJM062M-T1
IC3403
MC1495MR
IC3404
NJM062M-T1
IC3405
TC4W53FUTL
IC3406
AN90B68S
Q3401
XP6401-TX
Q3403
2SD1819A-TX
Q3404
XP6534-TX
Q3406
2SA1532-BCTX
Q3407
2SC3930-BCTX
Q3408
2SK662-QRTX
Q3409
2SK662-QRTX
Q3410
2SK662-QRTX
Q3411
2SK508-T2B
Q3412
2SK662-QRTX
Q3413
2SK662-QRTX
Q3414
2SK508-T2B
Q3415
2SK508-T2B
Q3416
XP6435-TX
Q3418
2SB1218A-TX
Q3419
XP1501-TX
Q3421
2SK662-QRTX
Q3422
XP1501-TX
Q3423
2SD1819A-TX
Q3424
2SK662-QRTX
Q3425
XP1501-TX
Q3427
2SD1819A-TX
Q3428
2SC3930-BCTX
Q3429
2SK662-QRTX
D3401
MA142K-TX
D3402
MA142K-TX
D3403
MA142K-TX
VR3401
50K/VR3
VR3402
2K/VR3
VR3403
20K/VR3
VR3404
100K/VR3
B TRACK
B PED
B BAL
B AD
TP3402
EYF8CU
TP3403
EYF8CU
CP3040
+5V
+3V
+8V
-3V
-5V
*PAT=PATTERN ONLY
Ref No.3401~3600 Series.

PRE PROCESS (4/4) SCHEMATIC DIAGRAM


A
B
C
D
E
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G
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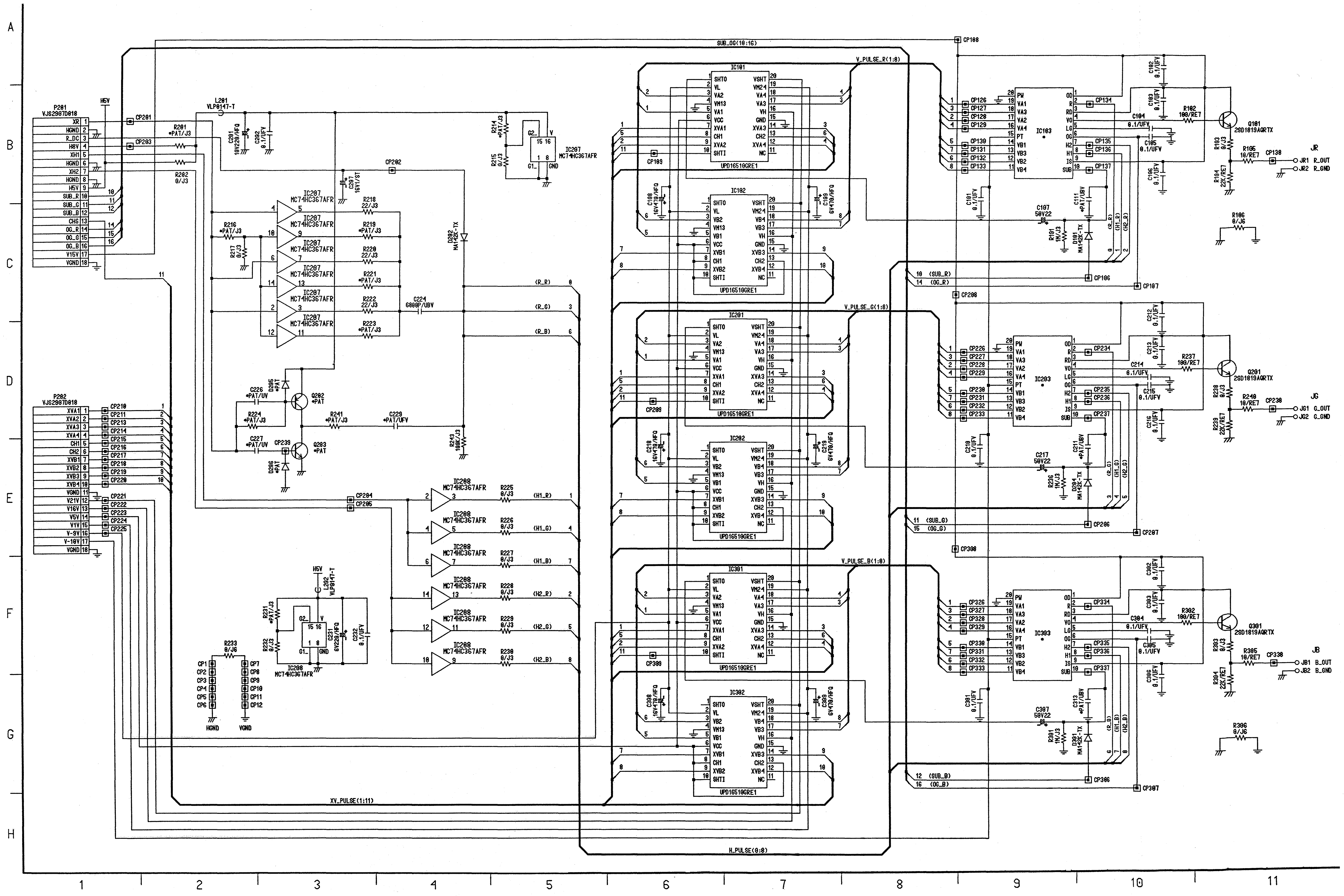
8
9
10
P1
VJP3125D006
R_SH
R_SH_GND
G_SH
G_SH_GND
B_SH
B_SH_GND
P2
VJP3125D006
AD_B
AD_B_GND
AD_G
AD_G_GND
AD_R
AD_R_GND
AD_R (1)
AD_G (2)
AD_B (3)
P3
VJS3791D045
GND
CPOB1
CPOB2
BLK
ADCP
GAMMA_SW
GND
PP_SIG
GND
DS_R
WS_R
AWB_R
PED_R
LIMIT_R
30DB_SW
TEST_R
TEST_G
TEST_B
TEST_GND
G_STEP1
G_STEP2
G_STEP3
G_STEP4
-3DB_SW
DS_G
WS_G
PED_G
LIMIT_G
DS_B
WS_B
AWB_B
PED_B
LIMIT_B
OFFSET_OB
+9V
GND
+5.6V
GND
+3.5V
GND
-5.6V
GND
-3.5V
GND
GND
CP3001
CP3002
CP3003
CP3004
CP3005
CP3006
CP3008
CP3009
CP3010
CP3011
CP3012
CP3013
CP3014
CP3015
CP3016
CP3017
CP3018
CP3019
CP3020
CP3021
CP3022
CP3023
CP3024
CP3025
CP3026
CP3027
CP3028
CP3029
CP3030
CP3031
CP3032
CP3033
CP3034
CP3035
CP3036
JP1
JP2
JP3
JP4
JP5
JP6
JP7
JP8
(1) R_SH
(2) G_SH
(3) B_SH
(1,2,3) CP1
(1,2,3) CP2
(1,2,3) CP3
(1,2,3) r_ON
(1,2,3) REF_2V
(1,2,3) r_CONT(5:8)
(1,2,3) BLK2
(1,2,3) BLK1
(1) DS_R
(1) WS_R
(1) AWB_R
(1) PED_R
(1) LIMIT_R
(1) TEST_R
(2) TEST_G
(3) TEST_B
(2) DS_G
(2) WS_G
(2) PED_G
(2) LIMIT_G
(3) DS_B
(3) WS_B
(3) AWB_B
(3) PED_B
(3) LIMIT_B
(1,2,3) OFFSET_OB
PP(10:34)
(1,2,3) G_STEP(1:4)
(1,2,3) LL
(1,2,3) 30DB_ON
(1,2,3) -3DB_SW
(1,2,3) AD_CLAMP
+5V
-5V
+3V
+8V
-3V
IC3601
NJM062M-T1
IC3607
MC74HC4053FR
IC3603
NJM064M-T1
IC3604
NJM2904M-T1
IC3605
NJM2904M-T1
IC3606
NJM431U-TE2
IC3608
XC62AP3002ML
IC3609
XC62DN3002ML
Q3601
2SD1819A-TX
Q3602
2SD1819A-TX
Q3603
2SB956-QRTX
Q3604
2SB956-QRTX
Q3605
2SD1280-QRTX
D3601
MA142K-TX
D3602
MA8024-TX
D3603
MA8024-TX
D3604
MA8024-TX
R3646
EXB24V103JX
R3645
10K/J3
R3659
*PAT/J3
R3658
0/J3
R3601
8200/RET
R3602
33K/RET
R3603
150/J3
R3617
5600/J3
R3618
820/J3
R3619
10K/J3
R3657
10K/J3
R3628
33K/J3
R3621
150/RE7
R3622
330/RE7
R3623
20/RE7
R3624
300/RE7
R3625
300/RE7
R3626
1000/RE7
R3627
8200/RE7
R3653
100/J3
R3654
100/J3
R3655
100/J3
R3656
100/J3
CP3037
R3647
10K/J3
R3651
1K/J3
R3652
220K/J3
R3608
27K/J3
R3613
36K/J3
R3604
18K/J3
R3605
18K/J3
R3606
18K/J3
R3607
18K/J3
R3609
12K/J3
R3610
12K/J3
R3611
12K/J3
R3612
12K/J3
R3629
2700/J3
R3636
15K/J3
R3637
39K/RE7
R3638
39K/RE7
R3639
1000/J3
R3640
0/J3
R3661
100/J3
R3630
15K/J3
R3631
39K/RE7
R3632
0/J3
R3633
18K/RE7
R3634
1000/J3
R3635
100/J3
R3641
15K/RE7
R3642
39K/RE7
R3643
1000/J3
R3644
0/J3
R3662
100/J3
R3614
*PAT/J3
R3660
3900/J3
R3650
5600/J3
R3648
91K/RE7
R3649
1200/RE7
C3601
35VR1/ST
C3602
4V100/EVV
C3603
0.1/UFV
C3604
0.1/UFV
C3607
0.1/UFV
C3608
0.1/UFV
C3609
0.1/UFV
C3628
25V4R7/EVN
C3639
47P/UV
C3611
0.1/UFV
C3613
0.1/UFV
C3614
0.1/UFV
C3617
35VR1/ST
C3618
35VR1/ST
C3623
0.1/UFV
C3624
16V33/ST1
C3610
0.1/UFV
C3620
0.1/UFV
C3615
35VR1/ST
C3616
35VR1/ST
C3621
0.1/UFV
C3622
25V22/ST1
C3612
0.1/UFV
C3619
35VR1/ST
C3625
0.1/UFV
C3626
16V33/ST1
C3627
0.1/UFV
C3633
0.1/UFV
C3634
0.1/UFV
C3635
10V22/ST1
C3636
0.1/UFV
C3637
0.1/UFV
C3638
10V22/ST1
IN
OUT
GND
VCC
VEE
TG3001
EYFGCU
*PAT=PATTERN ONLY

Ref No.3601~ Series.

REVERSE SIDE

PRE PROCESS 3/4

CCD (1/2) SCHEMATIC DIAGRAM



A
B
C
D
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F
G
H
1
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3
4
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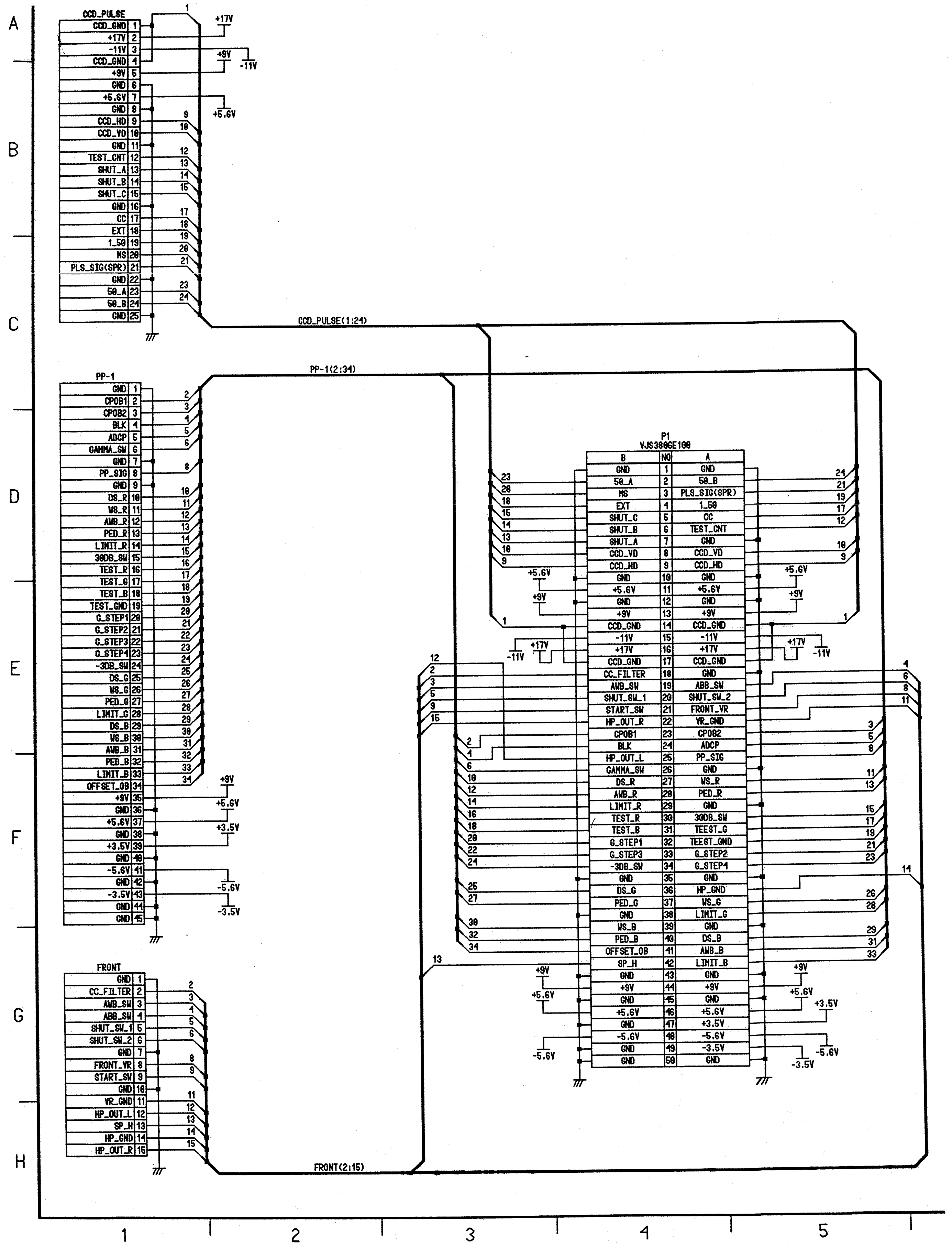
7
8
9
10
11
P201
VJS2907D018
XR
HGND
R_DC
H8V
XH1
HGND
XH2
HGND
H5V
SUB_R
SUB_G
SUB_B
CHS
OG_R
OG_G
OG_B
V15V
VGND
H5V
CP201
CP203
R201
R202
L201
VLP0147-T
C201
C202
R214
R215
IC207
MC74HC367AFR
CP202
C207
R216
R217
R218
R219
R220
R221
R222
R223
C224
D202
(R_R)
(R_G)
(R_B)
D205
C226
Q202
R224
C227
CP239
Q203
D206
R241
C229
R243
P202
VJS2907D018
XVA1
XVA2
XVA3
XVA4
CH1
CH2
XVB1
XVB2
XVB3
XVB4
VGND
V21V
V16V
V5V
V1V
V-9V
V-10V
CP210
CP211
CP213
CP214
CP215
CP216
CP217
CP218
CP219
CP220
CP221
CP222
CP223
CP224
CP225
CP204
CP205
IC208
MC74HC367AFR
R225
R226
R227
R228
R229
R230
(H1_R)
(H1_G)
(H1_B)
(H2_R)
(H2_G)
(H2_B)
L202
VLP0147-T
R231
R232
C231
C232
R233
CP1
CP2
CP3
CP4
CP5
CP6
CP7
CP8
CP9
CP10
CP11
CP12
HGND
VGND
SUB_OG(10:16)
V_PULSE_R(1:8)
V_PULSE_G(1:8)
V_PULSE_B(1:8)
XV_PULSE(1:11)
H_PULSE(0:8)
IC101
IC102
IC201
IC202
IC301
IC302
UPD16510GRE1
SHTO
VL
VA2
VH13
VA1
VCC
XVA1
CH1
XVA2
SHTI
VSHT
VH24
VA4
VA3
VH
GND
XVA3
CH2
XVA4
NC
VB2
VB1
XVB1
XVB2
VB4
VB3
XVB3
XVB4
CP109
CP209
CP309
C108
C109
C208
C209
C308
C309
CP108
CP208
CP308
IC103
IC203
IC303
PW
PT
OD
RD
VO
LG
OG
H2
H1
IS
SUB
CP126
CP127
CP128
CP129
CP130
CP131
CP132
CP133
CP134
CP135
CP136
CP137
CP226
CP227
CP228
CP229
CP230
CP231
CP232
CP233
CP234
CP235
CP236
CP237
CP326
CP327
CP328
CP329
CP330
CP331
CP332
CP333
CP334
CP335
CP336
CP337
C101
C102
C103
C104
C105
C106
C107
C111
R101
D101
R102
R103
R104
R105
R106
Q101
2SD1819AQRTX
CP138
JR
JR1 R_OUT
JR2 R_GND
CP106
CP107
(SUB_R)
(OG_R)
C201
C212
C213
C214
C215
C216
C217
C211
R236
D204
R237
R238
R239
R240
Q201
2SD1819AQRTX
CP238
JG
JG1 G_OUT
JG2 G_GND
CP206
CP207
(SUB_G)
(OG_G)
C301
C302
C303
C304
C305
C306
C307
C313
R301
D301
R302
R303
R304
R305
R306
Q301
2SD1819AQRTX
CP338
JB
JB1 B_OUT
JB2 B_GND
CP306
CP307
(SUB_B)
(OG_B)

CCD (2/2) COMPARISON CHART BETWEEN MODELS

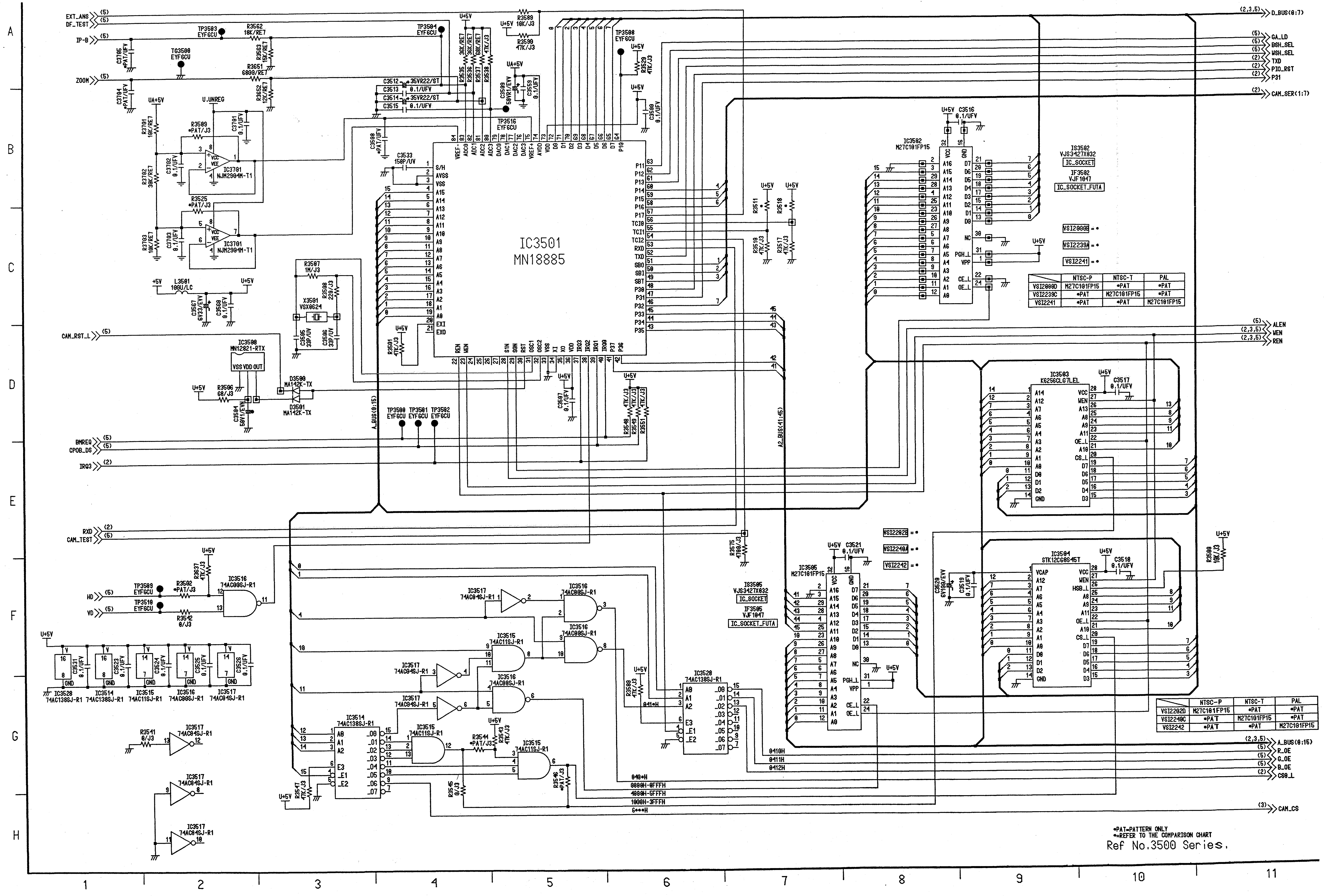
REF	NTSC	PAL	ON
C111	*PAT/UBV	*PAT/UBV	6800P/UBV
C211	*PAT/UBV	*PAT/UBV	6800P/UBV
C226	*PAT/UV	*PAT/UV	220P/UV
C227	*PAT/UV	*PAT/UV	180P/UV
C229	*PAT/UFV	*PAT/UFV	0. 1/UFV
C313	*PAT/UBV	*PAT/UBV	6800P/UBV
D205	*PAT	*PAT	MA141K-TX
D206	*PAT	*PAT	MA141K-TX
IC103	MW3753MAE	MW3763MAE	MW3753MAE
IC203	MW3753MAE	MW3763MAE	MW3753MAE
IC303	MW3753MAE	MW3763MAE	MW3753MAE
Q202	*PAT	*PAT	2SB1218AQRTX
Q203	*PAT	*PAT	2SD1819AQRTX
R201	*PAT/J3	*PAT/J3	0/J3
R214	*PAT/J3	*PAT/J3	0/J3
R216	*PAT/J3	*PAT/J3	0/J3
R219	*PAT/J3	*PAT/J3	22/J3
R221	*PAT/J3	*PAT/J3	22/J3
R223	*PAT/J3	*PAT/J3	22/J3
R224	*PAT/J3	*PAT/J3	1M/J3
R231	*PAT/J3	*PAT/J3	0/J3
R241	*PAT/J3	*PAT/J3	22/J3

REVERSE SIDE
CCD 1/2

CAMERA FLEX SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
1
2
3
4
5
CCD_PULSE
CCD_PULSE(1:24)
PP-1
PP-1(2:34)
FRONT
FRONT(2:15)
P1
VJS3806E100
+17V
-11V
+9V
+5.6V
+3.5V
-5.6V
-3.5V

CAMERA SYSCON (1/5) SCHEMATIC DIAGRAM


EXT_ANS
DF_TEST
IP-B
ZOOM
CAM_RST_L
BMREQ
CPOB_DS
IRQ3
RXD
CAM_TEST
HD
VD
IC3501
MN18885
IC3701
NJM2904M-T1
IC3508
MN12821-RTX
X3501
VSX0624
D3500
MA142K-TX
D3501
MA142K-TX
L3501
100U/LC
IC3502
M27C101FP15
IS3502
VJS3427X032
IC_SOCKET
IF3502
VJF1047
IC_SOCKET_FUTA
IC3503
K6256CLG7LEL
IC3504
STK12C68S45T
IC3505
M27C101FP15
IS3505
VJS3427X032
IF3505
VJF1047
IC3514
74AC138SJ-R1
IC3515
74AC11SJ-R1
IC3516
74AC08SJ-R1
IC3517
74AC04SJ-R1
IC3528
74AC138SJ-R1
TP3503
TP3504
TP3508
TP3509
TP3510
TP3516
TP3500
TP3501
TP3502
EYF6CU
U+5V
UA+5V
U.UNREG
+5V
A_BUS(0:15)
A2_BUS(41:45)
D_BUS(0:7)
GA_LD
BSH_SEL
WSH_SEL
TXD
PIO_RST
P31
CAM_SER(1:7)
ALEN
WEN
REN
R_OE
G_OE
B_OE
CS0_L
CAM_CS
0410H
0411H
0412H
040*H
0000H-0FFFH
4000H-5FFFH
1000H-3FFFH
6***H
VSI2000B = *
VSI2239A = *
VSI2241 = *
VSI2202B = *
VSI2240A = *
VSI2242 = *
A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11

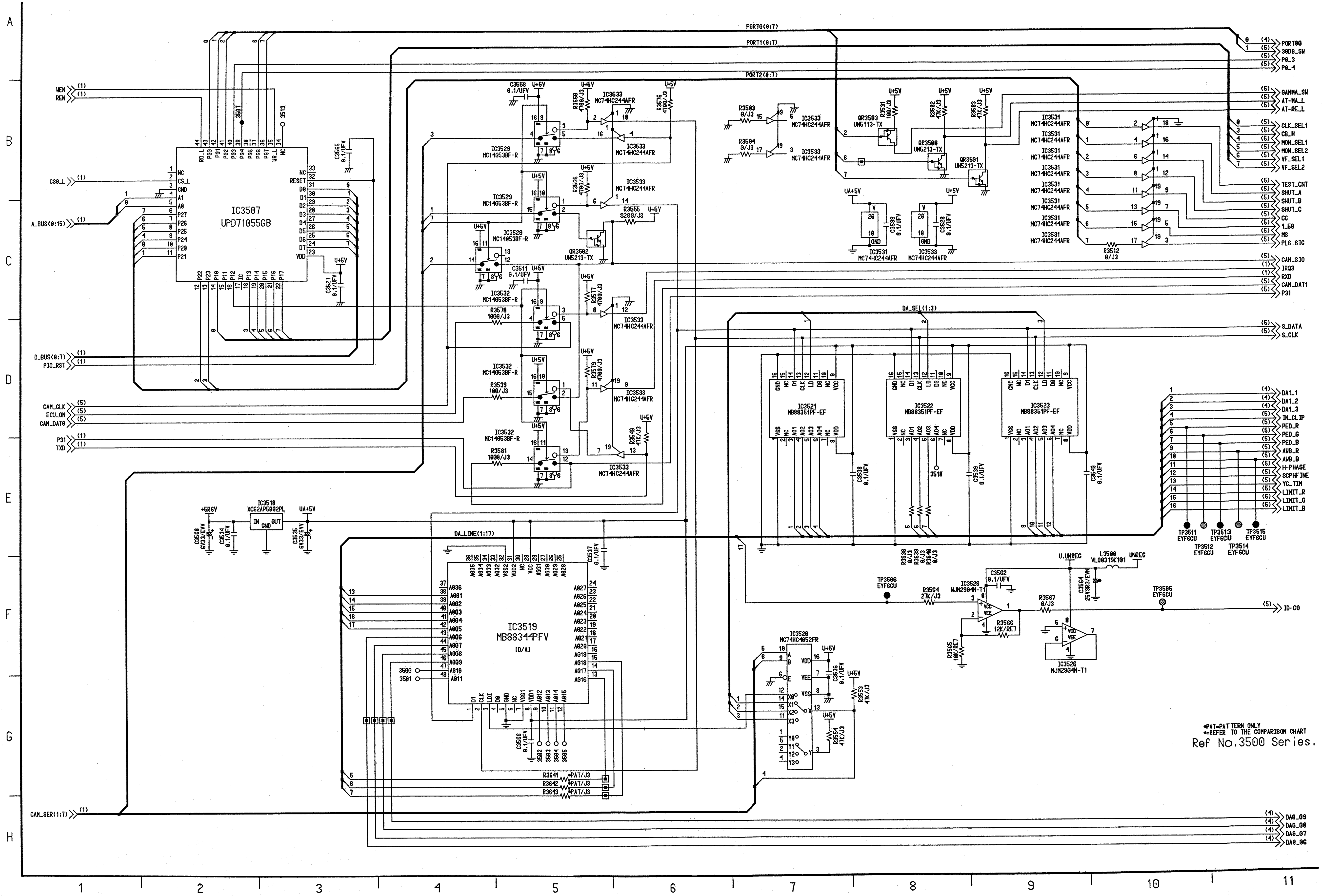
	NTSC-P	NTSC-T	PAL
VSI2000D	M27C101FP15	*PAT	*PAT
VSI2239C	*PAT	M27C101FP15	*PAT
VSI2241	*PAT	*PAT	M27C101FP15

	NTSC-P	NTSC-T	PAL
VSI2202D	M27C101FP15	*PAT	*PAT
VSI2240C	*PAT	M27C101FP15	*PAT
VSI2242	*PAT	*PAT	M27C101FP15

*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART

Ref No.3500 Series.

CAMERA SYSCON (2/5) SCHEMATIC DIAGRAM


IC3507
UPD71055GB
IC3519
MB88344PFV
[D/A]
IC3521
MB88351PF-EF
IC3522
MB88351PF-EF
IC3523
MB88351PF-EF
IC3520
MC74HC4052FR
IC3518
XC62AP5002PL
IC3526
NJM2904M-T1
IC3529
MC14053BF-R
IC3532
MC14053BF-R
IC3533
MC74HC244AFR
IC3531
MC74HC244AFR
QR3502
UN5213-TX
QR3503
UN5113-TX
QR3500
UN5213-TX
QR3501
UN5213-TX
L3500
VLQ0319K101
PORT0(0:7)
PORT1(0:7)
PORT2(0:7)
DA_SEL(1:3)
DA_LINE(1:17)
WEN
REN
CS0_L
A_BUS(0:15)
D_BUS(0:7)
PIO_RST
CAM_CLK
ECU_ON
CAM_DAT0
P31
TXD
CAM_SER(1:7)
PORT00
30DB_SW
P0_3
P0_4
GAMMA_SW
AT-MA_L
AT-RE_L
CLK_SEL1
CB_H
MON_SEL1
MON_SEL2
VF_SEL1
VF_SEL2
TEST_CNT
SHUT_A
SHUT_B
SHUT_C
CC
1_50
MS
PLS_SIG
CAM_SIO
IRQ3
RXD
CAM_DAT1
P31
S_DATA
S_CLK
DA1_1
DA1_2
DA1_3
IN_CLIP
PED_R
PED_G
PED_B
AWB_R
AWB_B
H-PHASE
SCPHFINE
YC_TIM
LIMIT_R
LIMIT_G
LIMIT_B
ID-CO
DA0_09
DA0_08
DA0_07
DA0_06
TP3511
TP3512
TP3513
TP3514
TP3515
TP3505
TP3506
EYF6CU
U.UNREG
UNREG
+5R6V
UA+5V
U+5V
*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART
Ref No.3500 Series.
A
B
C
D
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G
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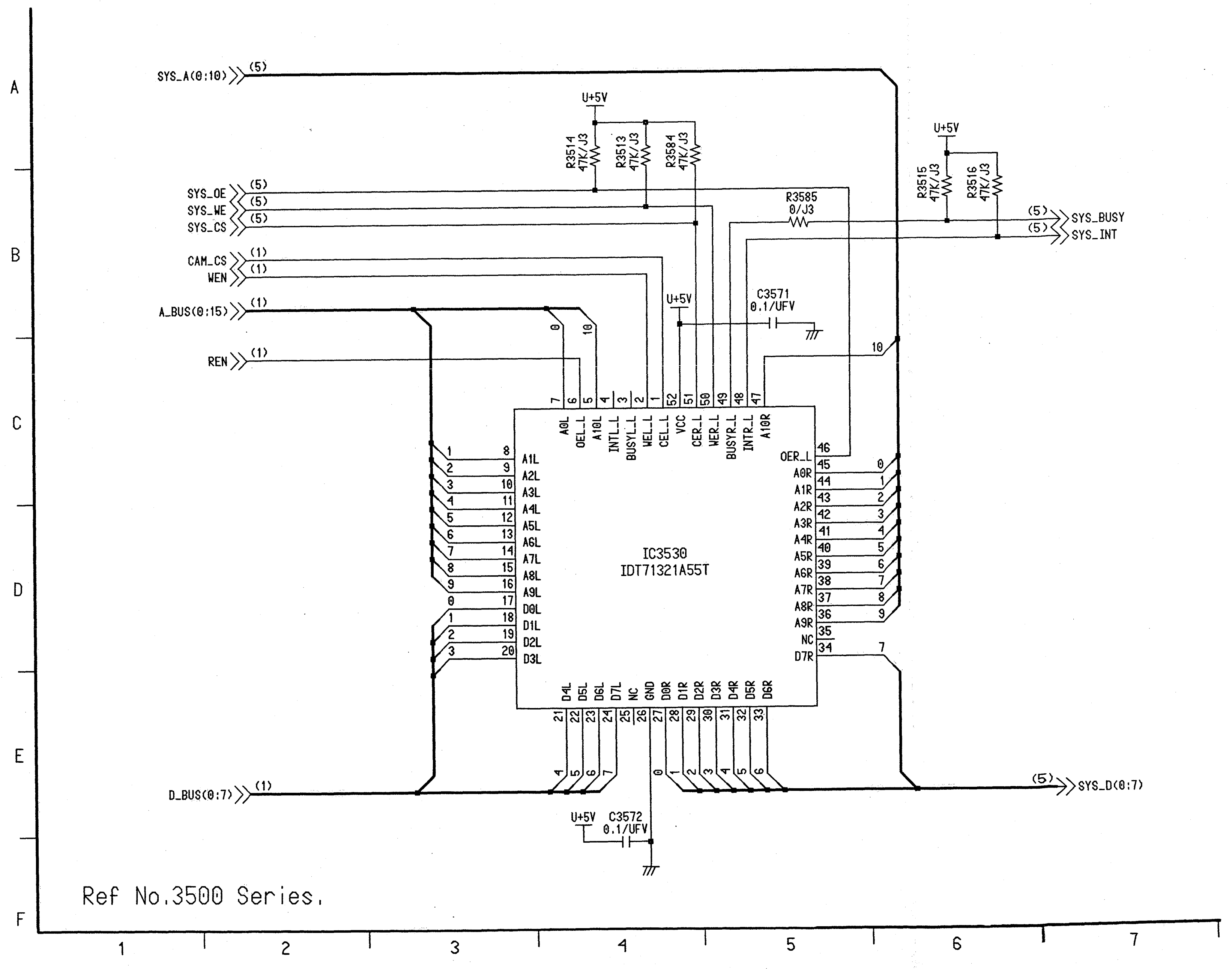
CAMERA SYSCON (3/5) SCHEMATIC DIAGRAM

REF	PAL	NTSC-P	NTSC-T	ON
C3508	*PAT/UFV	*PAT/UFV	*PAT/UFV	0. 1/UFV
C3704	*PAT/UFV	*PAT/UFV	*PAT/UFV	0. 1/UFV
C3705	*PAT/UFV	*PAT/UFV	*PAT/UFV	0. 1/UFV
R3502	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3509	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3511	10K/J3	*PAT/J3	*PAT/J3	10K/J3
R3518	*PAT/J3	*PAT/J3	10K/J3	10K/J3
R3525	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3544	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3546	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3641	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3642	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3643	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3650	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
VSI2000D	M27C101FP15	*PAT	*PAT	M27C101FP15
VSI2202D	M27C101FP15	*PAT	*PAT	M27C101FP15
VSI2239C	*PAT	M27C101FP15	*PAT	M27C101FP15
VSI2240C	*PAT	M27C101FP15	*PAT	M27C101FP15
VSI2241	*PAT	*PAT	M27C101FP15	M27C101FP15
VSI2242	*PAT	*PAT	M27C101FP15	M27C101FP15


A
B
C
D
E
F
1
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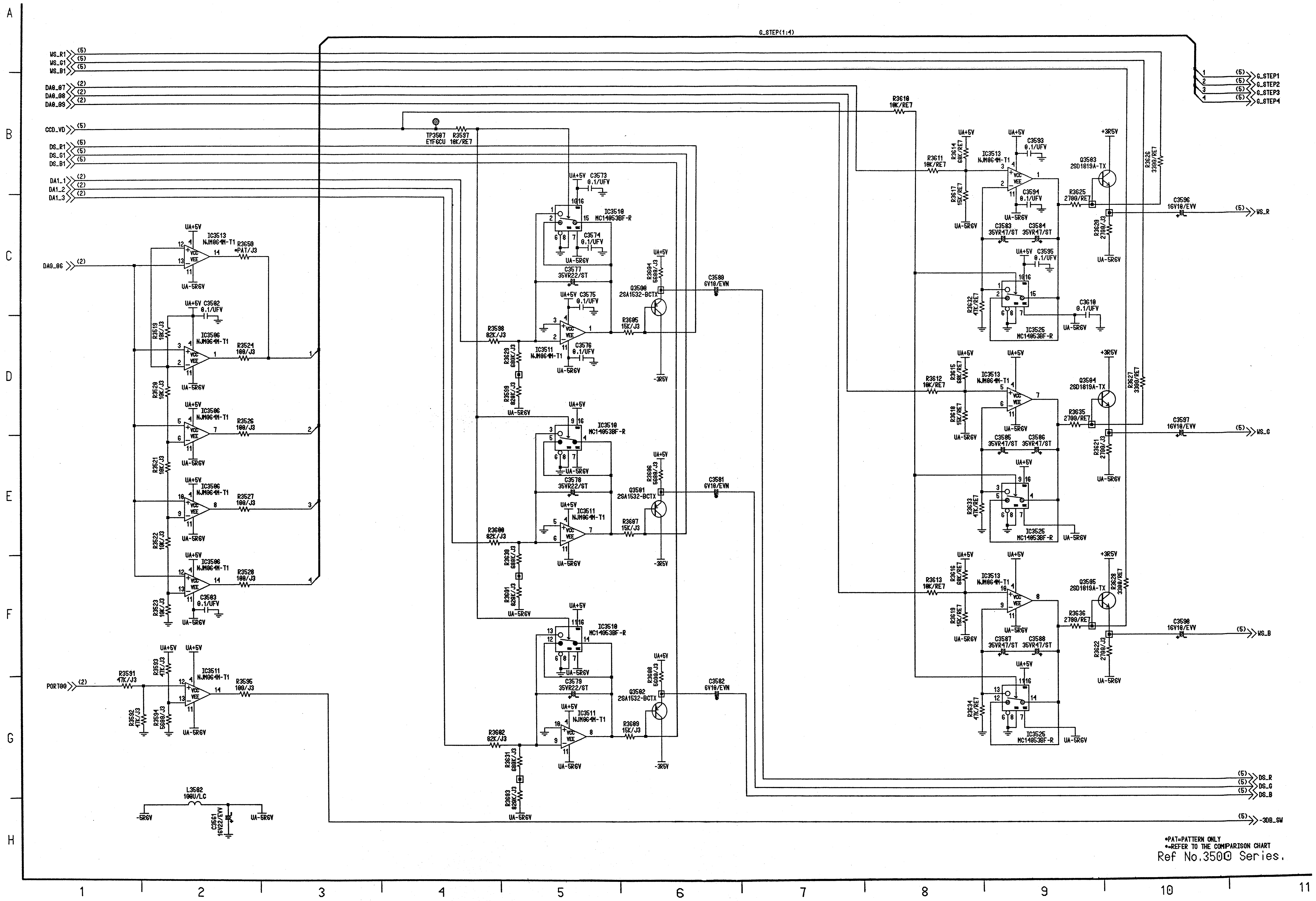
3
4
5
6
7
SYS_A(0:10) (5)
U+5V
R3514 47K/J3
R3513 47K/J3
R3584 47K/J3
R3515 47K/J3
R3516 47K/J3
R3585 0/J3
SYS_OE (5)
SYS_WE (5)
SYS_CS (5)
CAM_CS (1)
WEN (1)
A_BUS(0:15) (1)
REN (1)
C3571 0.1/UFV
(5) SYS_BUSY
(5) SYS_INT
IC3530
IDT71321A55T
A0L
OEL_L
A10L
INTL_L
BUSYL_L
WEL_L
CEL_L
VCC
CER_L
WER_L
BUSYR_L
INTR_L
A10R
A1L
A2L
A3L
A4L
A5L
A6L
A7L
A8L
A9L
D0L
D1L
D2L
D3L
OER_L
A0R
A1R
A2R
A3R
A4R
A5R
A6R
A7R
A8R
A9R
NC
D7R
D4L
D5L
D6L
D7L
NC
GND
D0R
D1R
D2R
D3R
D4R
D5R
D6R
D_BUS(0:7) (1)
(5) SYS_D(0:7)
C3572 0.1/UFV
Ref No.3500 Series.

CAMERA SYSCON (4/5) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
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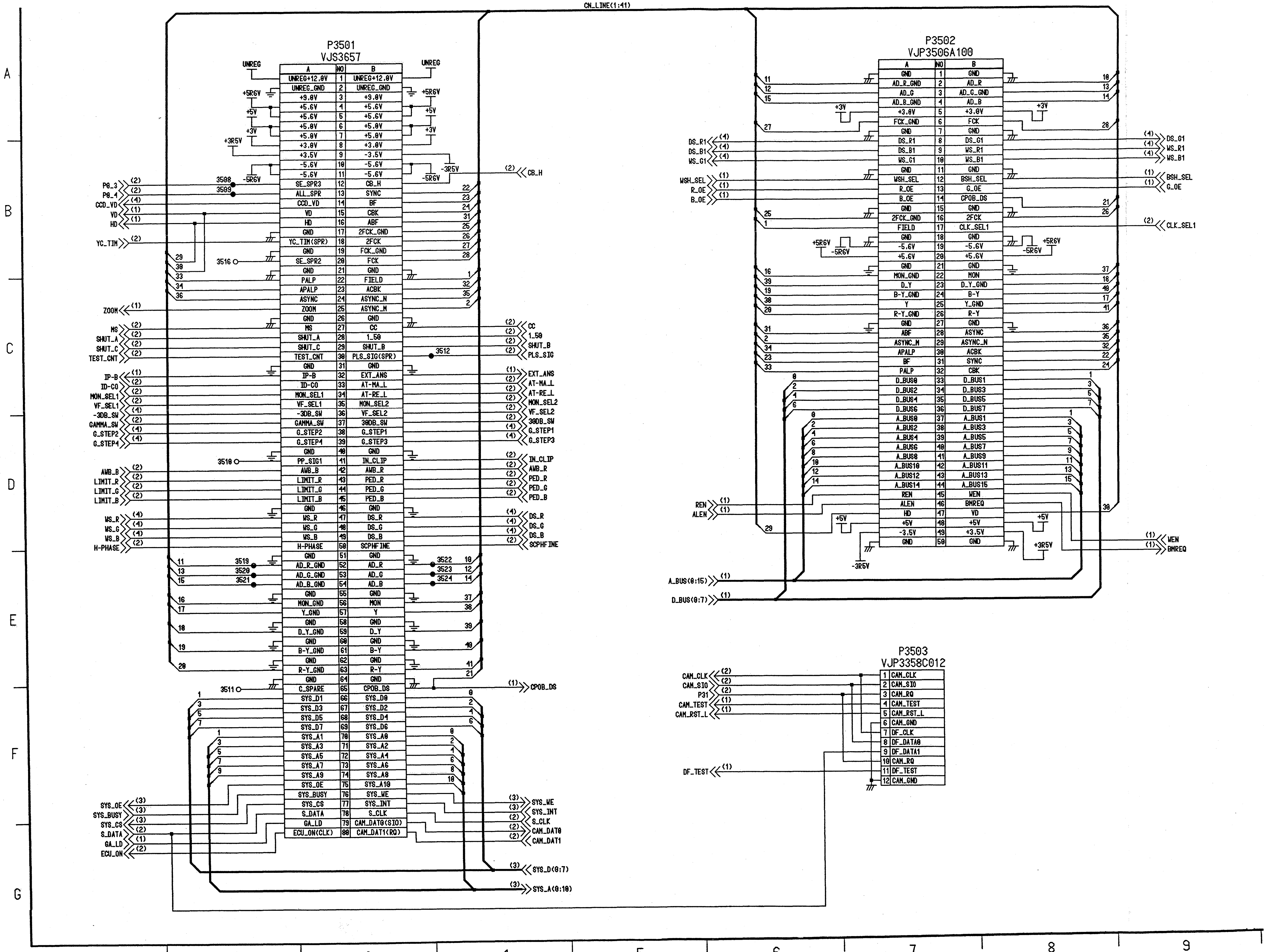
7
8
9
10
11
G_STEP(1:4)
WS_R1 (5)
WS_G1 (5)
WS_B1 (5)
DA0_07 (2)
DA0_08 (2)
DA0_09 (2)
CCD_VD (5)
DS_R1 (5)
DS_G1 (5)
DS_B1 (5)
DA1_1 (2)
DA1_2 (2)
DA1_3 (2)
DA0_06 (2)
PORTG0 (2)
TP3507 EYF6CU
R3597 10K/RE7
IC3513 NJM064M-T1
R3650 *PAT/J3
UA+5V
UA-5R6V
C3502 0.1/UFV
R3519 10K/J3
IC3506 NJM064M-T1
R3524 100/J3
R3520 10K/J3
R3526 100/J3
R3521 10K/J3
R3527 100/J3
R3522 10K/J3
R3528 100/J3
R3523 10K/J3
C3503 0.1/UFV
R3591 47K/J3
R3592 47K/J3
R3593 47K/J3
R3594 5600/J3
IC3511 NJM064M-T1
R3595 100/J3
L3502 100U/LC
-5R6V
C3561 16V22/EVV
C3573 0.1/UFV
IC3510 MC14053BF-R
C3574 0.1/UFV
C3577 35VR22/ST
C3575 0.1/UFV
C3576 0.1/UFV
R3598 82K/J3
R3629 680K/J3
R3599 820K/J3
R3604 5600/J3
Q3500 2SA1532-BCTX
R3605 15K/J3
-3R5V
C3580 6V10/EVN
C3578 35VR22/ST
R3600 82K/J3
R3630 680K/J3
R3601 820K/J3
R3606 5600/J3
Q3501 2SA1532-BCTX
R3607 15K/J3
C3581 6V10/EVN
C3579 35VR22/ST
R3602 82K/J3
R3631 680K/J3
R3603 820K/J3
R3608 5600/J3
Q3502 2SA1532-BCTX
R3609 15K/J3
C3582 6V10/EVN
R3610 10K/RE7
R3611 10K/RE7
R3614 68K/RE7
R3617 15K/RE7
C3593 0.1/UFV
C3594 0.1/UFV
C3583 35VR47/ST
C3584 35VR47/ST
C3595 0.1/UFV
R3632 47K/RE7
IC3525 MC14053BF-R
C3610 0.1/UFV
+3R5V
Q3503 2SD1819A-TX
R3625 2700/RE7
R3620 2700/J3
R3626 3300/RE7
C3596 16V10/EVV
(5) WS_R
R3612 10K/RE7
R3615 68K/RE7
R3618 15K/RE7
C3585 35VR47/ST
C3586 35VR47/ST
R3633 47K/RE7
Q3504 2SD1819A-TX
R3635 2700/RE7
R3621 2700/J3
R3627 3300/RE7
C3597 16V10/EVV
(5) WS_G
R3613 10K/RE7
R3616 68K/RE7
R3619 15K/RE7
C3587 35VR47/ST
C3588 35VR47/ST
R3634 47K/RE7
Q3505 2SD1819A-TX
R3636 2700/RE7
R3622 2700/J3
R3628 3300/RE7
C3598 16V10/EVV
(5) WS_B
(5) G_STEP1
(5) G_STEP2
(5) G_STEP3
(5) G_STEP4
(5) DS_R
(5) DS_G
(5) DS_B
(5) -3DB_SW

*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART
Ref No.3500 Series.

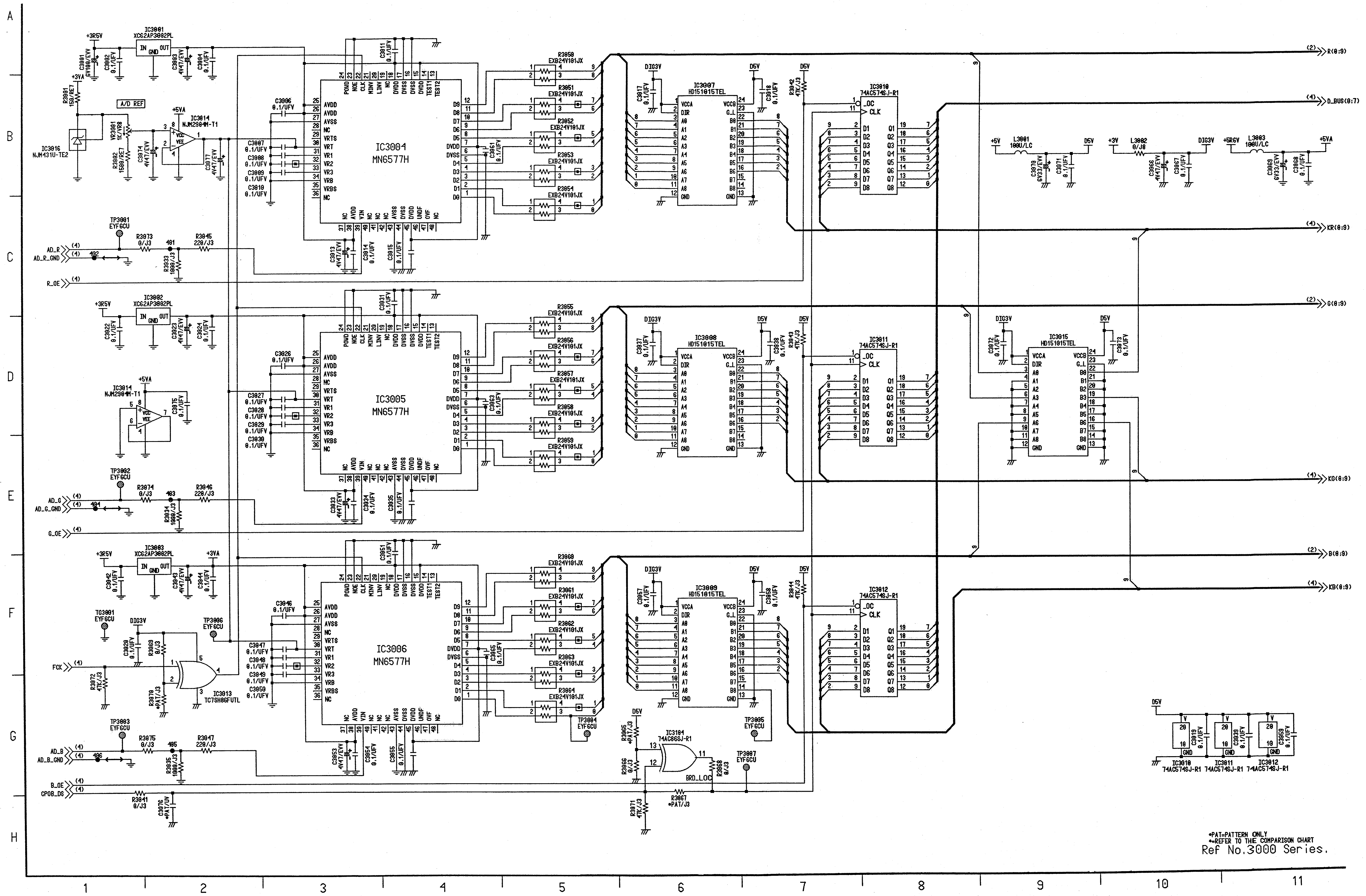
REVERSE SIDE

CAMERA SYSCON 3/5

CAMERA SYSCON (5/5) SCHEMATIC DIAGRAM


CN_LINE(1:41)
P3501
VJS3657
A
NO
B
UNREG
+5R6V
+5V
+3V
+3R5V
-5R6V
-3R5V
UNREG+12.0V
UNREG_GND
+9.0V
+5.6V
+5.0V
+3.0V
+3.5V
-3.5V
-5.6V
SE_SPR3
CB_H
ALL_SPR
SYNC
CCD_VD
BF
VD
CBK
HD
ABF
GND
2FCK_GND
YC_TIM(SPR)
2FCK
FCK_GND
SE_SPR2
FCK
PALP
FIELD
APALP
ACBK
ASYNC
ASYNC_N
ZOOM
MS
CC
SHUT_A
1_50
SHUT_C
SHUT_B
TEST_CNT
PLS_SIG(SPR)
IP-B
EXT_ANS
ID-CO
AT-MA_L
MON_SEL1
AT-RE_L
VF_SEL1
MON_SEL2
-3DB_SW
VF_SEL2
GAMMA_SW
30DB_SW
G_STEP2
G_STEP1
G_STEP4
G_STEP3
PP_SIG1
IN_CLIP
AWB_B
AWB_R
LIMIT_R
PED_R
LIMIT_G
PED_G
LIMIT_B
PED_B
WS_R
DS_R
WS_G
DS_G
WS_B
DS_B
H-PHASE
SCPHFINE
AD_R_GND
AD_R
AD_G_GND
AD_G
AD_B_GND
AD_B
MON_GND
MON
Y_GND
Y
D_Y_GND
D_Y
B-Y_GND
B-Y
R-Y_GND
R-Y
C_SPARE
CPOB_DS
SYS_D1
SYS_D0
SYS_D3
SYS_D2
SYS_D5
SYS_D4
SYS_D7
SYS_D6
SYS_A1
SYS_A0
SYS_A3
SYS_A2
SYS_A5
SYS_A4
SYS_A7
SYS_A6
SYS_A9
SYS_A8
SYS_OE
SYS_A10
SYS_BUSY
SYS_WE
SYS_CS
SYS_INT
S_DATA
S_CLK
GA_LD
CAM_DAT0(SIO)
ECU_ON(CLK)
CAM_DAT1(RQ)
3508
3509
3510
3511
3512
3516
3519
3520
3521
3522
3523
3524
PB_3
PB_4
CCD_VD
VD
HD
YC_TIM
ZOOM
MS
SHUT_A
SHUT_C
TEST_CNT
IP-B
ID-CO
MON_SEL1
VF_SEL1
-3DB_SW
GAMMA_SW
G_STEP2
G_STEP4
AWB_B
LIMIT_R
LIMIT_G
LIMIT_B
WS_R
WS_G
WS_B
H-PHASE
CB_H
CC
1_50
SHUT_B
PLS_SIG
EXT_ANS
AT-MA_L
AT-RE_L
MON_SEL2
VF_SEL2
30DB_SW
G_STEP1
G_STEP3
IN_CLIP
AWB_R
PED_R
PED_G
PED_B
DS_R
DS_G
DS_B
SCPHFINE
CPOB_DS
SYS_OE
SYS_BUSY
SYS_CS
S_DATA
GA_LD
ECU_ON
SYS_WE
SYS_INT
S_CLK
CAM_DAT0
CAM_DAT1
SYS_D(0:7)
SYS_A(0:10)
P3502
VJP3506A100
AD_R_GND
AD_R
AD_G
AD_G_GND
AD_B_GND
AD_B
+3.0V
FCK_GND
FCK
DS_R1
DS_G1
DS_B1
WS_R1
WS_G1
WS_B1
WSH_SEL
BSH_SEL
R_OE
G_OE
B_OE
CPOB_DS
2FCK_GND
2FCK
FIELD
CLK_SEL1
-5.6V
+5.6V
MON_GND
MON
D_Y
D_Y_GND
B-Y_GND
B-Y
Y
Y_GND
R-Y_GND
R-Y
ABF
ASYNC
ASYNC_N
APALP
ACBK
BF
SYNC
PALP
CBK
D_BUS0
D_BUS1
D_BUS2
D_BUS3
D_BUS4
D_BUS5
D_BUS6
D_BUS7
A_BUS0
A_BUS1
A_BUS2
A_BUS3
A_BUS4
A_BUS5
A_BUS6
A_BUS7
A_BUS8
A_BUS9
A_BUS10
A_BUS11
A_BUS12
A_BUS13
A_BUS14
A_BUS15
REN
WEN
ALEN
BMREQ
+5V
-3.5V
+3.5V
-3R5V
+3R5V
DS_R1
DS_B1
WS_G1
WSH_SEL
R_OE
B_OE
DS_G1
WS_R1
WS_B1
BSH_SEL
G_OE
CLK_SEL1
REN
ALEN
WEN
BMREQ
A_BUS(0:15)
D_BUS(0:7)
P3503
VJP3358C012
CAM_CLK
CAM_SIO
CAM_RQ
CAM_TEST
CAM_RST_L
CAM_GND
DF_CLK
DF_DATA0
DF_DATA1
DF_TEST
P31
A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9

CAMERA DSP (1/4) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
IC3001
XC62AP3002PL
IC3002
XC62AP3002PL
IC3003
XC62AP3002PL
IC3004
MN6577H
IC3005
MN6577H
IC3006
MN6577H
IC3007
HD151015TEL
IC3008
HD151015TEL
IC3009
HD151015TEL
IC3010
74AC574SJ-R1
IC3011
74AC574SJ-R1
IC3012
74AC574SJ-R1
IC3013
TC7SH86FUTL
IC3014
NJM2904M-T1
IC3015
HD151015TEL
IC3016
NJM431U-TE2
IC3104
74AC86SJ-R1
A/D REF
VR3001
TP3001
EYF6CU
TP3002
EYF6CU
TP3003
EYF6CU
TP3004
EYF6CU
TP3005
EYF6CU
TP3006
EYF6CU
TP3007
EYF6CU
TG3001
EYF6CU
L3001
100U/LC
L3002
0/J8
L3003
100U/LC
+3R5V
+3VA
+5VA
DIG3V
D5V
+5V
+3V
+5R6V
AD_R
AD_R_GND
R_OE
AD_G
AD_G_GND
G_OE
AD_B
AD_B_GND
B_OE
CPOB_DS
FCK
BRD_LOC
R(0:9)
D_BUS(0:7)
KR(0:9)
G(0:9)
KG(0:9)
B(0:9)
KB(0:9)
(2)
(4)

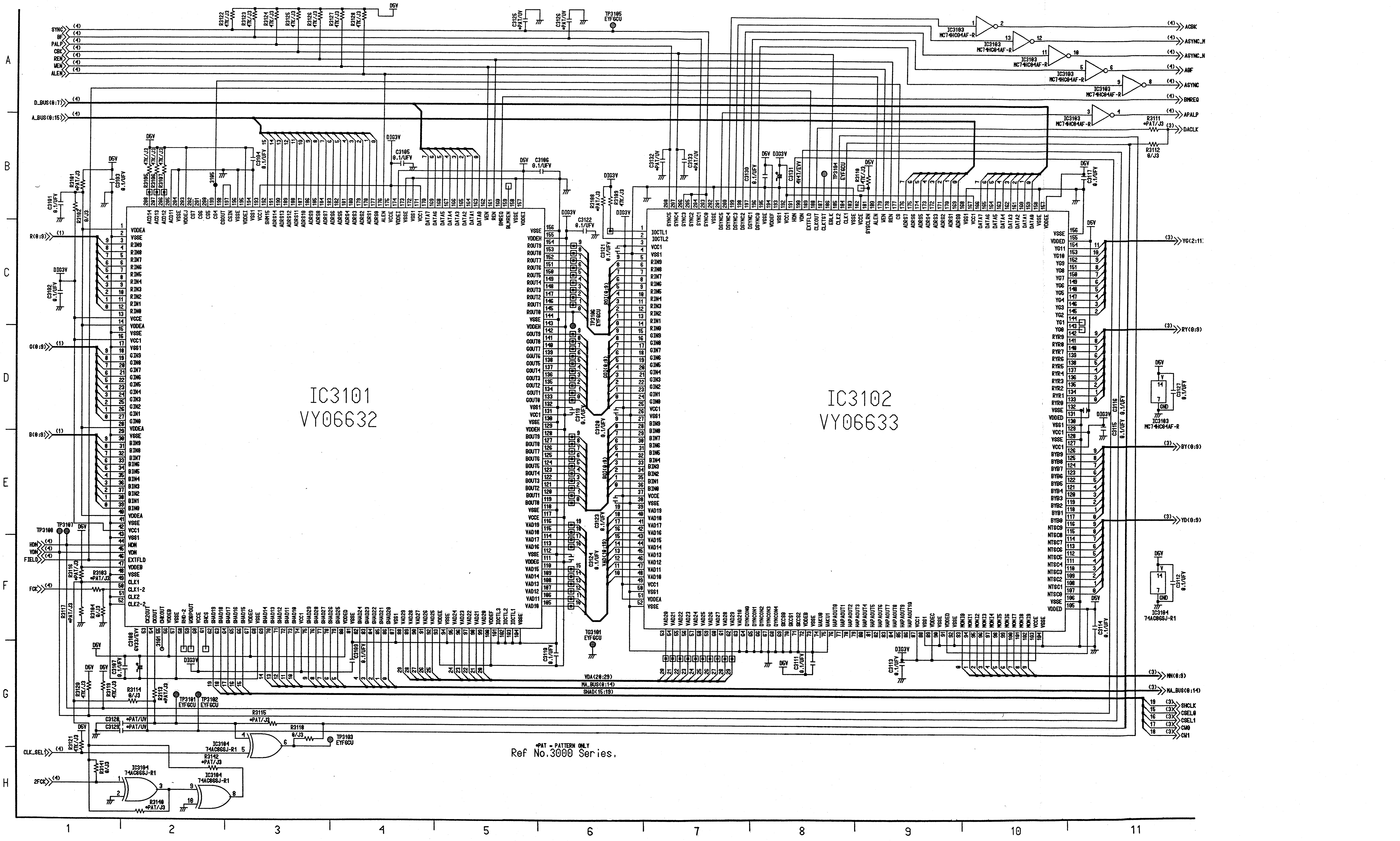
*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART

Ref No.3000 Series.

REVERSE SIDE

CAMERA SYSCON 5/5

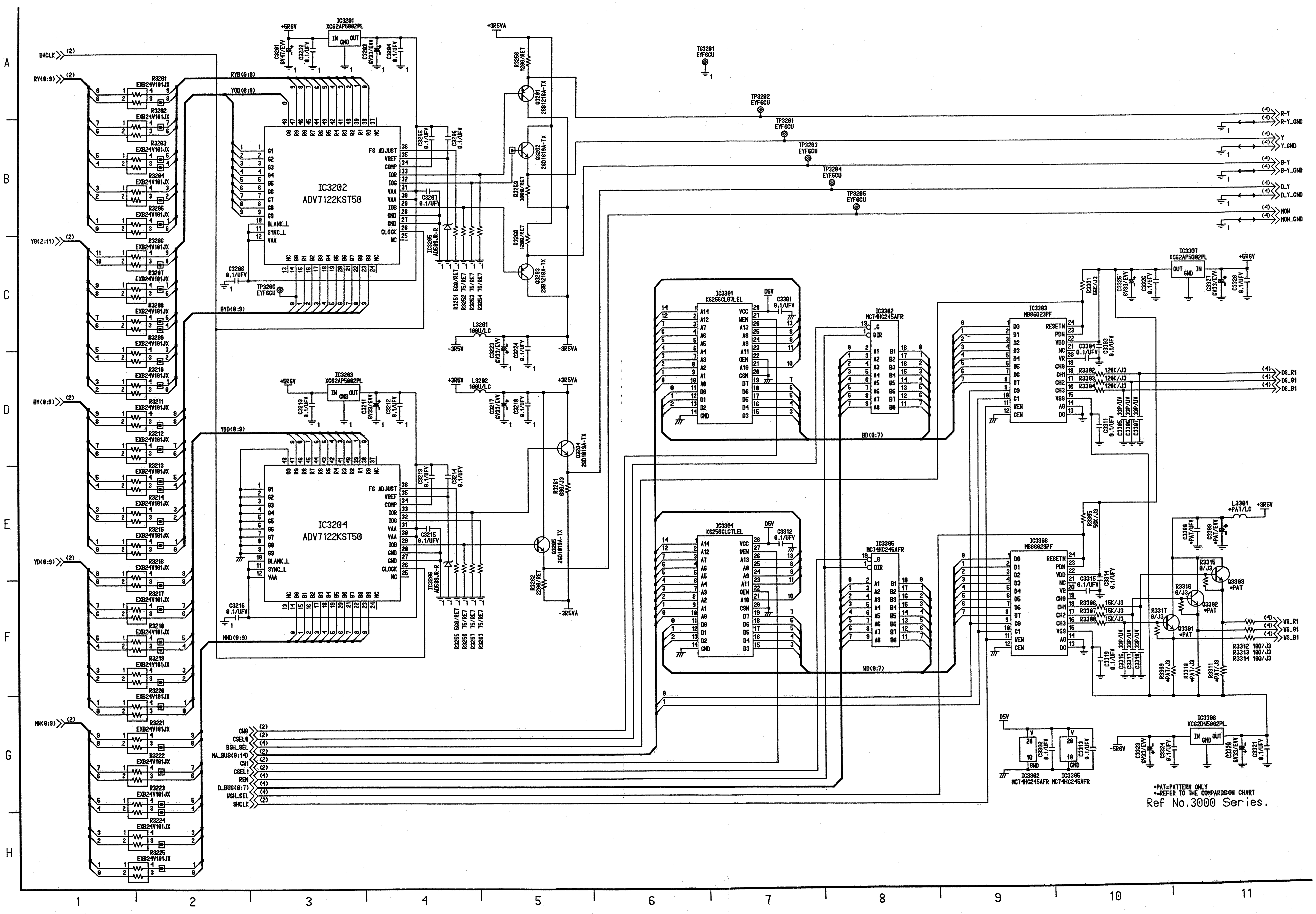
CAMERA DSP (2/4) SCHEMATIC DIAGRAM


IC3101
VY06632
IC3102
VY06633
SYNC
BF
PALP
CBK
REN
WEN
ALEN
D_BUS(0:7)
A_BUS(0:15)
R(0:9)
G(0:9)
B(0:9)
HDN
VDN
FIELD
FCK
CLK_SEL1
2FCK
ACBK
ASYNC_N
ABF
ASYNC
BMREQ
APALP
DACLK
YG(2:11)
RY(0:9)
BY(0:9)
YD(0:9)
MN(0:9)
MA_BUS(0:14)
VDA(20:29)
SHAD(15:19)
SHCLK
CSEL0
CSEL1
CM0
CM1
IC3103 MC74HC04AF-R
IC3104 74AC86SJ-R1
D5V
DIG3V
TP3105 EYF6CU
TP3106 EYF6CU
TP3101 EYF6CU
TP3102 EYF6CU
TP3103 EYF6CU
TP3104 EYF6CU
TG3101 EYF6CU
A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11

*PAT = PATTERN ONLY

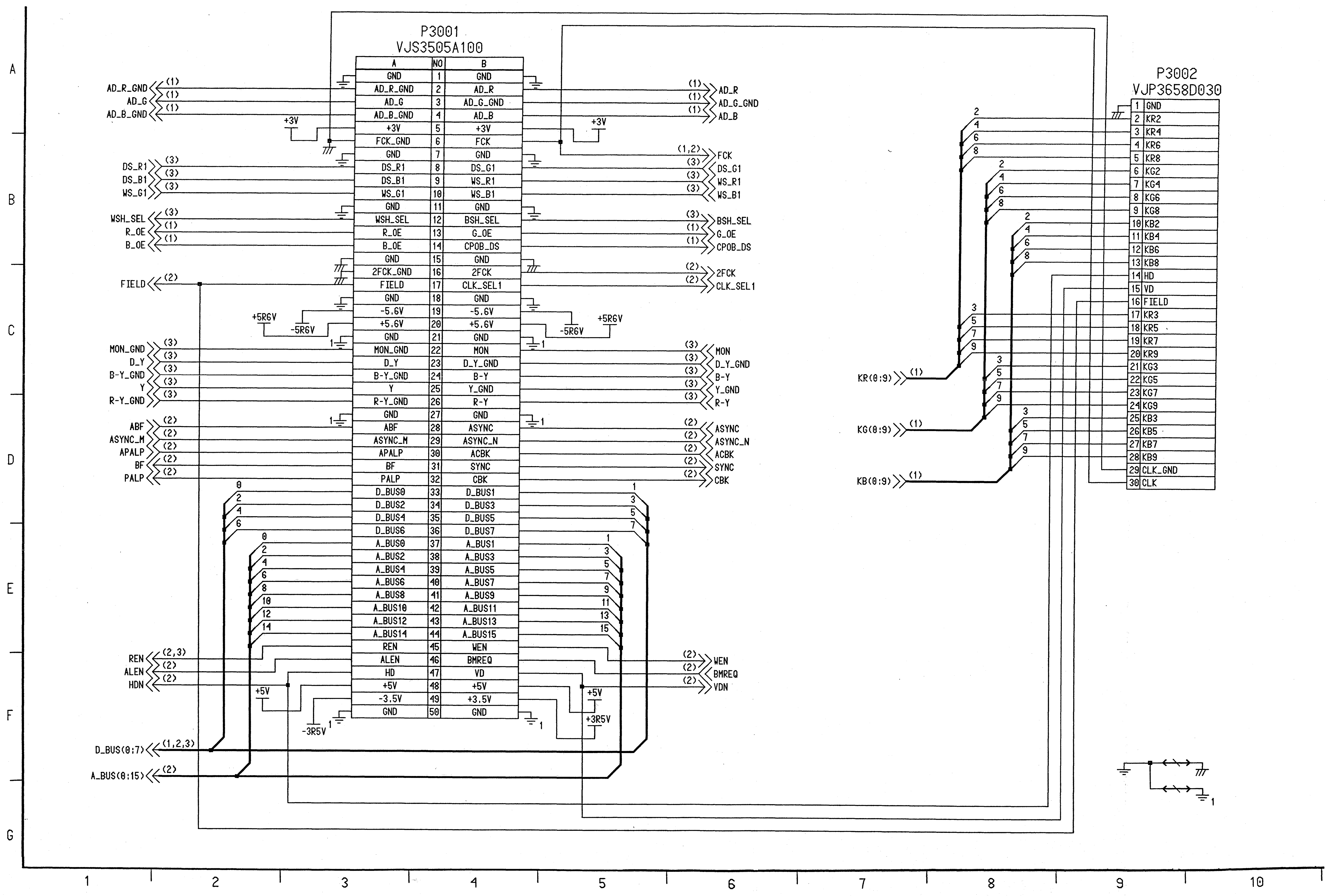
Ref No.3000 Series.

CAMERA DSP (3/4) SCHEMATIC DIAGRAM

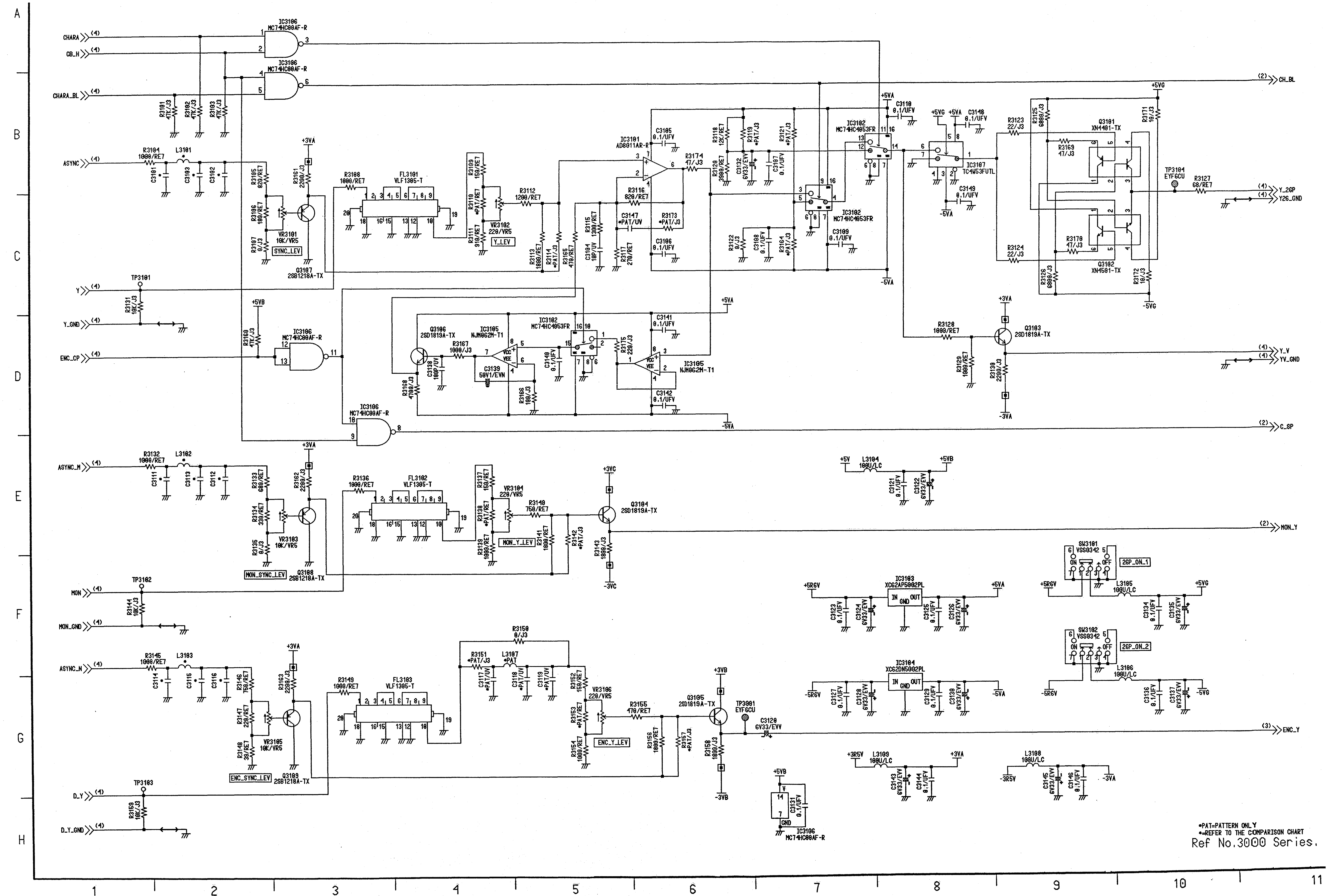

A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
DACLK (2)
RY(0:9) (2)
YG(2:11) (2)
BY(0:9) (2)
YD(0:9) (2)
MM(0:9) (2)
RYD(0:9)
YGD(0:9)
BYD(0:9)
YDD(0:9)
MMD(0:9)
EXB24V101JX
IC3201
XC62AP5002PL
IC3202
ADV7122KST50
IC3203
XC62AP5002PL
IC3204
ADV7122KST50
IC3205
AD589JR-R
IC3206
AD589JR-R
+5R6V
+3R5VA
-3R5V
-3R5VA
L3201
100U/LC
L3202
100U/LC
Q3201
2SB1218A-TX
Q3202
2SD1819A-TX
Q3203
2SB1218A-TX
Q3204
2SD1819A-TX
Q3205
2SD1819A-TX
TG3201
EYF6CU
TP3201
TP3202
TP3203
TP3204
TP3205
TP3206
EYF6CU
(4) R-Y
(4) R-Y_GND
(4) Y
(4) Y_GND
(4) B-Y
(4) B-Y_GND
(4) D_Y
(4) D_Y_GND
(4) MON
(4) MON_GND
IC3301
K6256CLG7LEL
IC3302
MC74HC245AFR
IC3303
MB86023PF
IC3304
K6256CLG7LEL
IC3305
MC74HC245AFR
IC3306
MB86023PF
IC3307
XC62AP5002PL
IC3308
XC62DN5002PL
D5V
BD(0:7)
WD(0:7)
(4) DS_R1
(4) DS_G1
(4) DS_B1
(4) WS_R1
(4) WS_G1
(4) WS_B1
R3312 100/J3
R3313 100/J3
R3314 100/J3
L3301
*PAT/LC
Q3301
*PAT
Q3302
*PAT
Q3303
*PAT
CW0 (2)
CSEL0 (2)
BSH_SEL (4)
MA_BUS(0:14) (2)
CH1 (2)
CSEL1 (2)
REN (4)
D_BUS(0:7) (4)
WSH_SEL (4)
SHCLK (2)
-5R6V
*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART
Ref No.3000 Series.

REVERSE SIDE
CAMERA DSP 2/4

CAMERA DSP (4/4) CONNECTOR SCHEMATIC DIAGRAM


P3001
VJS3505A100
A
NO
B
1 GND GND
2 AD_R_GND AD_R
3 AD_G AD_G_GND
4 AD_B_GND AD_B
5 +3V +3V
6 FCK_GND FCK
7 GND GND
8 DS_R1 DS_G1
9 DS_B1 WS_R1
10 WS_G1 WS_B1
11 GND GND
12 WSH_SEL BSH_SEL
13 R_OE G_OE
14 B_OE CPOB_DS
15 GND GND
16 2FCK_GND 2FCK
17 FIELD CLK_SEL1
18 GND GND
19 -5.6V -5.6V
20 +5.6V +5.6V
21 GND GND
22 MON_GND MON
23 D_Y D_Y_GND
24 B-Y_GND B-Y
25 Y Y_GND
26 R-Y_GND R-Y
27 GND GND
28 ABF ASYNC
29 ASYNC_M ASYNC_N
30 APALP ACBK
31 BF SYNC
32 PALP CBK
33 D_BUS0 D_BUS1
34 D_BUS2 D_BUS3
35 D_BUS4 D_BUS5
36 D_BUS6 D_BUS7
37 A_BUS0 A_BUS1
38 A_BUS2 A_BUS3
39 A_BUS4 A_BUS5
40 A_BUS6 A_BUS7
41 A_BUS8 A_BUS9
42 A_BUS10 A_BUS11
43 A_BUS12 A_BUS13
44 A_BUS14 A_BUS15
45 REN WEN
46 ALEN BMREQ
47 HD VD
48 +5V +5V
49 -3.5V +3.5V
50 GND GND
AD_R_GND (1)
AD_G (1)
AD_B_GND (1)
+3V
DS_R1 (3)
DS_B1 (3)
WS_G1 (3)
WSH_SEL (3)
R_OE (1)
B_OE (1)
FIELD (2)
+5R6V
-5R6V
MON_GND (3)
D_Y (3)
B-Y_GND (3)
Y (3)
R-Y_GND (3)
ABF (2)
ASYNC_M (2)
APALP (2)
BF (2)
PALP (2)
REN (2,3)
ALEN (2)
HDN (2)
+5V
-3R5V
D_BUS(0:7) (1,2,3)
A_BUS(0:15) (2)
(1) AD_R
(1) AD_G_GND
(1) AD_B
(1,2) FCK
(3) DS_G1
(3) WS_R1
(3) WS_B1
(3) BSH_SEL
(1) G_OE
(1) CPOB_DS
(2) 2FCK
(2) CLK_SEL1
(3) MON
(3) D_Y_GND
(3) B-Y
(3) Y_GND
(3) R-Y
(2) ASYNC
(2) ASYNC_N
(2) ACBK
(2) SYNC
(2) CBK
(2) WEN
(2) BMREQ
(2) VDN
+3R5V
P3002
VJP3658D030
1 GND
2 KR2
3 KR4
4 KR6
5 KR8
6 KG2
7 KG4
8 KG6
9 KG8
10 KB2
11 KB4
12 KB6
13 KB8
14 HD
15 VD
16 FIELD
17 KR3
18 KR5
19 KR7
20 KR9
21 KG3
22 KG5
23 KG7
24 KG9
25 KB3
26 KB5
27 KB7
28 KB9
29 CLK_GND
30 CLK
KR(0:9) (1)
KG(0:9) (1)
KB(0:9) (1)
A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9
10

CAMERA ENCODER (1/7) SCHEMATIC DIAGRAM

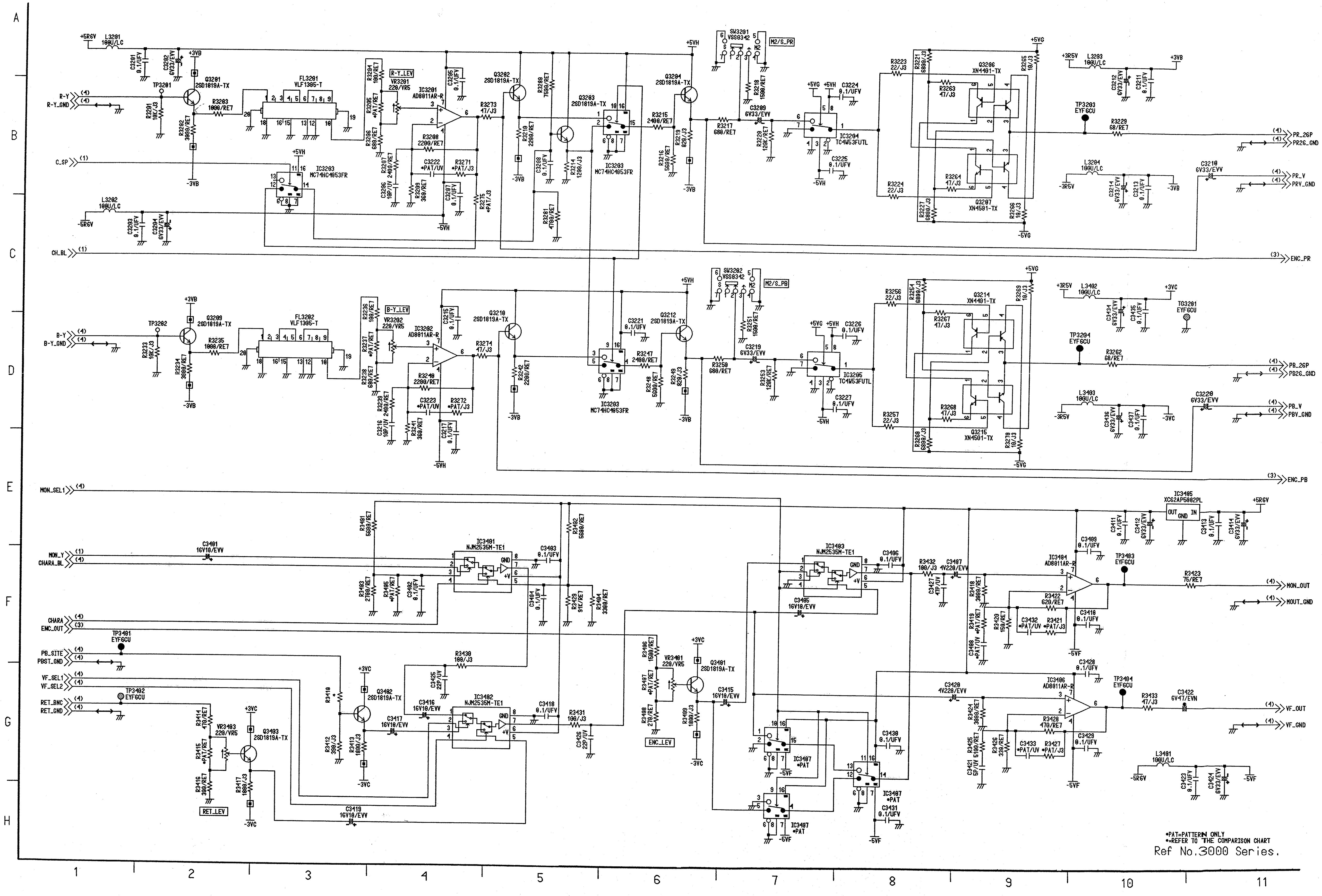

A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
CHARA
CB_H
CHARA_BL
ASYNC
Y
Y_GND
ENC_CP
ASYNC_M
MON
MON_GND
ASYNC_N
D_Y
D_Y_GND
CH_BL
Y_26P
Y26_GND
Y_V
YV_GND
C_SP
MON_Y
ENC_Y
IC3106 MC74HC08AF-R
IC3101 AD8011AR-R
IC3102 MC74HC4053FR
IC3107 TC4W53FUTL
IC3105 NJM062M-T1
IC3103 XC62AP5002PL
IC3104 XC62DN5002PL
FL3101 VLF1305-T
FL3102 VLF1305-T
FL3103 VLF1305-T
Q3101 XN4401-TX
Q3102 XN4501-TX
Q3103 2SD1819A-TX
Q3104 2SD1819A-TX
Q3105 2SD1819A-TX
Q3106 2SD1819A-TX
Q3107 2SB1218A-TX
Q3108 2SB1218A-TX
Q3109 2SB1218A-TX
SW3101 VSS0342
SW3102 VSS0342
TP3101
TP3102
TP3103
TP3104 EYF6CU
TP3001 EYF6CU
SYNC_LEV
Y_LEV
MON_SYNC_LEV
MON_Y_LEV
ENC_SYNC_LEV
ENC_Y_LEV
26P_ON_1
26P_ON_2
VR3101 10K/VR5
VR3102 220/VR5
VR3103 10K/VR5
VR3104 220/VR5
VR3105 10K/VR5
VR3106 220/VR5
+3VA
+5VA
-5VA
+5VB
+3VB
-3VB
+3VC
-3VC
+5VG
-5VG
-3VA
+5R6V
-5R6V
+3R5V
-3R5V

*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART
Ref No.3000 Series.

REVERSE SIDE

CAMERA DSP 4/4

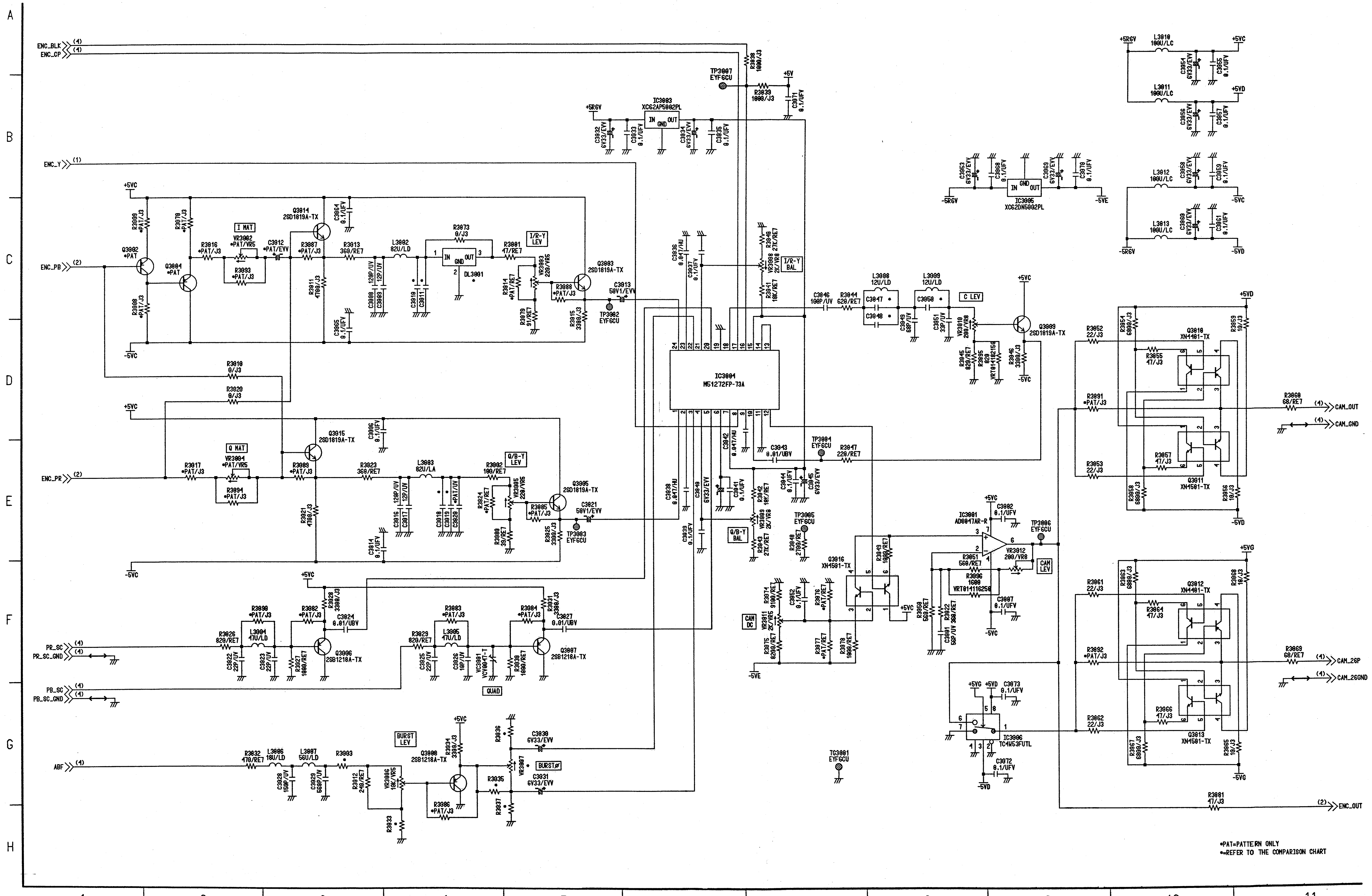
CAMERA ENCODER (2/7) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
R-Y
R-Y_GND
C_SP
CH_BL
B-Y
B-Y_GND
MON_SEL1
MON_Y
CHARA_BL
CHARA
ENC_OUT
PB_SITE
PBST_GND
VF_SEL1
VF_SEL2
RET_BNC
RET_GND
PR_26P
PR26_GND
PR_V
PRV_GND
ENC_PR
PB_26P
PB26_GND
PB_V
PBV_GND
ENC_PB
MON_OUT
MOUT_GND
VF_OUT
VF_GND
Q3201 2SD1819A-TX
FL3201 VLF1305-T
VR3201 220/VR5
IC3201 AD8011AR-R
Q3202 2SD1819A-TX
Q3203 2SD1819A-TX
IC3203 MC74HC4053FR
Q3204 2SD1819A-TX
SW3201 VSS0342
M2/S_PR
IC3204 TC4W53FUTL
Q3206 XN4401-TX
Q3207 XN4501-TX
TP3201
TP3203 EYF6CU
L3201 100U/LC
L3202 100U/LC
L3203 100U/LC
L3204 100U/LC
R-Y_LEV
Q3209 2SD1819A-TX
FL3202 VLF1305-T
VR3202 220/VR5
IC3202 AD8011AR-R
Q3210 2SD1819A-TX
Q3212 2SD1819A-TX
SW3202 VSS0342
M2/S_PB
IC3205 TC4W53FUTL
Q3214 XN4401-TX
Q3215 XN4501-TX
TP3202
TP3204 EYF6CU
TC3201 EYF6CU
L3402 100U/LC
L3403 100U/LC
B-Y_LEV
IC3401 NJM2535M-TE1
IC3402 NJM2535M-TE1
IC3403 NJM2535M-TE1
IC3404 AD8011AR-R
IC3405 XC62AP5002PL
IC3406 AD8011AR-R
IC3407
Q3401 2SD1819A-TX
Q3402 2SD1819A-TX
Q3403 2SD1819A-TX
VR3401 220/VR5
VR3403 220/VR5
TP3401 EYF6CU
TP3402 EYF6CU
TP3403 EYF6CU
TP3404 EYF6CU
L3401 100U/LC
ENC_LEV
RET_LEV
+5R6V
-5R6V
+3R5V
-3R5V
+5VG
-5VG
+5VH
-5VH
+3VB
-3VB
+3VC
-3VC
-5VF
+5R6V

*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART

Ref No.3000 Series.

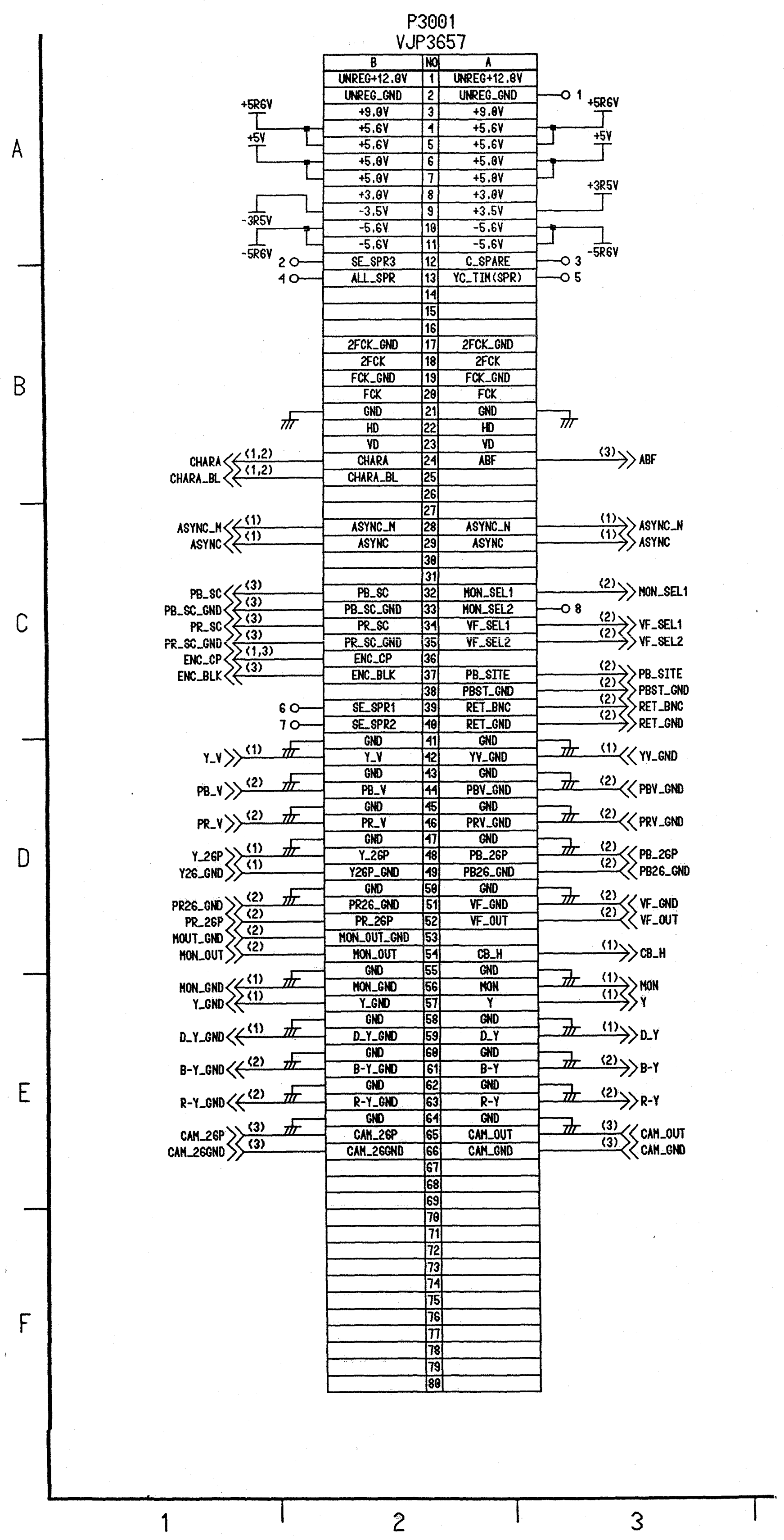
CAMERA ENCODER (3/7) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
ENC_BLK
ENC_CP
ENC_Y
ENC_PB
ENC_PR
PR_SC
PR_SC_GND
PB_SC
PB_SC_GND
ABF
CAM_OUT
CAM_GND
CAM_2GP
CAM_2GGND
ENC_OUT
IC3004
M51272FP-73A
IC3003
XC62AP5002PL
IC3005
XC62DN5002PL
IC3001
AD8047AR-R
IC3006
TC4W53FUTL
DL3001
Q3014
2SD1819A-TX
Q3015
2SD1819A-TX
Q3003
2SD1819A-TX
Q3005
2SD1819A-TX
Q3009
2SD1819A-TX
Q3006
2SB1218A-TX
Q3007
2SB1218A-TX
Q3008
2SB1218A-TX
Q3016
XN4501-TX
Q3010
XN4401-TX
Q3011
XN4501-TX
Q3012
XN4401-TX
Q3013
XN4501-TX
I MAT
Q MAT
I/R-Y LEV
Q/B-Y LEV
I/R-Y BAL
Q/B-Y BAL
C LEV
CAM LEV
CAM DC
BURST LEV
BURSTφ
QUAD
TP3007
TP3002
TP3003
TP3004
TP3005
TP3006
TG3001
EYF6CU
+5VC
-5VC
+5V
+5R6V
-5R6V
+5VD
-5VD
+5VG
-5VG
-5VE
*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART

REVERSE SIDE

CAMERA ENCODER 2/7

CAMERA ENCODER (4/7) CONNECTOR SCHEMATIC DIAGRAM


P3001
VJP3657
B
NO
A
UNREG+12.0V 1 UNREG+12.0V
UNREG_GND 2 UNREG_GND
+9.0V 3 +9.0V
+5.6V 4 +5.6V
+5.6V 5 +5.6V
+5.0V 6 +5.0V
+5.0V 7 +5.0V
+3.0V 8 +3.0V
-3.5V 9 +3.5V
-5.6V 10 -5.6V
-5.6V 11 -5.6V
SE_SPR3 12 C_SPARE
ALL_SPR 13 YC_TIN(SPR)
2FCK_GND 17 2FCK_GND
2FCK 18 2FCK
FCK_GND 19 FCK_GND
FCK 20 FCK
GND 21 GND
HD 22 HD
VD 23 VD
CHARA 24 ABF
CHARA_BL 25
ASYNC_M 28 ASYNC_N
ASYNC 29 ASYNC
PB_SC 32 MON_SEL1
PB_SC_GND 33 MON_SEL2
PR_SC 34 VF_SEL1
PR_SC_GND 35 VF_SEL2
ENC_CP 36
ENC_BLK 37 PB_SITE
38 PBST_GND
SE_SPR1 39 RET_BNC
SE_SPR2 40 RET_GND
GND 41 GND
Y_V 42 YV_GND
GND 43 GND
PB_V 44 PBV_GND
GND 45 GND
PR_V 46 PRV_GND
GND 47 GND
Y_26P 48 PB_26P
Y26P_GND 49 PB26_GND
GND 50 GND
PR26_GND 51 VF_GND
PR_26P 52 VF_OUT
MON_OUT_GND 53
MON_OUT 54 CB_H
GND 55 GND
MON_GND 56 MON
Y_GND 57 Y
GND 58 GND
D_Y_GND 59 D_Y
GND 60 GND
B-Y_GND 61 B-Y
GND 62 GND
R-Y_GND 63 R-Y
GND 64 GND
CAM_26P 65 CAM_OUT
CAM_26GND 66 CAM_GND
+5R6V
+5V
+3R5V
-3R5V
-5R6V
CHARA (1,2)
CHARA_BL (1,2)
ASYNC_M (1)
ASYNC (1)
ABF (3)
ASYNC_N (1)
PB_SC (3)
PB_SC_GND (3)
PR_SC (3)
PR_SC_GND (3)
ENC_CP (1,3)
ENC_BLK (3)
MON_SEL1 (2)
VF_SEL1 (2)
VF_SEL2 (2)
PB_SITE (2)
PBST_GND (2)
RET_BNC (2)
RET_GND (2)
Y_V (1)
PB_V (2)
PR_V (2)
Y_26P (1)
Y26_GND (1)
PR26_GND (2)
PR_26P (2)
MOUT_GND (2)
MON_OUT (2)
MON_GND (1)
Y_GND (1)
D_Y_GND (1)
B-Y_GND (2)
R-Y_GND (2)
CAM_26P (3)
CAM_26GND (3)
YV_GND (1)
PBV_GND (2)
PRV_GND (2)
PB_26P (2)
PB26_GND (2)
VF_GND (2)
VF_OUT (2)
CB_H (1)
MON (1)
Y (1)
D_Y (1)
B-Y (2)
R-Y (2)
CAM_OUT (3)
CAM_GND (3)
A
B
C
D
E
F
1
2
3

CAMERA ENCODER (5/7)
COMPARISON CHART 1 BETWEEN MODELS

REF	NTSC	PAL	ON
C3010	56P/UV	100P/UV	56P/UV
C3011	33P/UV	15P/UV	33P/UV
C3012	*PAT/EVV	*PAT/EVV	6V33/EVV
C3018	56P/UV	100P/UV	680P/USV
C3019	33P/UV	15P/UV	330P/UV
C3020	*PAT/UV	*PAT/UV	9P/UV
C3047	3P/UV	2P/UV	3P/UV
C3048	33P/UV	18P/UV	33P/UV
C3050	18P/UV	9P/UV	18P/UV
C3101	8P/UV	22P/UV	18P/UV
C3102	100P/UV	180P/UV	120P/UV
C3103	*PAT/UV	33P/UV	12P/UV
C3111	8P/UV	22P/UV	18P/UV
C3112	100P/UV	180P/UV	120P/UV
C3113	*PAT/UV	33P/UV	12P/UV
C3114	8P/UV	22P/UV	18P/UV
C3115	100P/UV	180P/UV	120P/UV
C3116	*PAT/UV	33P/UV	12P/UV
C3117	*PAT/UV	*PAT/UV	18P/UV
C3118	*PAT/UV	*PAT/UV	18P/UV
C3119	*PAT/UV	*PAT/UV	1P/UV
C3147	*PAT/UV	*PAT/UV	27P/UV
C3222	*PAT/UV	*PAT/UV	27P/UV
C3223	*PAT/UV	*PAT/UV	27P/UV
C3408	*PAT/UV	*PAT/UV	12P/UV
C3432	*PAT/UV	*PAT/UV	27P/UV
C3433	*PAT/UV	*PAT/UV	27P/UV
DL3001	*PAT	*PAT	ELB4M087
IC3407	*PAT	*PAT	MC74HC4053FR
L3101	47U/LD	100U/LD	47U/LD
L3102	47U/LD	100U/LD	47U/LD
L3103	47U/LD	100U/LD	47U/LD
L3107	*PAT	*PAT	39U/LD
Q3002	*PAT	*PAT	2SB1218A-TX
Q3004	*PAT	*PAT	2SB1218A-TX
R3003	110/RE7	0/J3	110/RE7
R3008	*PAT/J3	*PAT/J3	560/J3
R3009	*PAT/J3	*PAT/J3	560/J3
R3014	*PAT/RE7	*PAT/RE7	180/RE7
R3016	*PAT/J3	*PAT/J3	820/J3
R3017	*PAT/J3	*PAT/J3	820/J3
R3024	*PAT/RE7	*PAT/RE7	180/RE7
R3033	120/RE7	240/RE7	120/RE7

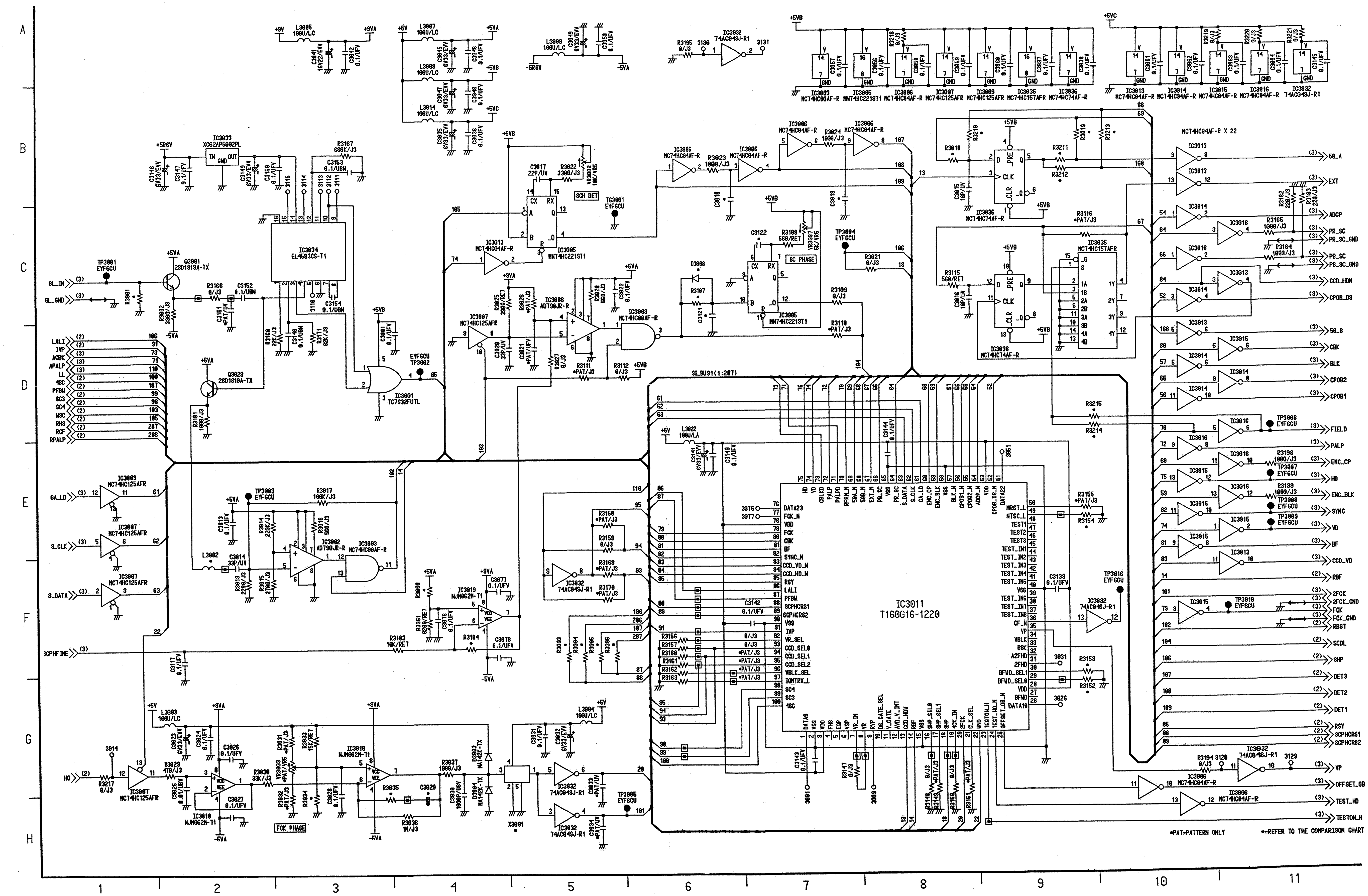
CAMERA ENCODER (7/7)
COMPARISON CHART 3 BETWEEN MODELS

REF	NTSC	PAL	ON
VR3004	*PAT/VR5	*PAT/VR5	1K/VR5
VR3007	*PAT/VR5	5K/VR5	5K/VR5

CAMERA ENCODER (6/7)
COMPARISON CHART 2 BETWEEN MODELS

REF	NTSC	PAL	ON
R3035	0/J3	*PAT/J3	0/J3
R3036	0/J3	*PAT/J3	0/J3
R3037	*PAT/J3	*PAT/J3	2200/J3
R3070	*PAT/J3	*PAT/J3	1000/J3
R3076	*PAT/RE7	*PAT/RE7	12K/RE7
R3077	*PAT/RE7	*PAT/RE7	8200/RE7
R3082	*PAT/J3	*PAT/J3	0/J3
R3083	*PAT/J3	*PAT/J3	0/J3
R3084	*PAT/J3	*PAT/J3	0/J3
R3085	*PAT/J3	*PAT/J3	0/J3
R3086	*PAT/J3	*PAT/J3	0/J3
R3087	*PAT/J3	*PAT/J3	0/J3
R3088	*PAT/J3	*PAT/J3	0/J3
R3089	*PAT/J3	*PAT/J3	0/J3
R3090	*PAT/J3	*PAT/J3	0/J3
R3091	*PAT/J3	*PAT/J3	0/J3
R3092	*PAT/J3	*PAT/J3	0/J3
R3093	*PAT/J3	*PAT/J3	0/J3
R3094	*PAT/J3	*PAT/J3	0/J3
R3110	*PAT/RE7	*PAT/RE7	220/RE7
R3114	*PAT/RE7	*PAT/RE7	220/RE7
R3119	*PAT/J3	*PAT/J3	1000/J3
R3121	*PAT/J3	*PAT/J3	1000/J3
R3138	*PAT/RE7	*PAT/RE7	240/RE7
R3142	*PAT/J3	*PAT/J3	1000/J3
R3151	*PAT/J3	*PAT/J3	0/J3
R3153	*PAT/RE7	*PAT/RE7	270/RE7
R3157	*PAT/J3	*PAT/J3	1000/J3
R3164	*PAT/J3	*PAT/J3	1000/J3
R3173	*PAT/J3	*PAT/J3	0/J3
R3205	*PAT/RE7	*PAT/RE7	220/RE7
R3237	*PAT/RE7	*PAT/RE7	220/RE7
R3271	*PAT/J3	*PAT/J3	0/J3
R3272	*PAT/J3	*PAT/J3	0/J3
R3275	*PAT/J3	*PAT/J3	47/J3
R3405	*PAT/RE7	*PAT/RE7	39K/RE7
R3407	*PAT/RE7	*PAT/RE7	220/RE7
R3410	680/J3	560/J3	680/J3
R3415	*PAT/RE7	*PAT/RE7	220/RE7
R3419	*PAT/RE7	*PAT/RE7	2200/RE7
R3421	*PAT/J3	*PAT/J3	0/J3
R3427	*PAT/J3	*PAT/J3	0/J3
VR3002	*PAT/VR5	*PAT/VR5	1K/VR5

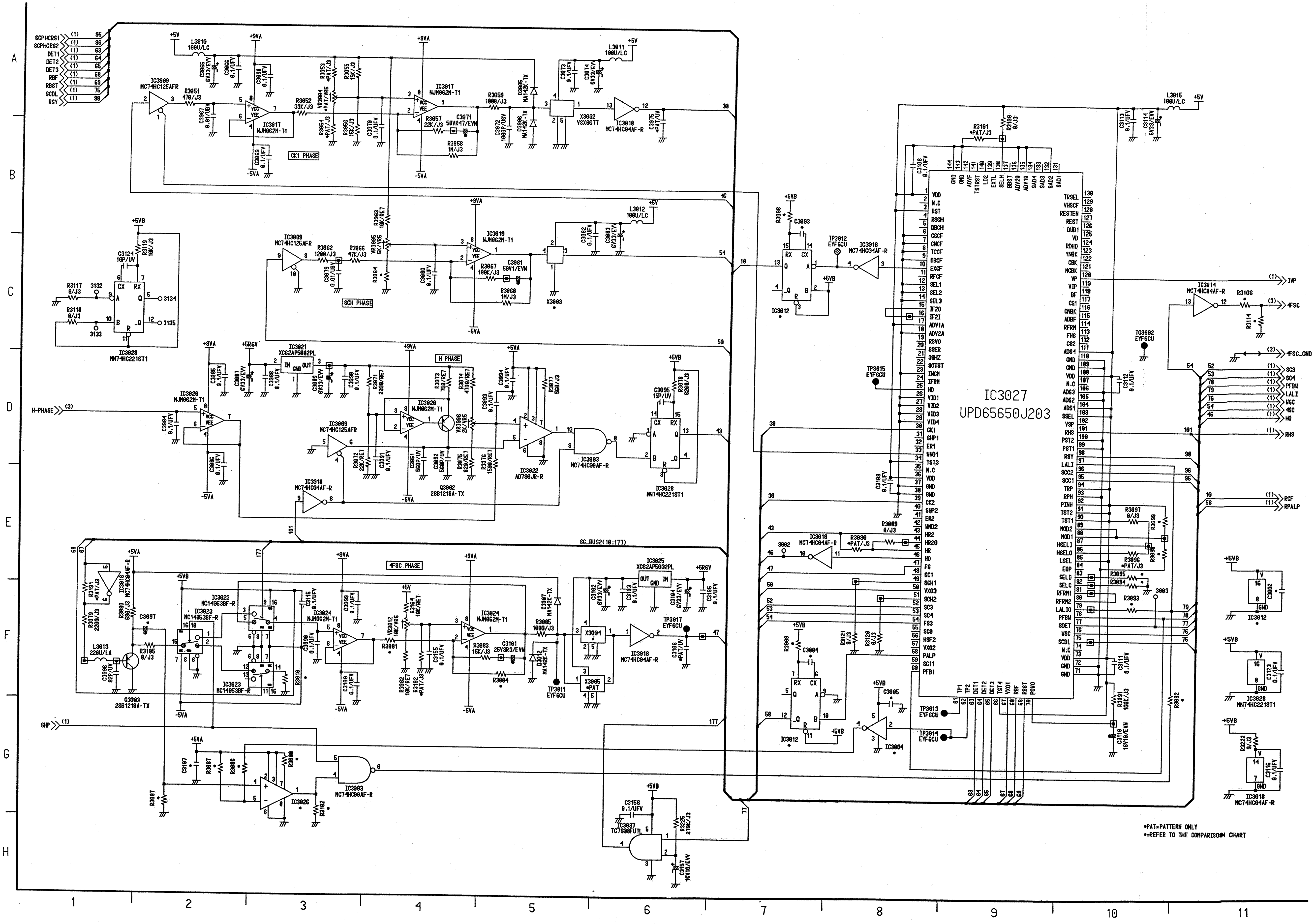
CAMERA SYNC (1/6) SCHEMATIC DIAGRAM


IC3011
T160G16-1220
IC3034
EL4583CS-T1
IC3033
XC62AP5002PL
IC3001
TC7S32FUTL
IC3005
MN74HC221ST1
IC3036
MC74HC74AF-R
IC3035
MC74HC157AFR
IC3002
AD799JR-R
IC3003
MC74HC00AF-R
IC3008
AD799JR-R
IC3010
NJM062M-T1
IC3019
NJM062M-T1
IC3007
MC74HC125AFR
IC3009
MC74HC125AFR
IC3032
74AC04SJ-R1
MC74HC04AF-R X 22
Q3001
2SD1819A-TX
Q3023
2SD1819A-TX
SG_BUS1(1:287)
GL_IN
GL_GND
LALI
IVP
ACBK
APALP
LL
4SC
PFBW
SC3
SC4
WSC
RHS
RCF
RPALP
GA_LD
S_CLK
S_DATA
SCPHFINE
HO
50_A
EXT
ADCP
PR_SC
PR_SC_GND
PB_SC
PB_SC_GND
CCD_HDN
CPOB_DS
50_B
CBK
BLK
CPOB2
CPOB1
FIELD
PALP
ENC_CP
HD
ENC_BLK
SYNC
VD
BF
CCD_VD
RBF
2FCK
2FCK_GND
FCK
FCK_GND
RBST
SCDL
SHP
DET3
DET2
DET1
RSY
SCPHCRS1
SCPHCRS2
VP
OFFSET_OB
TEST_HD
TESTON_H
SCH DET
SC PHASE
FCK PHASE
X3001
+5V
+9V
+5VA
+9VA
-5VA
+5VB
+5VC
-5R6V
+5R6V
*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART
A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11

REVERSE SIDE

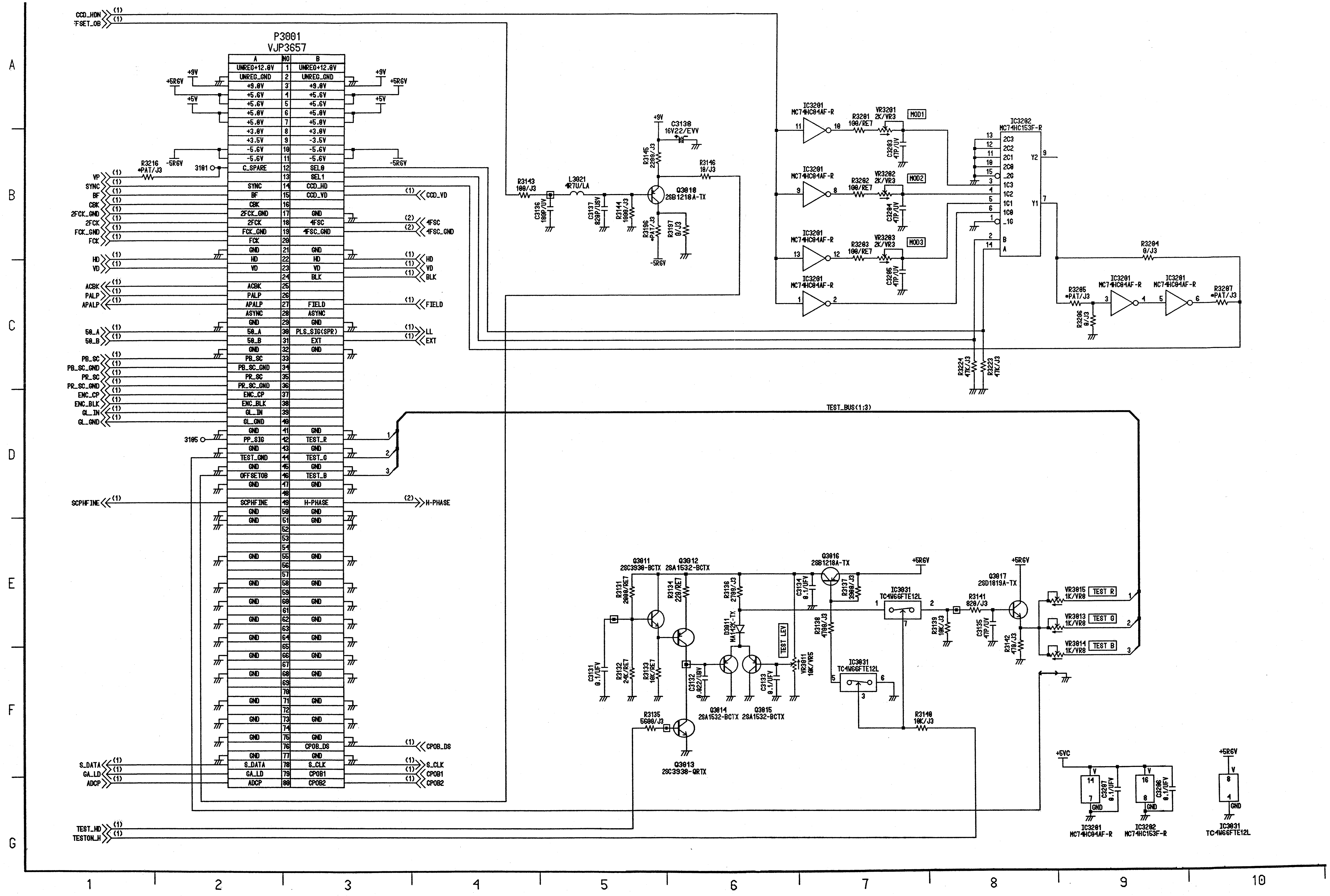
CAMERA ENCODER 4/7—7/7

CAMERA SYNC (2/6) SCHEMATIC DIAGRAM


SCPHCRS1
SCPHCRS2
DET1
DET2
DET3
RBF
RBST
SCDL
RSY
H-PHASE
SHP
IC3009 MC74HC125AFR
IC3017 NJM062M-T1
IC3019 NJM062M-T1
IC3020 NJM062M-T1
IC3022 AD790JR-R
IC3024 NJM062M-T1
IC3021 XC62AP5002PL
IC3025 XC62AP5002PL
IC3023 MC14053BF-R
IC3026
IC3018 MC74HC04AF-R
IC3003 MC74HC08AF-R
IC3028 MN74HC221ST1
IC3012
IC3014 MC74HC04AF-R
IC3037 TC7S08FUTL
IC3027
UPD65650J203
X3002 VSX0677
X3003
X3004
X3005 *PAT
Q3002 2SB1218A-TX
Q3003 2SB1218A-TX
L3010 100U/LC
L3011 100U/LC
L3012 100U/LC
L3013 220U/LA
L3015 100U/LC
D3005 MA142K-TX
D3006 MA142K-TX
D3007 MA142K-TX
D3012 MA142K-TX
TP3011 EYF6CU
TP3012 EYF6CU
TP3013 EYF6CU
TP3014 EYF6CU
TP3015 EYF6CU
TP3017 EYF6CU
TG3002 EYF6CU
CK1 PHASE
SCH PHASE
H PHASE
FSC PHASE
SG_BUS2(10:177)
+5V
+9VA
-5VA
+5VB
+5R6V
IVP
FSC
FSC_GND
SC3
SC4
PFBW
LALI
WSC
HO
RHS
RCF
RPALP
A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11

*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART

CAMERA SYNC (3/6) SCHEMATIC DIAGRAM


P3001
VJP3657
CCD_HDN
FSET_OB
CCD_VD
4FSC
4FSC_GND
HD
VD
BLK
FIELD
LL
EXT
H-PHASE
SCPHFINE
CPOB_DS
S_DATA
GA_LD
ADCP
S_CLK
CPOB1
CPOB2
TEST_HD
TESTON_H
TEST_BUS(1:3)
IC3201 MC74HC04AF-R
IC3202 MC74HC153F-R
IC3031 TC4W66FTE12L
Q3018 2SB1218A-TX
Q3011 2SC3938-BCTX
Q3012 2SA1532-BCTX
Q3013 2SC3938-QRTX
Q3014 2SA1532-BCTX
Q3015 2SA1532-BCTX
Q3016 2SB1218A-TX
Q3017 2SD1819A-TX
D3011 MA142K-TX
VR3201 2K/VR3
VR3202 2K/VR3
VR3203 2K/VR3
MOD1
MOD2
MOD3
VR3011 10K/VR5
TEST LEV
VR3015 1K/VR8
VR3013 1K/VR8
VR3014 1K/VR8
TEST R
TEST G
TEST B
+5VC
+5R6V
+9V
-5R6V
A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9
10

REVERSE SIDE
CAMERA SYNC 2/5

CAMERA SYNC (4/6)
COMPARISON CHART 1 BETWEEN MODELS

REF	NTSC	PAL-E	PAL-EN	ON
C3002	*PAT/UFV	0. 1/UFV	0. 1/UFV	0. 1/UFV
C3003	*PAT/UV	10P/UV	10P/UV	10P/UV
C3004	*PAT/UV	150P/UV	150P/UV	150P/UV
C3005	*PAT/UFV	0. 1/UFV	0. 1/UFV	0. 1/UFV
C3018	15P/UV	*PAT/UV	*PAT/UV	15P/UV
C3019	15P/UV	*PAT/UV	*PAT/UV	15P/UV
C3021	*PAT/UFV	*PAT/UFV	*PAT/UFV	0. 1/UFV
C3029	50VR47/EVN	50V1/EVN	50V1/EVN	50VR47/EVN
C3033	*PAT/UV	*PAT/UV	*PAT/UV	10P/UV
C3034	*PAT/UV	*PAT/UV	*PAT/UV	10P/UV
C3075	*PAT/UV	*PAT/UV	*PAT/UV	10P/UV
C3097	*PAT/EVN	16V10/EVN	16V10/EVN	16V10/EVN
C3106	*PAT/UV	*PAT/UV	*PAT/UV	10P/UV
C3107	*PAT/UFV	0. 1/UFV	0. 1/UFV	0. 1/UFV
C3121	10P/UV	*PAT/UV	*PAT/UV	10P/UV
C3122	22P/UV	12P/UV	12P/UV	22P/UV
C3151	*PAT/UV	*PAT/UV	*PAT/UV	470P/UV
D3008	MA142K-TX	*PAT	*PAT	MA142K-TX
IC3004	*PAT	TC7S04FUTL	TC7S04FUTL	TC7S04FUTL
IC3012	*PAT	MN74HC221ST1	MN74HC221ST1	MN74HC221ST1
IC3026	*PAT	AD790JR-R	AD790JR-R	AD790JR-R
L3002	68U/LA	39U/LA	39U/LA	68U/LA
R3001	75/RE7	910/RE7	75/RE7	75/RE7
R3003	0/J3	*PAT/J3	*PAT/J3	0/J3
R3004	*PAT/J3	0/J3	0/J3	0/J3
R3005	0/J3	*PAT/J3	*PAT/J3	0/J3
R3006	*PAT/J3	0/J3	0/J3	0/J3
R3007	*PAT/J3	10K/J3	10K/J3	10K/J3
R3008	*PAT/J3	15K/J3	15K/J3	15K/J3
R3009	*PAT/J3	270K/J3	270K/J3	270K/J3
R3010	0/J3	*PAT/J3	*PAT/J3	0/J3
R3018	560/RE7	*PAT/RE7	*PAT/RE7	560/RE7
R3019	*PAT/J3	0/J3	0/J3	0/J3
R3026	*PAT/J3	*PAT/J3	*PAT/J3	12K/J3
R3031	*PAT/J3	*PAT/J3	*PAT/J3	10K/J3
R3032	*PAT/J3	*PAT/J3	*PAT/J3	10K/J3
R3034	16K/RE7	22K/RE7	20K/RE7	16K/RE7
R3035	22K/J3	5100/RE7	5100/RE7	22K/J3
R3053	*PAT/J3	*PAT/J3	*PAT/J3	10K/J3
R3054	*PAT/J3	*PAT/J3	*PAT/J3	10K/J3
R3060	9100/RE7	11K/RE7	10K/RE7	9100/RE7
R3064	13K/RE7	22K/RE7	18K/RE7	13K/RE7
R3081	22K/J3	82K/J3	82K/J3	22K/J3

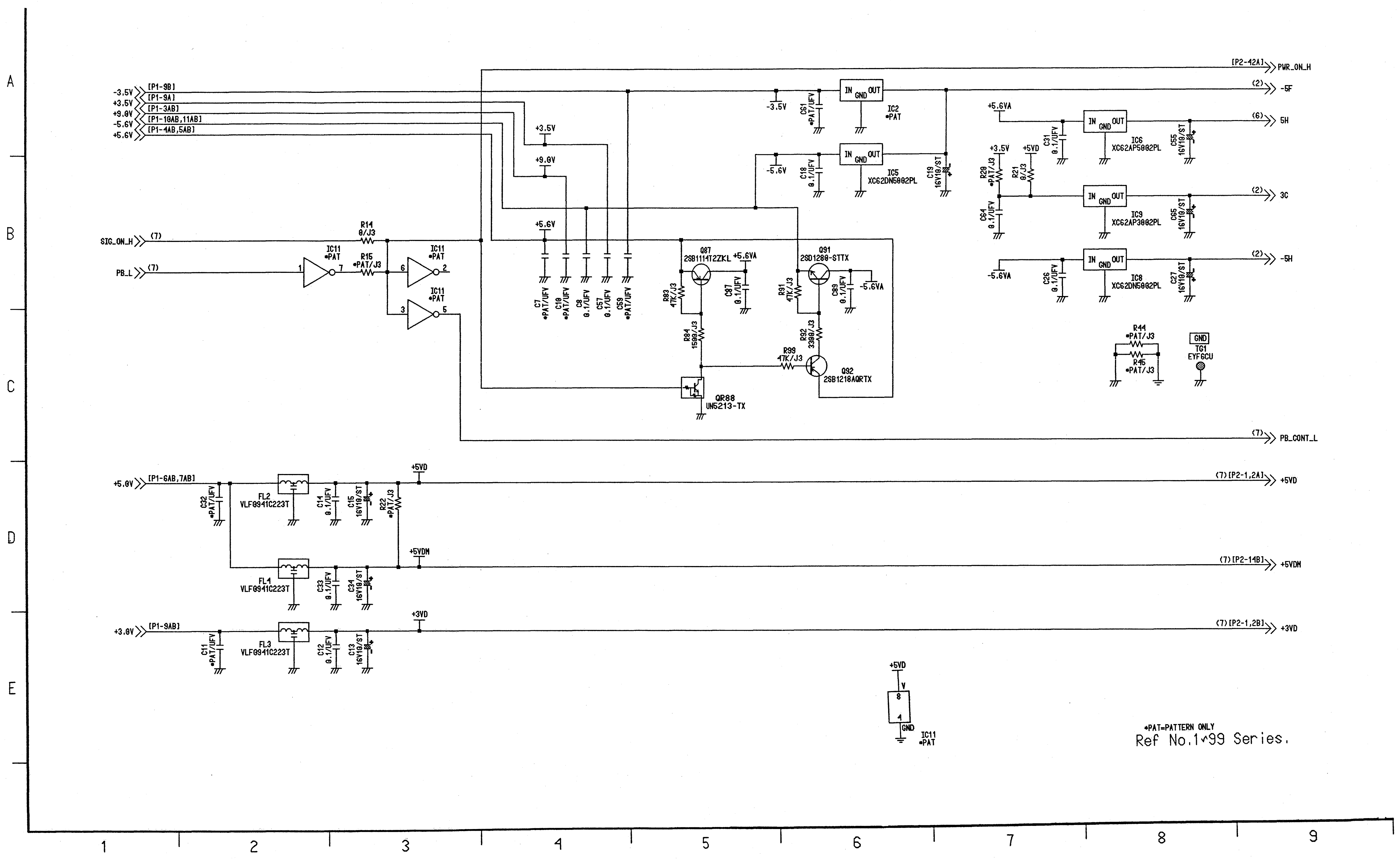
CAMERA SYNC (5/6)
COMPARISON CHART 2 BETWEEN MODELS

REF	NTSC	PAL-E	PAL-EN	ON
R3084	680K/J3	1M/J3	1M/J3	680K/J3
R3086	*PAT/J3	4700/J3	4700/J3	4700/J3
R3087	*PAT/J3	18K/J3	18K/J3	18K/J3
R3088	*PAT/J3	560/J3	560/J3	560/J3
R3090	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3092	*PAT/J3	0/J3	0/J3	0/J3
R3093	0/J3	*PAT/J3	*PAT/J3	0/J3
R3094	*PAT/J3	0/J3	0/J3	0/J3
R3095	*PAT/J3	0/J3	0/J3	0/J3
R3096	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3098	0/J3	*PAT/J3	*PAT/J3	0/J3
R3099	*PAT/J3	0/J3	0/J3	0/J3
R3101	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3102	0/J3	*PAT/J3	*PAT/J3	0/J3
R3104	5600/RE7	4700/RE7	4700/RE7	5600/RE7
R3106	*PAT/J3	1000/J3	1000/J3	1000/J3
R3107	820/RE7	0/J3	0/J3	820/RE7
R3110	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3111	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3114	*PAT/J3	1000/J3	1000/J3	1000/J3
R3116	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3149	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3151	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3152	0/J3	*PAT/J3	*PAT/J3	0/J3
R3153	*PAT/J3	0/J3	0/J3	0/J3
R3154	0/J3	*PAT/J3	*PAT/J3	0/J3
R3155	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3158	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3160	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3161	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3162	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3163	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3169	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3170	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3191	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3192	*PAT/J3	*PAT/J3	*PAT/J3	18K/J3
R3196	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3205	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3207	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R3210	*PAT/RE7	560/RE7	560/RE7	560/RE7
R3211	0/J3	*PAT/J3	*PAT/J3	0/J3
R3212	*PAT/J3	0/J3	0/J3	0/J3
R3213	0/J3	*PAT/J3	*PAT/J3	0/J3

CAMERA SYNC (6/6)
COMPARISON CHART 3 BETWEEN MODELS

REF	NTSC	PAL-E	PAL-EN	ON
R3214	0/J3	*PAT/J3	*PAT/J3	0/J3
R3215	*PAT/J3	0/J3	0/J3	0/J3
R3216	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
VR3003	*PAT/VR5	*PAT/VR5	*PAT/VR5	5K/VR5
VR3004	*PAT/VR5	*PAT/VR5	*PAT/VR5	5K/VR5
X3001	VSX0686	VSX0687	VSX0687	VSX0686
X3003	VSX0338	VSX0270	VSX0270	VSX0338
X3004	VSX0688	VSX0689	VSX0689	VSX0688
X3005	*PAT	*PAT	*PAT	VSX0332

VIDEO IF (1/7) SCHEMATIC DIAGRAM

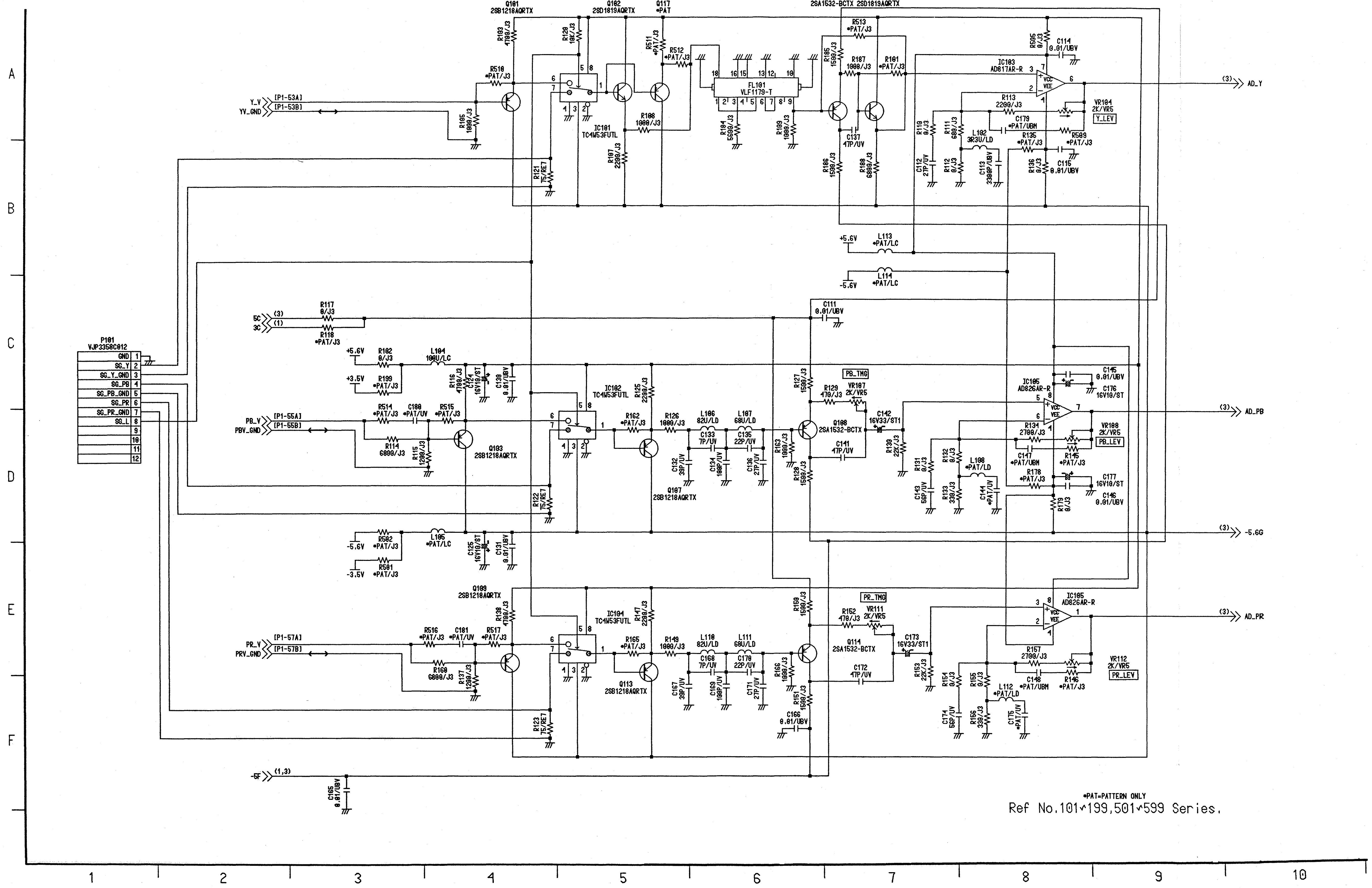

A
B
C
D
E
1
2
3
4
5
6
7
8
9
-3.5V
+3.5V
+9.0V
-5.6V
+5.6V
[P1-9B]
[P1-9A]
[P1-3AB]
[P1-10AB,11AB]
[P1-4AB,5AB]
[P2-42A]
PWR_ON_H
-3.5V
C61
*PAT/UFV
IN GND OUT
IC2
*PAT
(2)
-5F
+3.5V
+9.0V
-5.6V
C18
0.1/UFV
IN GND OUT
IC5
XC62DN5002PL
C19
16V10/ST
+5.6VA
C31
0.1/UFV
IN GND OUT
IC6
XC62AP5002PL
C55
16V10/ST
(6)
5H
+3.5V
+5VD
R20
*PAT/J3
R21
0/J3
C64
0.1/UFV
IN GND OUT
IC9
XC62AP3002PL
C65
16V10/ST
(2)
3C
-5.6VA
C26
0.1/UFV
IN GND OUT
IC8
XC62DN5002PL
C27
16V10/ST
(2)
-5H
SIG_ON_H
(7)
R14
0/J3
PB_L
(7)
IC11
*PAT
1
7
R15
*PAT/J3
6
IC11
*PAT
2
IC11
*PAT
3
5
+5.6V
C7
*PAT/UFV
C10
*PAT/UFV
C8
0.1/UFV
C57
0.1/UFV
C59
*PAT/UFV
Q87
2SB1114T2ZKL
+5.6VA
R83
47K/J3
C87
0.1/UFV
R84
1500/J3
Q91
2SD1280-STTX
R91
47K/J3
C89
0.1/UFV
-5.6VA
R92
3300/J3
R99
47K/J3
Q92
2SB1218AQRTX
QR88
UN5213-TX
R44
*PAT/J3
R45
*PAT/J3
GND
TG1
EYF6CU
(7)
PB_CONT_L
+5.0V
[P1-6AB,7AB]
C32
*PAT/UFV
FL2
VLF0941C223T
C14
0.1/UFV
C15
16V10/ST
R22
*PAT/J3
+5VD
(7) [P2-1,2A]
+5VD
FL4
VLF0941C223T
C33
0.1/UFV
C34
16V10/ST
+5VDM
(7) [P2-14B]
+5VDM
+3.0V
[P1-9AB]
C11
*PAT/UFV
FL3
VLF0941C223T
C12
0.1/UFV
C13
16V10/ST
+3VD
(7) [P2-1,2B]
+3VD
+5VD
V
8
4
GND
IC11
*PAT

*PAT=PATTERN ONLY

Ref No.1~99 Series.

REVERSE SIDE
CAMERA SYNC 4/5, 5/5

VIDEO IF (2/7) SCHEMATIC DIAGRAM


Q101
2SB1218AQRTX
Q102
2SD1819AQRTX
Q117
*PAT
Q115
2SA1532-BCTX
Q116
2SD1819AQRTX
R103
4700/J3
R120
10K/J3
R511
*PAT/J3
R512
*PAT/J3
R513
*PAT/J3
R105
1500/J3
R107
1000/J3
R101
*PAT/J3
R505
0/J3
C114
0.01/UBV
IC103
AD817AR-R
VCC
VEE
AD_Y
R113
2200/J3
VR104
2K/VR5
Y_LEV
R510
*PAT/J3
Y_V
YV_GND
[P1-53A]
[P1-53B]
R106
1000/J3
IC101
TC4W53FUTL
R108
1000/J3
FL101
VLF1179-T
R104
5600/J3
R109
1000/J3
C137
47P/UV
R110
0/J3
R111
680/J3
L102
3R3U/LD
C179
*PAT/UBH
R135
*PAT/J3
R509
*PAT/J3
R121
75/RET
R107
2200/J3
R186
1500/J3
R188
6800/J3
C112
27P/UV
R112
0/J3
C113
3300P/UBV
R136
0/J3
C115
0.01/UBV
+5.6V
L113
*PAT/LC
-5.6V
L114
*PAT/LC
C111
0.01/UBV
R117
0/J3
R118
*PAT/J3
5C
3C
(3)
(1)
P101
VJP3358C012
GND
SG_Y
SG_Y_GND
SG_PB
SG_PB_GND
SG_PR
SG_PR_GND
SG_L
+5.6V
R102
0/J3
L104
100U/LC
+3.5V
R199
*PAT/J3
R116
4700/J3
C174
16V10/ST
C139
0.01/UBV
IC102
TC4W53FUTL
R125
2200/J3
R127
1500/J3
PB_TMG
R129
470/J3
VR107
2K/VR5
IC105
AD826AR-R
C145
0.01/UBV
C176
16V10/ST
PB_V
PBV_GND
[P1-55A]
[P1-55B]
R514
*PAT/J3
C180
*PAT/UV
R515
*PAT/J3
R162
*PAT/J3
R126
1000/J3
L106
82U/LD
L107
68U/LD
C133
7P/UV
C135
22P/UV
Q108
2SA1532-BCTX
C142
16V33/ST1
R134
2700/J3
AD_PB
VR108
2K/VR5
PB_LEV
R114
6800/J3
R115
1200/J3
Q103
2SB1218AQRTX
C132
39P/UV
C134
100P/UV
C136
27P/UV
R163
1000/J3
R128
1500/J3
C141
47P/UV
R130
22K/J3
R131
0/J3
R132
0/J3
L108
*PAT/LD
C147
*PAT/UBH
R145
*PAT/J3
R178
*PAT/J3
C177
16V10/ST
C146
0.01/UBV
Q107
2SB1218AQRTX
R122
75/RET
C143
56P/UV
R133
330/J3
C144
*PAT/UV
R179
0/J3
-5.6V
R502
*PAT/J3
L105
*PAT/LC
C125
16V10/ST
C131
0.01/UBV
-3.5V
R501
*PAT/J3
-5.6G
Q109
2SB1218AQRTX
R138
4700/J3
IC104
TC4W53FUTL
R147
2200/J3
R150
1500/J3
PR_TMG
R152
470/J3
VR111
2K/VR5
IC105
AD826AR-R
AD_PR
PR_V
PRV_GND
[P1-57A]
[P1-57B]
R516
*PAT/J3
C181
*PAT/UV
R517
*PAT/J3
R165
*PAT/J3
R149
1000/J3
L110
82U/LD
L111
68U/LD
Q114
2SA1532-BCTX
C173
16V33/ST1
R157
2700/J3
VR112
2K/VR5
PR_LEV
R160
6800/J3
R137
1200/J3
Q113
2SB1218AQRTX
C168
7P/UV
C170
22P/UV
C172
47P/UV
C148
*PAT/UBH
R146
*PAT/J3
C167
39P/UV
C169
100P/UV
C171
27P/UV
R166
1000/J3
R151
1500/J3
C166
0.01/UBV
R153
22K/J3
R154
0/J3
R155
0/J3
L112
*PAT/LD
R123
75/RET
C174
56P/UV
R156
330/J3
C175
*PAT/UV
-5F
(1,3)
C165
0.01/UBV
A
B
C
D
E
F
1
2
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4
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6
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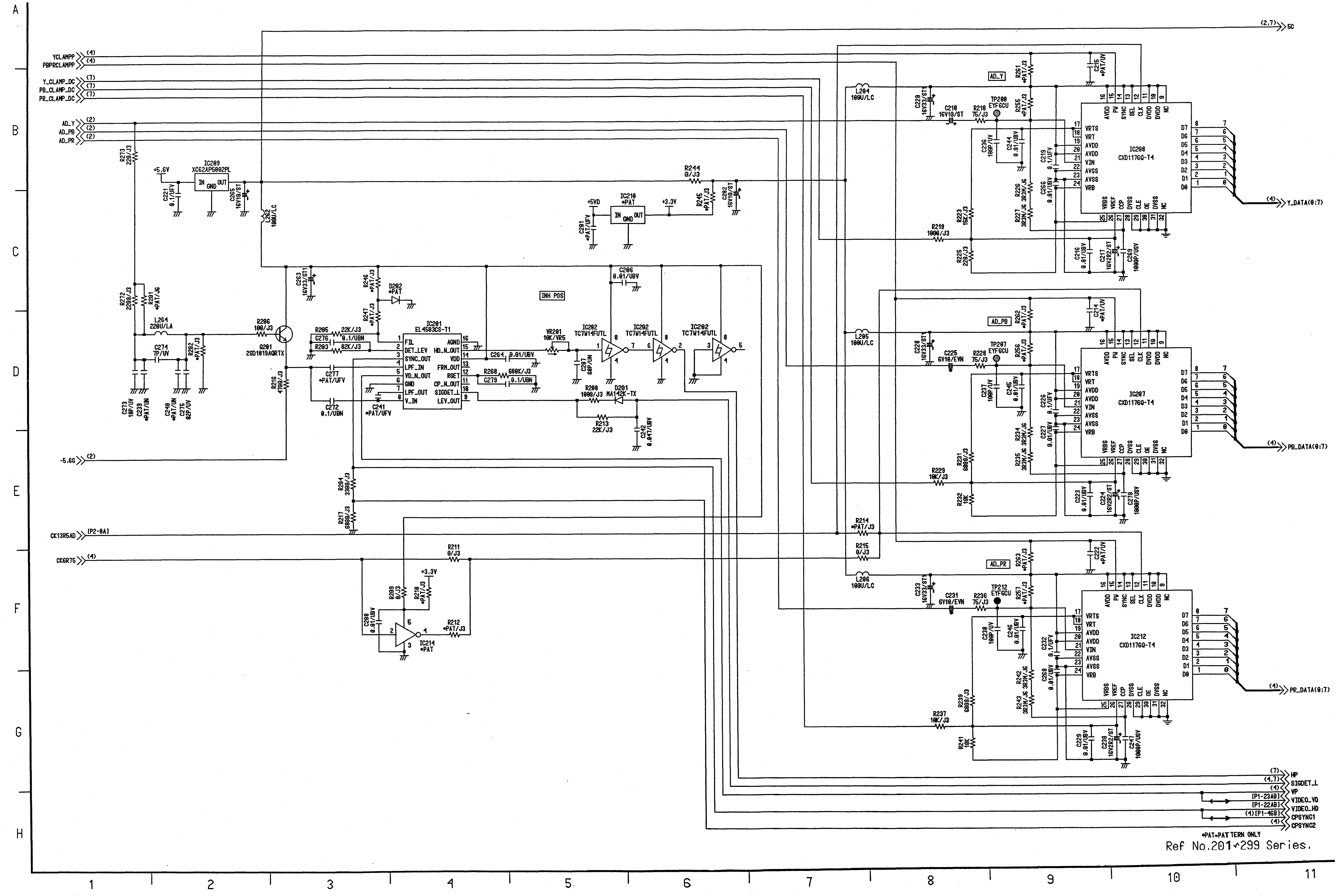
10

*PAT=PATTERN ONLY

Ref No.101~199,501~599 Series.

VIDEO IF (3/7) SCHEMATIC DIAGRAM



A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
YCLAMPP
PBPRCLAMPP
Y_CLAMP_DC
PB_CLAMP_DC
PR_CLAMP_DC
AD_Y
AD_PB
AD_PR
-5.6G
CK13R5AD
[P2-8A]
CK6R75
(2,7) 5C
IC209
XC62AP5002PL
IC210
*PAT
IC201
EL4583CS-T1
IC202
TC7W14FUTL
IC214
*PAT
Q201
2SD1819AQRTX
D201
MA142K-TX
D202
*PAT
INH POS
VR201
10K/VR5
+5.6V
+5VD
+3.3V
L262
100U/LC
L264
220U/LA
L204
100U/LC
L205
100U/LC
L206
100U/LC
R244
0/J3
R211
0/J3
R212
*PAT/J3
R214
*PAT/J3
R215
0/J3
AD_Y
AD_PB
AD_PR
TP208
EYF6CU
TP207
EYF6CU
TP212
EYF6CU
IC208
CXD1176Q-T4
IC207
CXD1176Q-T4
IC212
CXD1176Q-T4
VRTS
VRT
AVDD
VIN
AVSS
VRB
VRBS
VREF
CCP
DVSS
CLE
OE
NC
PW
SYNC
SEL
CLK
DVDD
D7
D6
D5
D4
D3
D2
D1
D0
(4) Y_DATA(0:7)
(4) PB_DATA(0:7)
(4) PR_DATA(0:7)
(7) HP
(4,7) SIGDET_L
(4) VP
[P1-23AB] VIDEO_VD
[P1-22AB] VIDEO_HD
(4) [P1-46B] CPSYNC1
(4) CPSYNC2
FIL
DET_LEV
SYNC_OUT
LPF_IN
VD_N_OUT
GND
LPF_OUT
V_IN
AGND
HD_N_OUT
VDD
FRM_OUT
RSET
CP_N_OUT
SIGDET_L
LEV_OUT

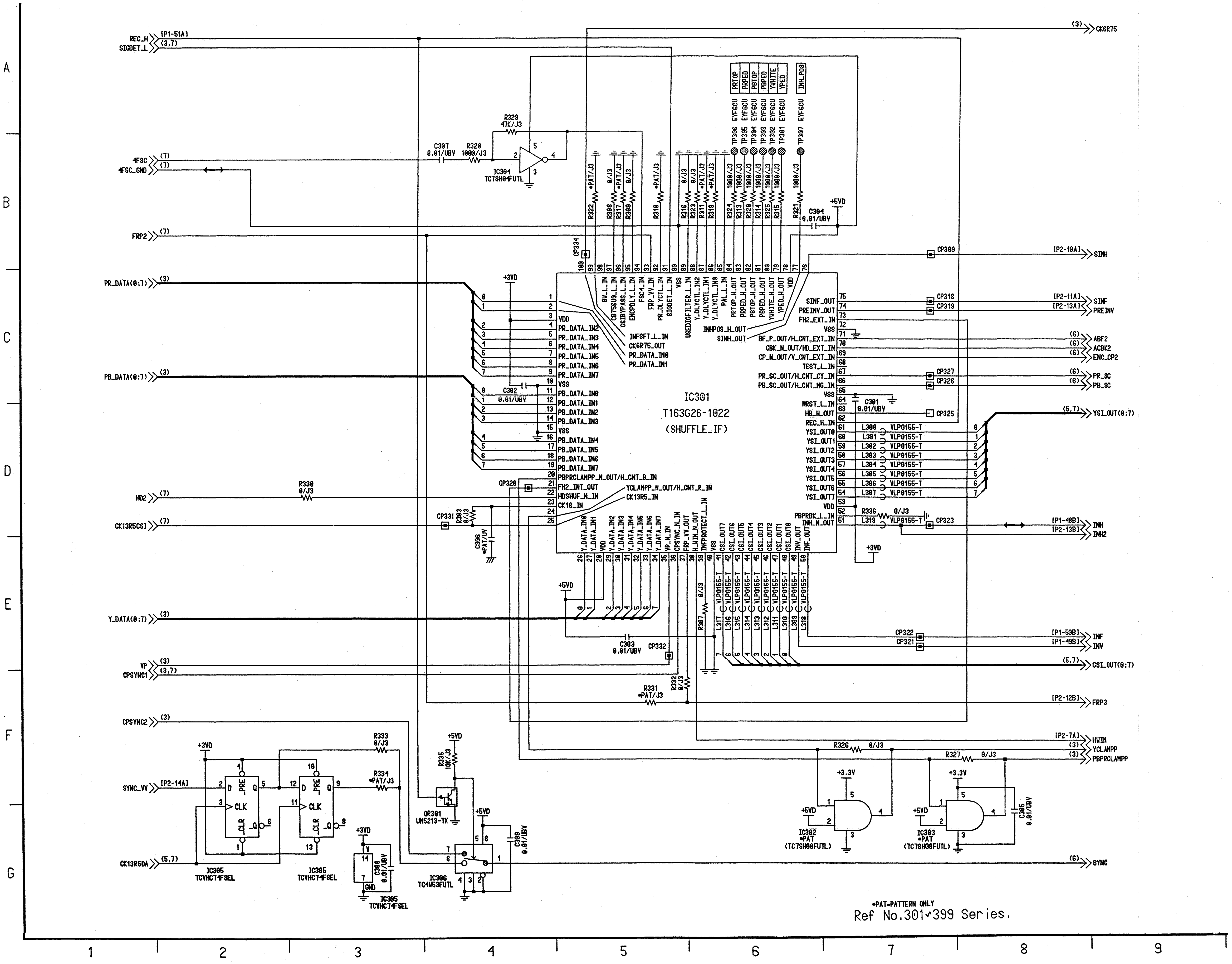
*PAT=PATTERN ONLY

Ref No.201~299 Series.

REVERSE SIDE

VIDEO IF 2/7

VIDEO IF (4/7) SCHEMATIC DIAGRAM


IC301
T163G26-1022
(SHUFFLE_IF)
REC_H
SIGDET_L
4FSC
4FSC_GND
FRP2
PR_DATA(0:7)
PB_DATA(0:7)
HD2
CK13R5CSI
Y_DATA(0:7)
VP
CPSYNC1
CPSYNC2
SYNC_VV
CK13R5DA
CK6R75
SINH
SINF
PREINV
ABF2
ACBK2
ENC_CP2
PR_SC
PB_SC
YSI_OUT(0:7)
INH
INH2
INF
INV
CSI_OUT(0:7)
FRP3
HWIN
YCLAMPP
PBPRCLAMPP
SYNC
IC304
TC7SH04FUTL
IC305
TCVHC74FSEL
IC306
TC4W53FUTL
QR301
UN5213-TX
IC302
*PAT
(TC7SH08FUTL)
IC303
*PAT
(TC7SH08FUTL)
+3VD
+5VD
+3.3V
A
B
C
D
E
F
G
1
2
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4
5
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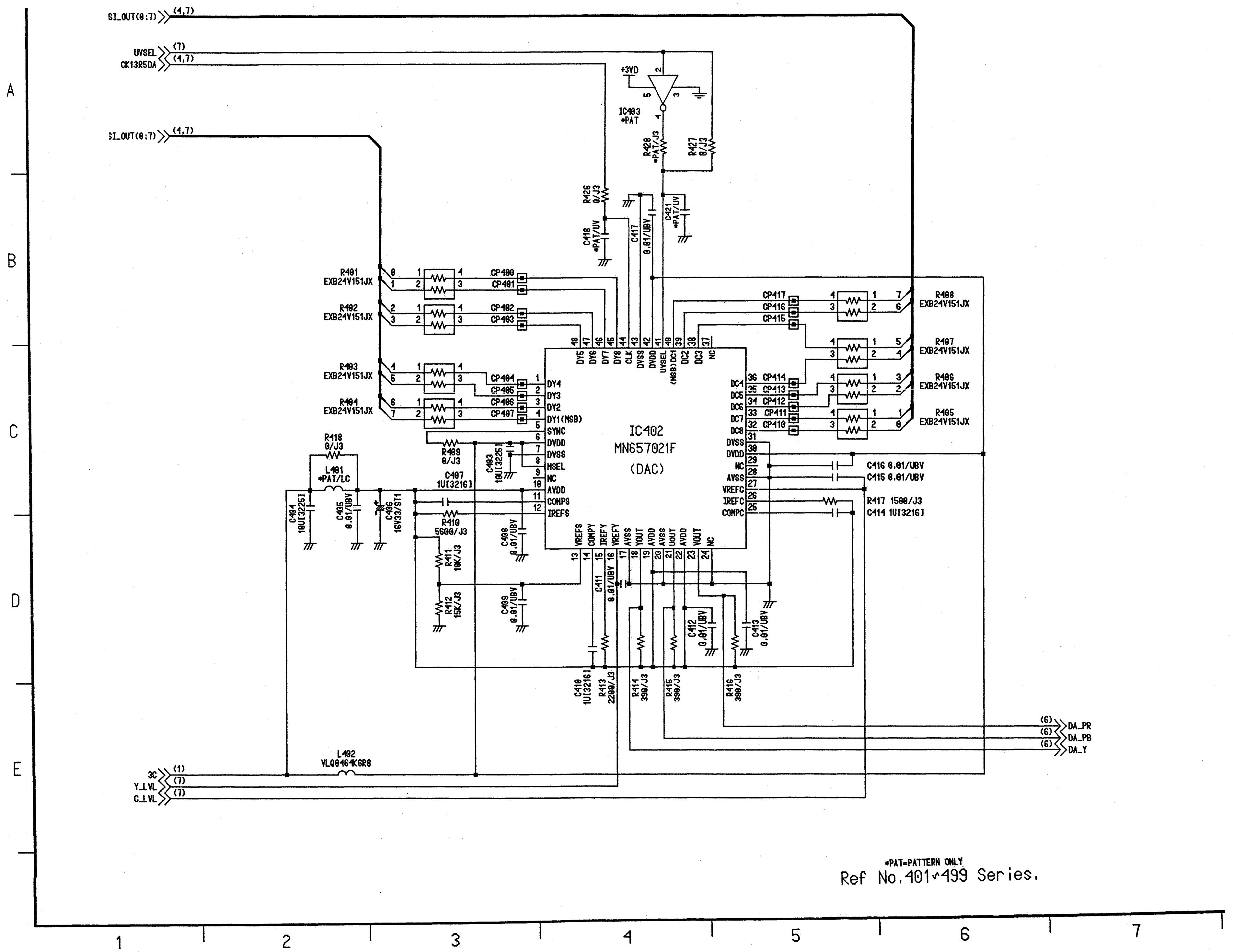
7
8
9

*PAT=PATTERN ONLY

Ref No.301~399 Series.

VIDEO IF (5/7) SCHEMATIC DIAGRAM


A
B
C
D
E
SI_OUT(0:7) (4,7)
UVSEL (7)
CK13R5DA (4,7)
SI_OUT(0:7) (4,7)
+3VD
IC403
*PAT
R428
*PAT/J3
R427
0/J3
R426
0/J3
C418
*PAT/UV
C417
0.01/UBV
C421
*PAT/UV
R401
EXB24V151JX
R402
EXB24V151JX
R403
EXB24V151JX
R404
EXB24V151JX
CP400
CP401
CP402
CP403
CP404
CP405
CP406
CP407
R408
EXB24V151JX
R407
EXB24V151JX
R406
EXB24V151JX
R405
EXB24V151JX
CP417
CP416
CP415
CP414
CP413
CP412
CP411
CP410
IC402
MN657021F
(DAC)
DY4
DY3
DY2
DY1(MSB)
SYNC
DVDD
DVSS
MSEL
NC
AVDD
COMPS
IREFS
DY5
DY6
DY7
DY8
CLK
DVSS
DVDD
UVSEL
(MSB)DC1
DC2
DC3
NC
DC4
DC5
DC6
DC7
DC8
DVSS
DVDD
NC
AVSS
VREFC
IREFC
COMPC
VREFS
COMPY
IREFY
VREFY
AVSS
YOUT
AVDD
AVSS
UOUT
AVDD
VOUT
NC
R418
0/J3
L401
*PAT/LC
C404
10U[3225]
C405
0.01/UBV
C406
16V33/ST1
R409
0/J3
C403
10U[3225]
C407
1U[3216]
R410
5600/J3
C408
0.01/UBV
R411
10K/J3
R412
15K/J3
C409
0.01/UBV
C411
0.01/UBV
C412
0.01/UBV
C413
0.01/UBV
C410
1U[3216]
R413
2200/J3
R414
390/J3
R415
390/J3
R416
390/J3
C416 0.01/UBV
C415 0.01/UBV
R417 1500/J3
C414 1U[3216]
(6) DA_PR
(6) DA_PB
(6) DA_Y
L402
VLQ0464K6R8
3C (1)
Y_LVL (7)
C_LVL (7)
*PAT=PATTERN ONLY
Ref No.401~499 Series.
1
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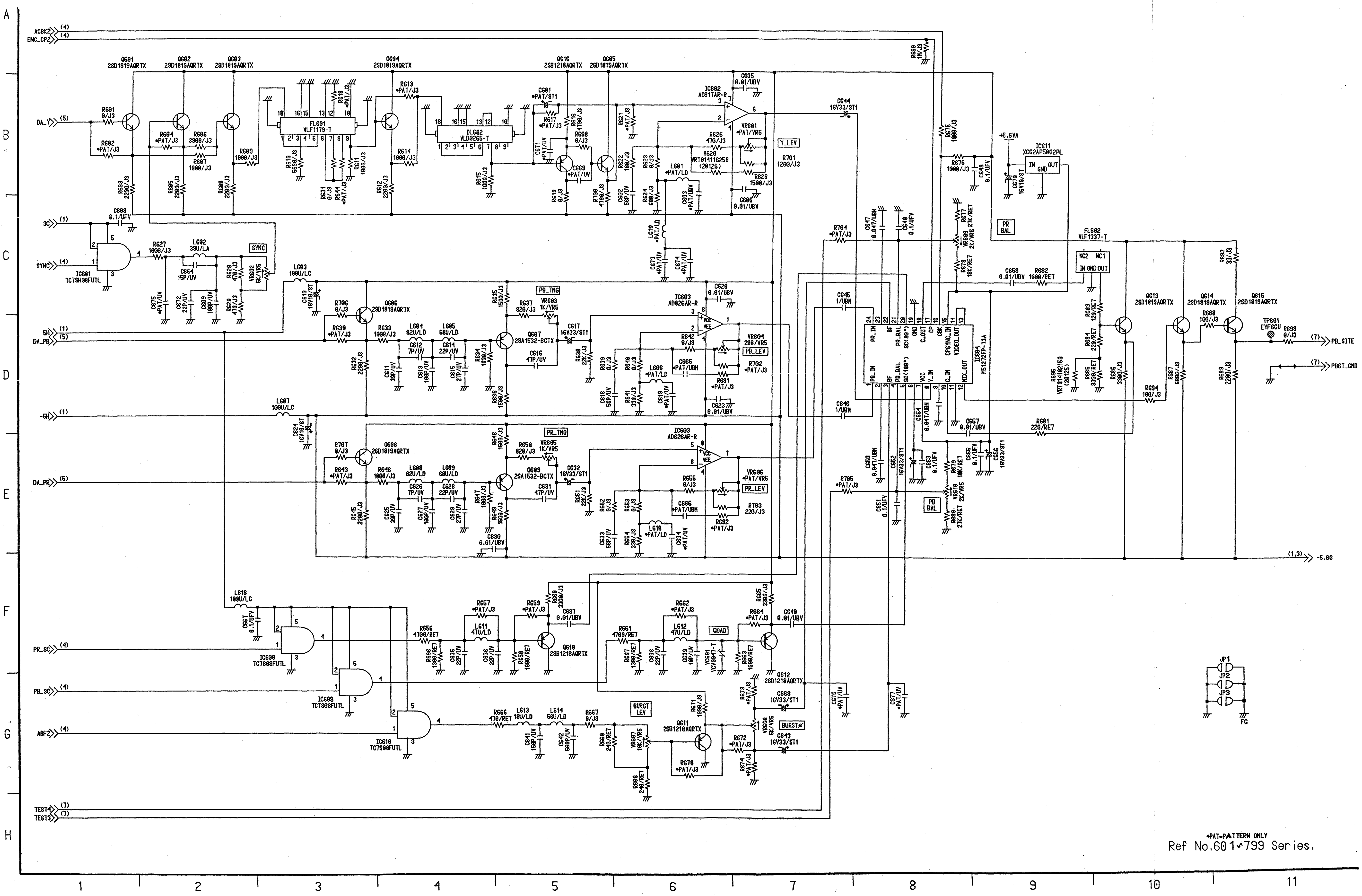
7

REVERSE SIDE

VIDEO IF 4/7

VIDEO IF (6/7) SCHEMATIC DIAGRAM


ACBK2 (4)
ENC_CP2 (4)
DA_Y (5)
3C (1)
SYNC (4)
5H (1)
DA_PB (5)
-5H (1)
DA_PR (5)
PR_SC (4)
PB_SC (4)
ABF2 (4)
TEST4 (7)
TEST3 (7)
Q601 2SD1819AQRTX
Q602 2SD1819AQRTX
Q603 2SD1819AQRTX
Q604 2SD1819AQRTX
Q616 2SB1218AQRTX
Q605 2SD1819AQRTX
FL601 VLF1179-T
DL602 VLD9265-T
IC602 AD817AR-R
IC601 TC7SH08FUTL
Q606 2SD1819AQRTX
Q607 2SA1532-BCTX
IC603 AD826AR-R
Q608 2SD1819AQRTX
Q609 2SA1532-BCTX
IC608 TC7S08FUTL
IC609 TC7S08FUTL
IC610 TC7S08FUTL
Q610 2SB1218AQRTX
Q611 2SB1218AQRTX
Q612 2SB1218AQRTX
IC604 M51272FP-73A
IC611 XC62AP5002PL
FL602 VLF1337-T
Q613 2SD1819AQRTX
Q614 2SD1819AQRTX
Q615 2SD1819AQRTX
TP601 EYF6CU
+5.6VA
Y_LEV
SYNC
PB_TMG
PB_LEV
PR_TMG
PR_LEV
QUAD
BURST LEV
BURSTø
PR BAL
PB BAL
(7) PB_SITE
(7) PBST_GND
(1,3) -5.6G
JP1
JP2
JP3
FG
A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
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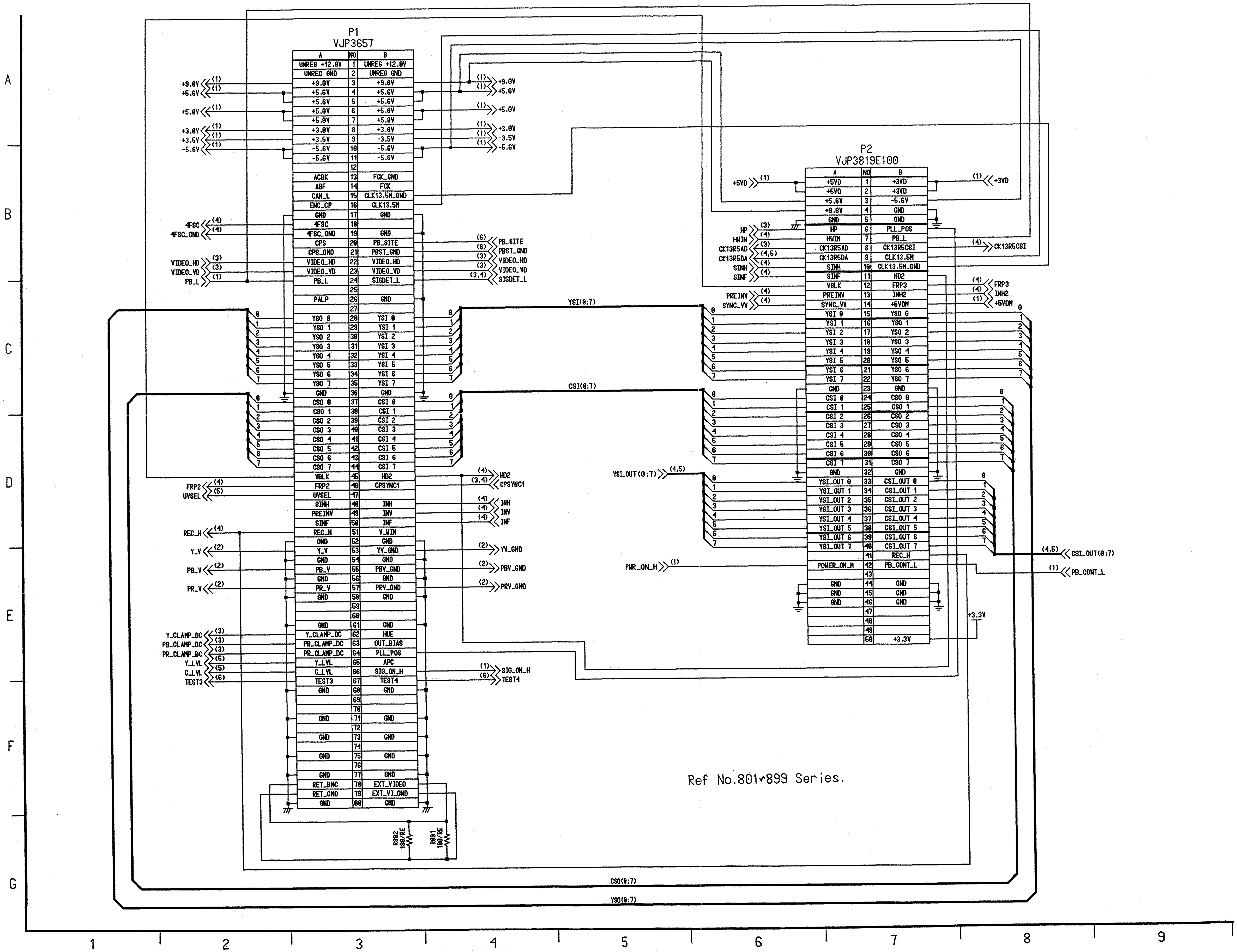
9
10
11

*PAT=PATTERN ONLY

Ref No.601~799 Series.

VIDEO IF (7/7) CONNECTOR SCHEMATIC DIAGRAM


P1
VJP3657
A NO B
UNREG +12.0V 1 UNREG +12.0V
UNREG GND 2 UNREG GND
+9.0V 3 +9.0V
+5.6V 4 +5.6V
+5.6V 5 +5.6V
+5.0V 6 +5.0V
+5.0V 7 +5.0V
+3.0V 8 +3.0V
+3.5V 9 -3.5V
-5.6V 10 -5.6V
-5.6V 11 -5.6V
12
ACBK 13 FCK_GND
ABF 14 FCK
CAM_L 15 CLK13.5M_GND
ENC_CP 16 CLK13.5M
GND 17 GND
4FSC 18
4FSC_GND 19 GND
CPS 20 PB_SITE
CPS_GND 21 PBST_GND
VIDEO_HD 22 VIDEO_HD
VIDEO_VD 23 VIDEO_VD
PB_L 24 SIGDET_L
25
PALP 26 GND
27
YSO 0 28 YSI 0
YSO 1 29 YSI 1
YSO 2 30 YSI 2
YSO 3 31 YSI 3
YSO 4 32 YSI 4
YSO 5 33 YSI 5
YSO 6 34 YSI 6
YSO 7 35 YSI 7
GND 36 GND
CSO 0 37 CSI 0
CSO 1 38 CSI 1
CSO 2 39 CSI 2
CSO 3 40 CSI 3
CSO 4 41 CSI 4
CSO 5 42 CSI 5
CSO 6 43 CSI 6
CSO 7 44 CSI 7
VBLK 45 HD2
FRP2 46 CPSYNC1
UVSEL 47
SINH 48 INH
PREINV 49 INV
SINF 50 INF
REC_H 51 V_MIN
GND 52 GND
Y_V 53 YV_GND
GND 54 GND
PB_V 55 PBV_GND
GND 56 GND
PR_V 57 PRV_GND
GND 58 GND
59
60
GND 61 GND
Y_CLAMP_DC 62 HUE
PB_CLAMP_DC 63 OUT_BIAS
PR_CLAMP_DC 64 PLL_POS
Y_LVL 65 APC
C_LVL 66 SIG_ON_H
TEST3 67 TEST4
GND 68 GND
69
70
GND 71 GND
72
GND 73 GND
74
GND 75 GND
76
GND 77 GND
RET_BNC 78 EXT_VIDEO
RET_GND 79 EXT_VI_GND
GND 80 GND
+9.0V (1)
+5.6V (1)
+5.0V (1)
+3.0V (1)
+3.5V (1)
-5.6V (1)
4FSC (4)
4FSC_GND (4)
VIDEO_HD (3)
VIDEO_VD (3)
PB_L (1)
FRP2 (4)
UVSEL (5)
REC_H (4)
Y_V (2)
PB_V (2)
PR_V (2)
Y_CLAMP_DC (3)
PB_CLAMP_DC (3)
PR_CLAMP_DC (3)
Y_LVL (5)
C_LVL (5)
TEST3 (6)
(1) +9.0V
(1) +5.6V
(1) +5.0V
(1) +3.0V
(1) -3.5V
(1) -5.6V
(6) PB_SITE
(6) PBST_GND
(3) VIDEO_HD
(3) VIDEO_VD
(3,4) SIGDET_L
(4) HD2
(3,4) CPSYNC1
(4) INH
(4) INV
(4) INF
(2) YV_GND
(2) PBV_GND
(2) PRV_GND
(1) SIG_ON_H
(6) TEST4
R802 180/RE
R801 180/RE
YSI(0:7)
CSI(0:7)
YSI_OUT(0:7) (4,5)
PWR_ON_H (1)
CSO(0:7)
YSO(0:7)
P2
VJP3819E100
A NO B
+5VD 1 +3VD
+5VD 2 +3VD
+5.6V 3 -5.6V
+9.0V 4 GND
GND 5 GND
HP 6 PLL_POS
HWIN 7 PB_L
CK13R5AD 8 CK13R5CSI
CK13R5DA 9 CLK13.5M
SINH 10 CLK13.5M_GND
SINF 11 HD2
VBLK 12 FRP3
PREINV 13 INH2
SYNC_VV 14 +5VDM
YSI 0 15 YSO 0
YSI 1 16 YSO 1
YSI 2 17 YSO 2
YSI 3 18 YSO 3
YSI 4 19 YSO 4
YSI 5 20 YSO 5
YSI 6 21 YSO 6
YSI 7 22 YSO 7
GND 23 GND
CSI 0 24 CSO 0
CSI 1 25 CSO 1
CSI 2 26 CSO 2
CSI 3 27 CSO 3
CSI 4 28 CSO 4
CSI 5 29 CSO 5
CSI 6 30 CSO 6
CSI 7 31 CSO 7
GND 32 GND
YSI_OUT 0 33 CSI_OUT 0
YSI_OUT 1 34 CSI_OUT 1
YSI_OUT 2 35 CSI_OUT 2
YSI_OUT 3 36 CSI_OUT 3
YSI_OUT 4 37 CSI_OUT 4
YSI_OUT 5 38 CSI_OUT 5
YSI_OUT 6 39 CSI_OUT 6
YSI_OUT 7 40 CSI_OUT 7
41 REC_H
POWER_ON_H 42 PB_CONT_L
43
GND 44 GND
GND 45 GND
GND 46 GND
47
48
49
50 +3.3V
+5VD (1)
HP (3)
HWIN (4)
CK13R5AD (3)
CK13R5DA (4,5)
SINH (4)
SINF (4)
PREINV (4)
SYNC_VV (4)
(1) +3VD
(4) CK13R5CSI
(4) FRP3
(4) INH2
(1) +5VDM
(4,5) CSI_OUT(0:7)
(1) PB_CONT_L
+3.3V
Ref No.801~899 Series.
A
B
C
D
E
F
G
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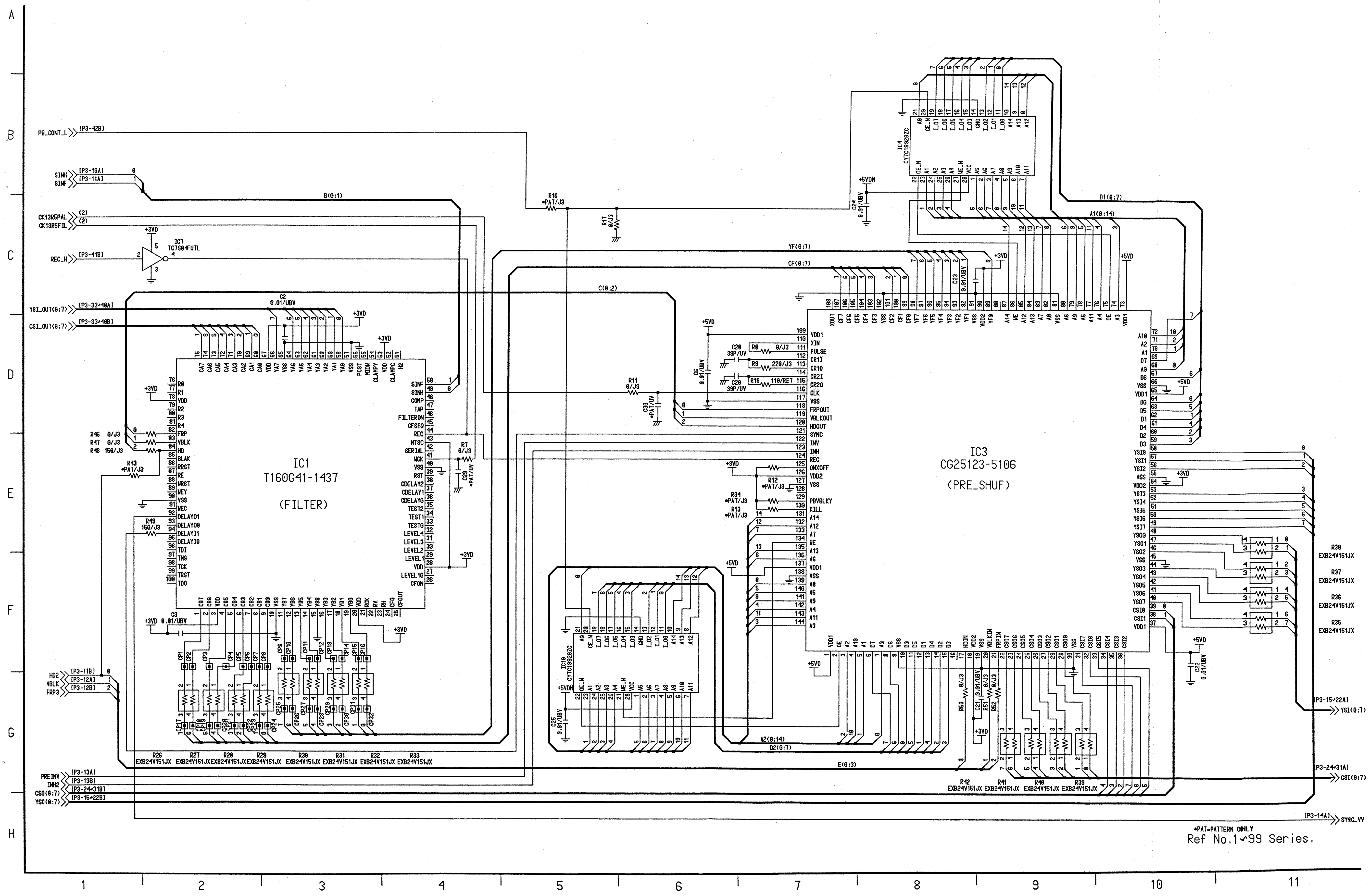
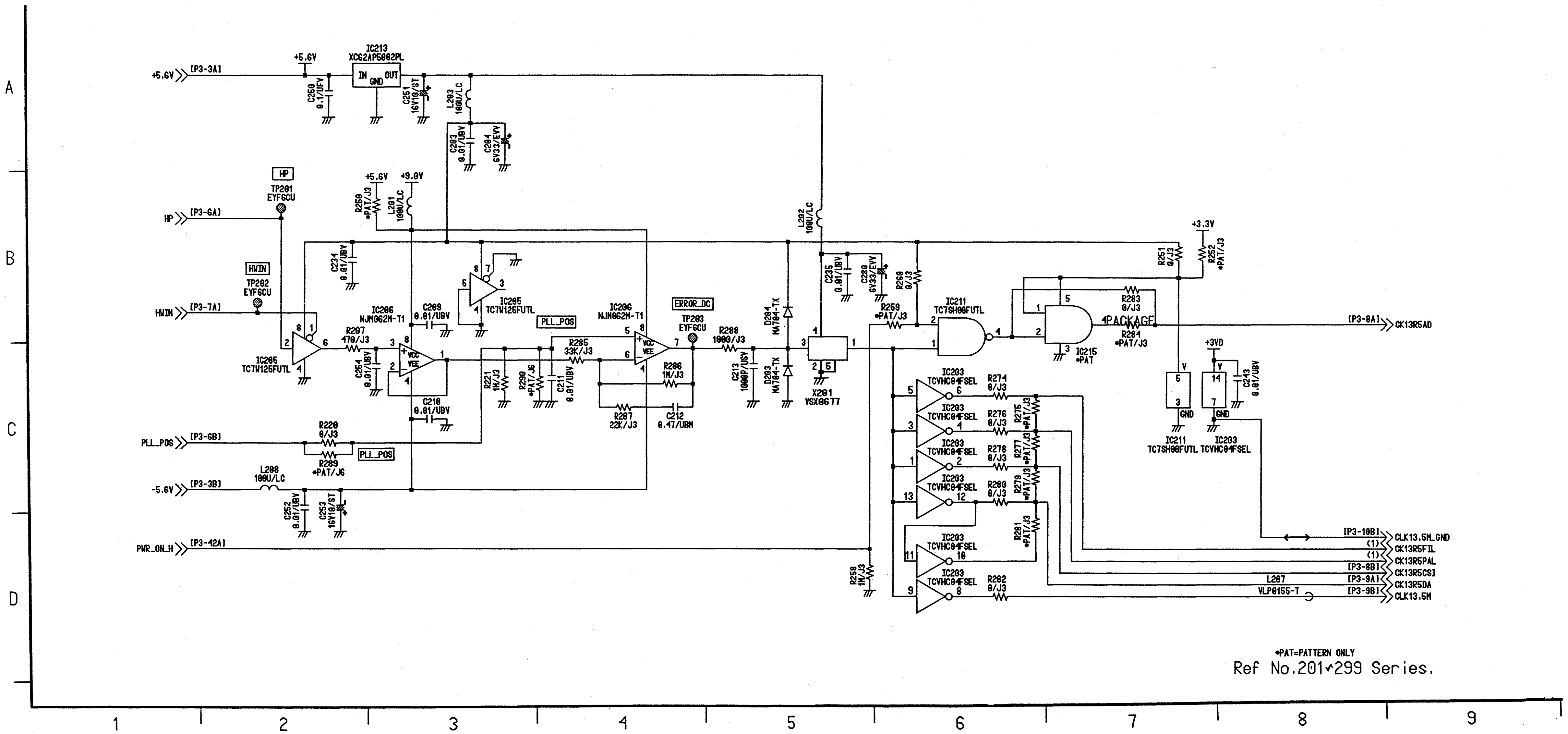
REVERSE SIDE

VIDEO IF 6/7

VIDEO IF SUB (1/3) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
PB_CONT_L [P3-42B]
SINH [P3-10A]
SINF [P3-11A]
CK13R5PAL (2)
CK13R5FIL (2)
REC_H [P3-41B]
IC7 TC7S04FUTL
+3VD
YSI_OUT(0:7) [P3-33+40A]
CSI_OUT(0:7) [P3-33+40B]
B(0:1)
C(0:2)
YF(0:7)
CF(0:7)
D1(0:7)
A1(0:14)
A2(0:14)
D2(0:7)
E(0:3)
R16 *PAT/J3
R17 0/J3
C24 0.01/UBY
+5VDM
IC4 CY7C199202C
C2 0.01/UBV
IC1
T160G41-1437
(FILTER)
R46 0/J3
R47 0/J3
R48 150/J3
R43 *PAT/J3
R49 150/J3
R7 0/J3
C29 *PAT/UV
C3 0.01/UBV
R11 0/J3
C30 *PAT/UV
C5 0.01/UBV
C28 39P/UV
C20 39P/UV
R8 0/J3
R9 220/J3
R10 110/RE7
C23 0.01/UBV
IC3
CG25123-5106
(PRE_SHUF)
R12 *PAT/J3
R34 *PAT/J3
R13 *PAT/J3
+5VD
IC10 CY7C199202C
C25 0.01/UBV
C22 0.01/UBV
R50 0/J3
R51 0/J3
R52 0/J3
C21 0.01/UBV
HD2 [P3-11B]
VBLK [P3-12A]
FRP3 [P3-12B]
PREINV [P3-13A]
INH2 [P3-13B]
CSO(0:7) [P3-24+31B]
YSO(0:7) [P3-15+22B]
R26 EXB24V151JX
R27 EXB24V151JX
R28 EXB24V151JX
R29 EXB24V151JX
R30 EXB24V151JX
R31 EXB24V151JX
R32 EXB24V151JX
R33 EXB24V151JX
R35 EXB24V151JX
R36 EXB24V151JX
R37 EXB24V151JX
R38 EXB24V151JX
R39 EXB24V151JX
R40 EXB24V151JX
R41 EXB24V151JX
R42 EXB24V151JX
[P3-15+22A] YSI(0:7)
[P3-24+31A] CSI(0:7)
[P3-14A] SYNC_VV
*PAT=PATTERN ONLY
Ref No.1~99 Series.

VIDEO IF SUB (2/3) SCHEMATIC DIAGRAM


A
B
C
D
1
2
3
4
5
6
7
8
9
+5.6V
[P3-3A]
+5.6V
IC213
XC62AP5002PL
IN
GND
OUT
C250
0.1/UFV
C251
16V10/ST
L203
100U/LC
C203
0.01/UBV
C204
6V33/EVV
HP
[P3-6A]
HP
TP201
EYF6CU
HWIN
[P3-7A]
HWIN
TP202
EYF6CU
+5.6V
+9.0V
R250
*PAT/J3
L201
100U/LC
C234
0.01/UBV
IC205
TC7W125FUTL
IC206
NJM062M-T1
R207
470/J3
C254
0.01/UBV
C209
0.01/UBV
C210
0.01/UBV
PLL_POS
R221
1M/J3
R290
*PAT/J6
C211
0.01/UBV
R285
33K/J3
R286
1M/J3
R287
22K/J3
C212
0.47/UBM
ERROR_DC
TP203
EYF6CU
R288
1000/J3
C213
1000P/USV
D204
MA704-TX
D203
MA704-TX
PLL_POS
[P3-6B]
R220
0/J3
R289
*PAT/J6
PLL_POS
-5.6V
[P3-3B]
L208
100U/LC
C252
0.01/UBV
C253
16V10/ST
PWR_ON_H
[P3-42A]
L202
100U/LC
C235
0.01/UBV
C280
6V33/EVV
R260
0/J3
R259
*PAT/J3
X201
VSX0677
IC211
TC7SH00FUTL
IC215
*PAT
R283
0/J3
R284
*PAT/J3
4PACKAGE
+3.3V
R251
0/J3
R252
*PAT/J3
[P3-8A]
CK13R5AD
+3VD
C243
0.01/UBV
GND
IC211
TC7SH00FUTL
IC203
TCVHC04FSEL
IC203
TCVHC04FSEL
R274
0/J3
R275
*PAT/J3
R276
0/J3
R277
*PAT/J3
R278
0/J3
R279
*PAT/J3
R280
0/J3
R281
*PAT/J3
R282
0/J3
R258
1M/J3
L207
VLP0155-T
[P3-10B]
CLK13.5M_GND
(1)
CK13R5FIL
(1)
CK13R5PAL
[P3-8B]
CK13R5CSI
[P3-9A]
CK13R5DA
[P3-9B]
CLK13.5M

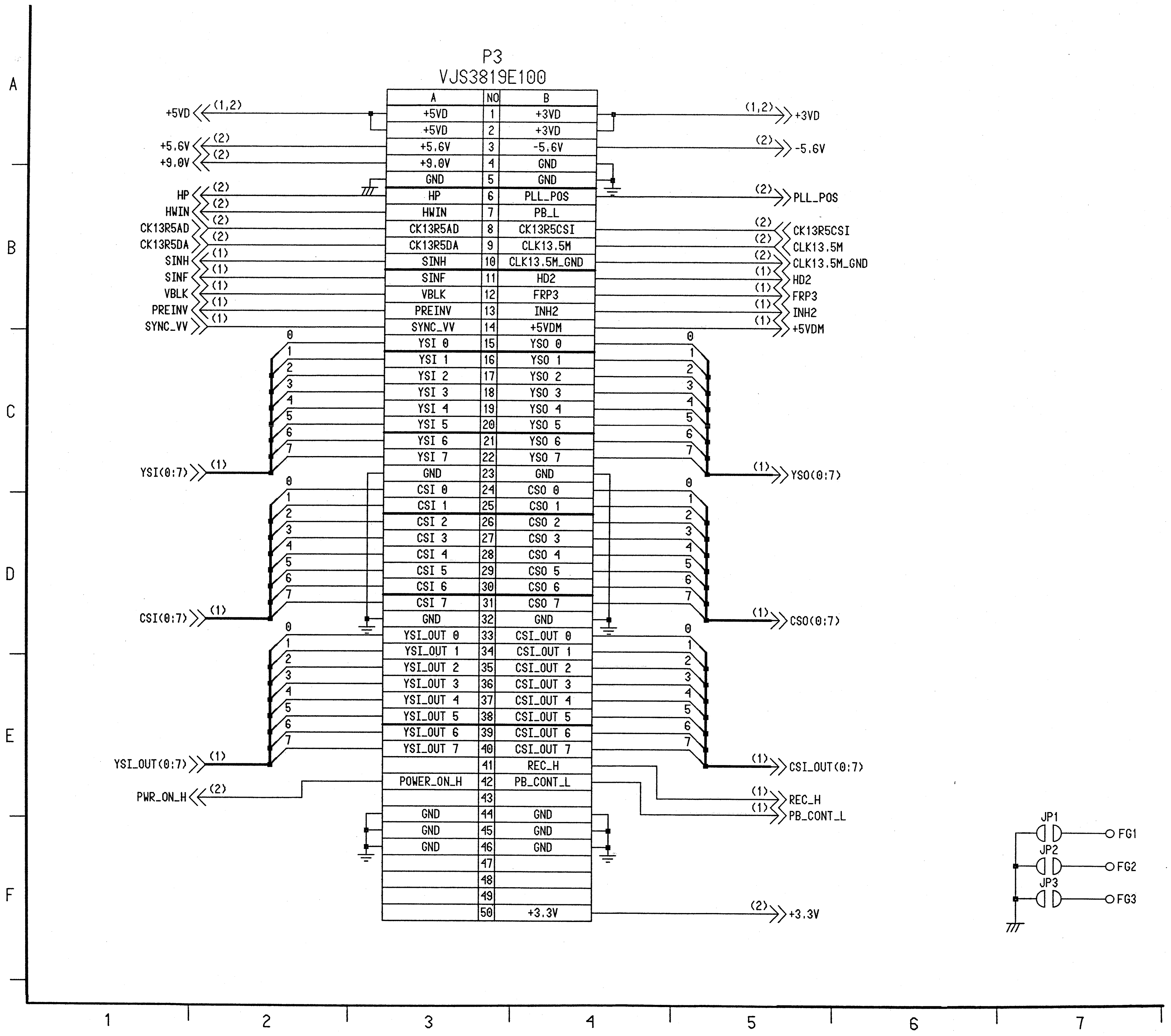
*PAT=PATTERN ONLY

Ref No.201~299 Series.

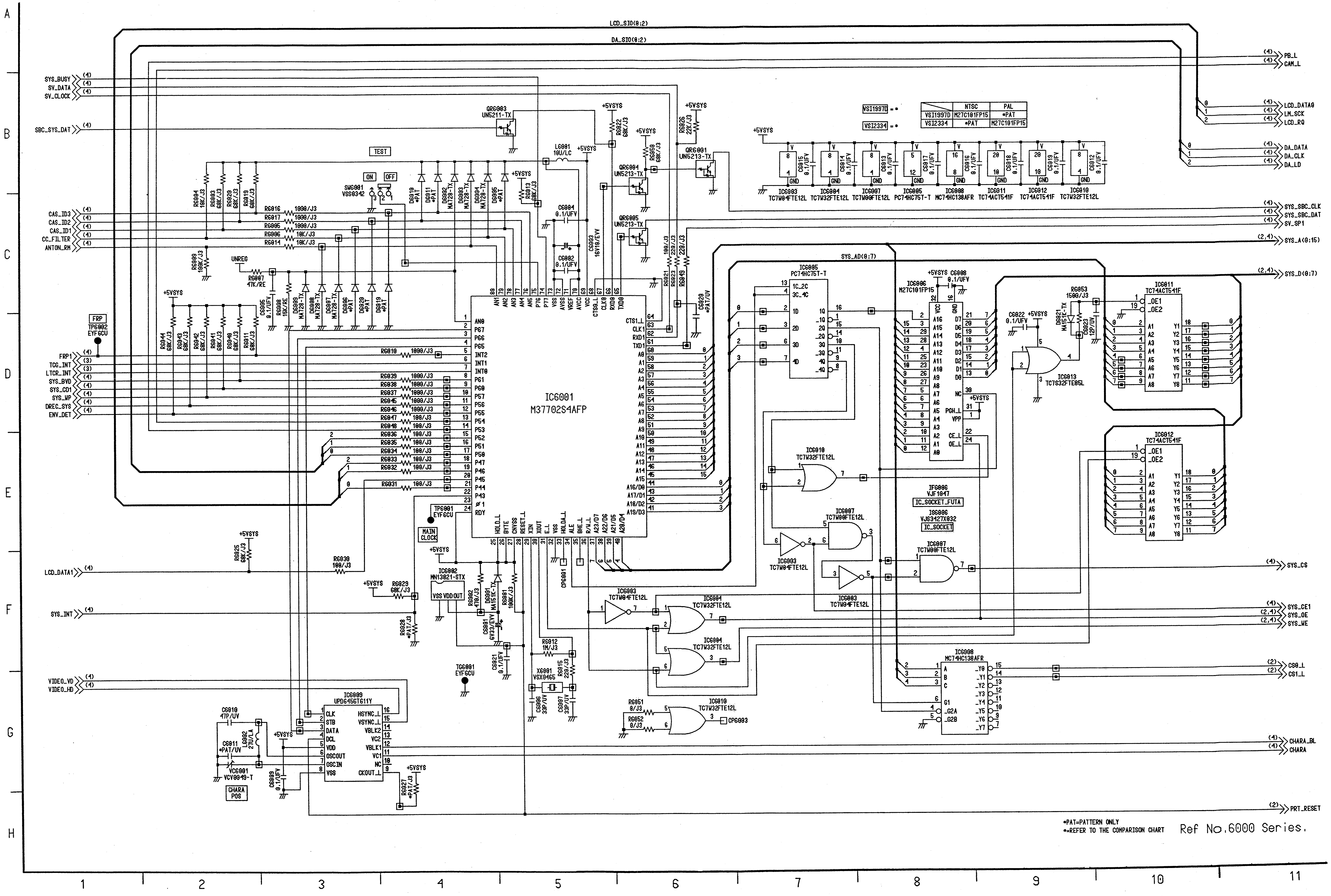
REVERSE SIDE

VIDEO IF SUB 1/3

VIDEO IF SUB (3/3) CONNECTOR SCHEMATIC DIAGRAM


P3
VJS3819E100
A | NO | B
+5VD | 1 | +3VD
+5VD | 2 | +3VD
+5.6V | 3 | -5.6V
+9.0V | 4 | GND
GND | 5 | GND
HP | 6 | PLL_POS
HWIN | 7 | PB_L
CK13R5AD | 8 | CK13R5CSI
CK13R5DA | 9 | CLK13.5M
SINH | 10 | CLK13.5M_GND
SINF | 11 | HD2
VBLK | 12 | FRP3
PREINV | 13 | INH2
SYNC_VV | 14 | +5VDM
YSI 0 | 15 | YSO 0
YSI 1 | 16 | YSO 1
YSI 2 | 17 | YSO 2
YSI 3 | 18 | YSO 3
YSI 4 | 19 | YSO 4
YSI 5 | 20 | YSO 5
YSI 6 | 21 | YSO 6
YSI 7 | 22 | YSO 7
GND | 23 | GND
CSI 0 | 24 | CSO 0
CSI 1 | 25 | CSO 1
CSI 2 | 26 | CSO 2
CSI 3 | 27 | CSO 3
CSI 4 | 28 | CSO 4
CSI 5 | 29 | CSO 5
CSI 6 | 30 | CSO 6
CSI 7 | 31 | CSO 7
GND | 32 | GND
YSI_OUT 0 | 33 | CSI_OUT 0
YSI_OUT 1 | 34 | CSI_OUT 1
YSI_OUT 2 | 35 | CSI_OUT 2
YSI_OUT 3 | 36 | CSI_OUT 3
YSI_OUT 4 | 37 | CSI_OUT 4
YSI_OUT 5 | 38 | CSI_OUT 5
YSI_OUT 6 | 39 | CSI_OUT 6
YSI_OUT 7 | 40 | CSI_OUT 7
41 | REC_H
POWER_ON_H | 42 | PB_CONT_L
43
GND | 44 | GND
GND | 45 | GND
GND | 46 | GND
47
48
49
50 | +3.3V
+5VD (1,2)
+5.6V (2)
+9.0V (2)
HP (2)
HWIN (2)
CK13R5AD (2)
CK13R5DA (2)
SINH (1)
SINF (1)
VBLK (1)
PREINV (1)
SYNC_VV (1)
YSI(0:7) (1)
CSI(0:7) (1)
YSI_OUT(0:7) (1)
PWR_ON_H (2)
(1,2) +3VD
(2) -5.6V
(2) PLL_POS
(2) CK13R5CSI
(2) CLK13.5M
(2) CLK13.5M_GND
(1) HD2
(1) FRP3
(1) INH2
(1) +5VDM
(1) YSO(0:7)
(1) CSO(0:7)
(1) CSI_OUT(0:7)
(1) REC_H
(1) PB_CONT_L
(2) +3.3V
0 1 2 3 4 5 6 7
JP1
FG1
JP2
FG2
JP3
FG3
A
B
C
D
E
F
1
2
3
4
5
6
7

VTR SYSCON (1/5) SCHEMATIC DIAGRAM



LCD_SIO(0:2)
DA_SIO(0:2)
SYS_BUSY
SV_DATA
SV_CLOCK
SBC_SYS_DAT
CAS_ID3
CAS_ID2
CAS_ID1
CC_FILTER
ANTON_RM
FRP
TP6002
EYF6CU
FRP1
TCO_INT
LTCR_INT
SYS_BVD
SYS_CD1
SYS_WP
DREC_SYS
ENV_DET
LCD_DATA1
SYS_INT
VIDEO_VD
VIDEO_HD
PB_L
CAM_L
LCD_DATA0
LM_SCK
LCD_RQ
DA_DATA
DA_CLK
DA_LD
SYS_SBC_CLK
SYS_SBC_DAT
SV_SP1
SYS_A(0:15)
SYS_D(0:7)
SYS_AD(0:7)
SYS_CS
SYS_CE1
SYS_OE
SYS_WE
CS0_L
CS1_L
CHARA_BL
CHARA
PRT_RESET
IC6001
M37702S4AFP
IC6005
PC74HC75T-T
IC6006
M27C101FP15
IC6011
TC74ACT541F
IC6012
TC74ACT541F
IC6010
TC7W32FTE12L
IC6007
TC7W00FTE12L
IC6003
TC7W04FTE12L
IC6004
TC7W32FTE12L
IC6013
TC7S32FTE85L
IC6008
MC74HC138AFR
IC6009
UPD6456TG11Y
IC6002
MN13821-STX
QR6003
UN5211-TX
QR6001
UN5213-TX
QR6004
UN5213-TX
QR6005
UN5213-TX
SW6001
VSS0342
TEST
ON
OFF
MAIN CLOCK
CHARA POS
IFG006
VJF1047
IC_SOCKET_FUTA
IS6006
VJS3427X032
IC_SOCKET
VSI1997D
VSI2334
NTSC
PAL
M27C101FP15
*PAT
X6001
VSX0465
VC6001
VCV0049-T
+5VSYS
UNREG
*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART
Ref No.6000 Series.
A
B
C
D
E
F
G
H
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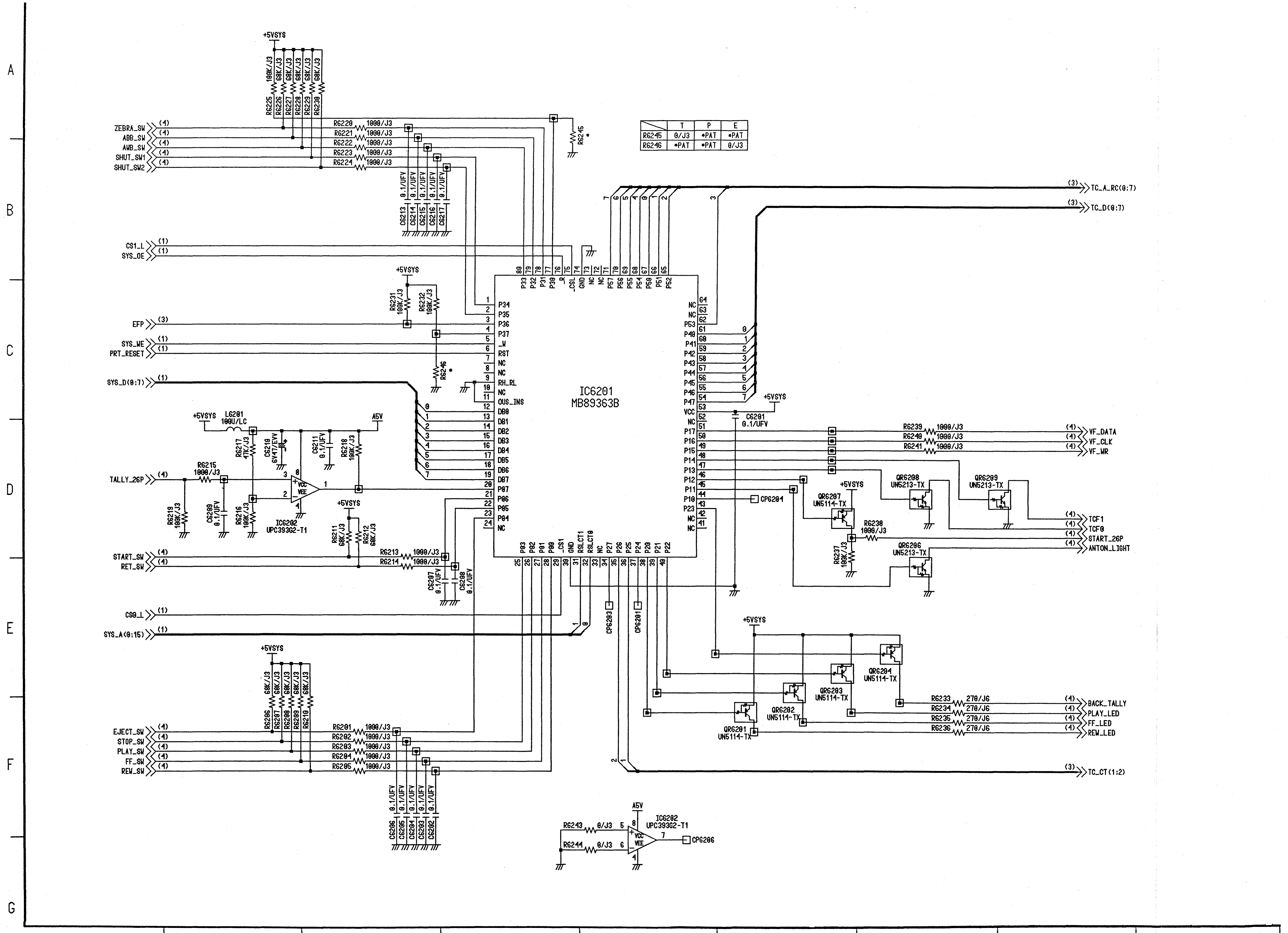
11

REVERSE SIDE

VIDEO IF SUB 3/3

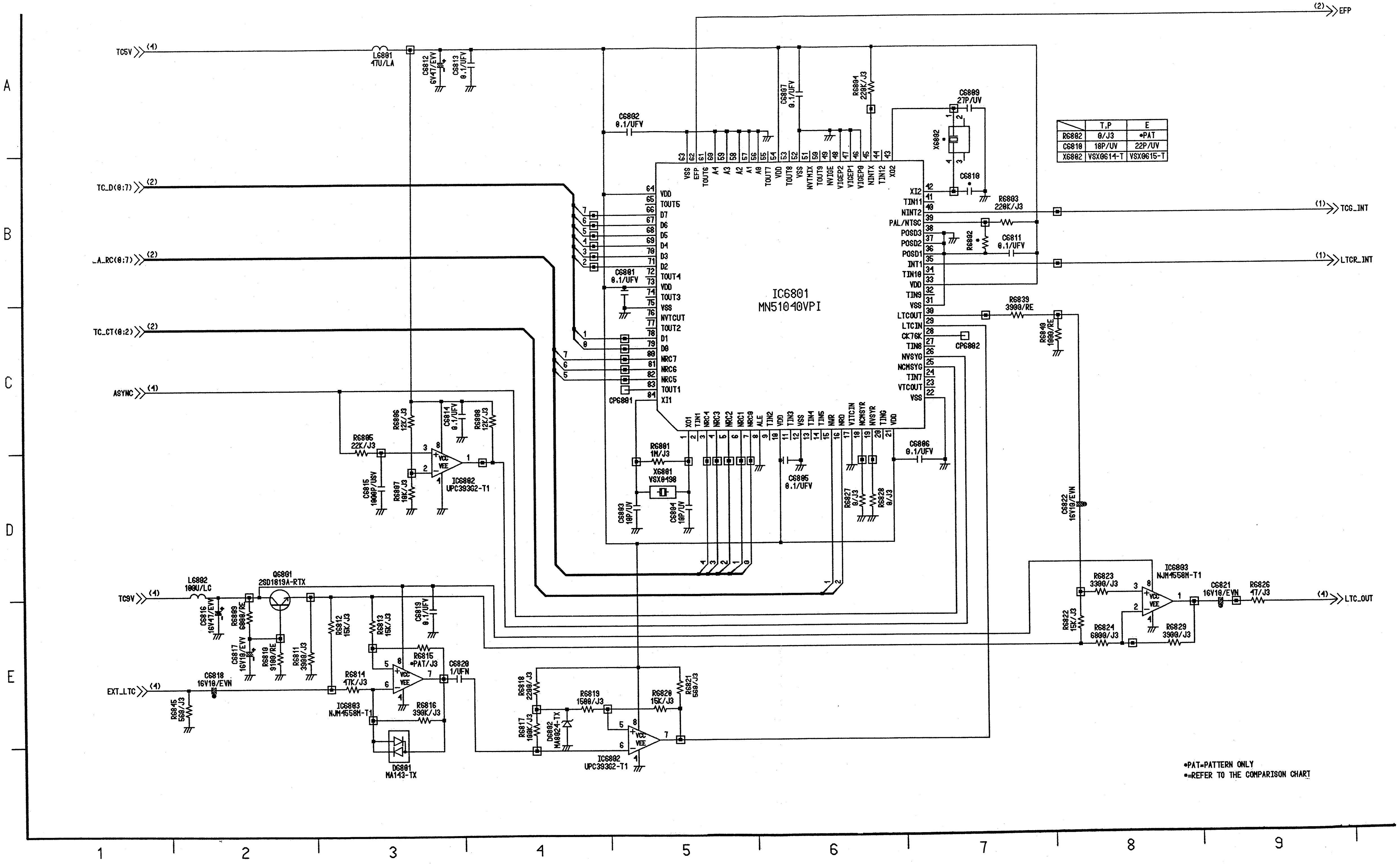
VTR SYSCON (2/5) SCHEMATIC DIAGRAM



	T	P	E
R6245	0/J3	*PAT	*PAT
R6246	*PAT	*PAT	0/J3

A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9
+5VSYS
R6225 100K/J3
R6226 68K/J3
R6227 68K/J3
R6228 68K/J3
R6229 68K/J3
R6230 68K/J3
ZEBRA_SW (4)
ABB_SW (4)
AWB_SW (4)
SHUT_SW1 (4)
SHUT_SW2 (4)
R6220 1000/J3
R6221 1000/J3
R6222 1000/J3
R6223 1000/J3
R6224 1000/J3
C6213 0.1/UFV
C6214 0.1/UFV
C6215 0.1/UFV
C6216 0.1/UFV
C6217 0.1/UFV
R6245
(3) TC_A_RC(0:7)
(3) TC_D(0:7)
CS1_L (1)
SYS_OE (1)
R6231 100K/J3
R6232 100K/J3
EFP (3)
SYS_WE (1)
PRT_RESET (1)
R6246
SYS_D(0:7) (1)
IC6201
MB89363B
P34
P35
P36
P37
_W
RST
NC
RH_RL
OUS_INS
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
P07
P06
P05
P04
P33
P32
P31
P30
_CSL
GND
P57
P56
P55
P54
P50
P51
P52
P53
P40
P41
P42
P43
P44
P45
P46
P47
VCC
P17
P16
P15
P14
P13
P12
P11
P10
P23
P03
P02
P01
P00
CS1
RSLCT1
RSLCT0
P27
P26
P25
P24
P20
P21
P22
C6201 0.1/UFV
+5VSYS L6201 100U/LC
A5V
R6217 47K/J3
C6219 6V47/EV
C6211 0.1/UFV
R6218 100K/J3
R6215 1000/J3
TALLY_26P (4)
R6219 100K/J3
C6209 0.1/UFV
R6216 100K/J3
IC6202 UPC393G2-T1
VCC
VEE
R6211 68K/J3
R6212 68K/J3
START_SW (4)
RET_SW (4)
R6213 1000/J3
R6214 1000/J3
C6207 0.1/UFV
C6208 0.1/UFV
CS0_L (1)
SYS_A(0:15) (1)
CP6203
CP6201
CP6204
R6239 1000/J3
R6240 1000/J3
R6241 1000/J3
(4) VF_DATA
(4) VF_CLK
(4) VF_WR
QR6207 UN5114-TX
QR6208 UN5213-TX
QR6209 UN5213-TX
R6238 1000/J3
R6237 100K/J3
QR6206 UN5213-TX
(4) TCF1
(4) TCF0
(4) START_26P
(4) ANTON_LIGHT
R6206 68K/J3
R6207 68K/J3
R6208 68K/J3
R6209 68K/J3
R6210 68K/J3
EJECT_SW (4)
STOP_SW (4)
PLAY_SW (4)
FF_SW (4)
REW_SW (4)
R6201 1000/J3
R6202 1000/J3
R6203 1000/J3
R6204 1000/J3
R6205 1000/J3
C6206 0.1/UFV
C6205 0.1/UFV
C6204 0.1/UFV
C6203 0.1/UFV
C6202 0.1/UFV
QR6201 UN5114-TX
QR6202 UN5114-TX
QR6203 UN5114-TX
QR6204 UN5114-TX
R6233 270/J6
R6234 270/J6
R6235 270/J6
R6236 270/J6
(4) BACK_TALLY
(4) PLAY_LED
(4) FF_LED
(4) REW_LED
(3) TC_CT(1:2)
R6243 0/J3
R6244 0/J3
CP6206

VTR SYSCON (3/5) SCHEMATIC DIAGRAM

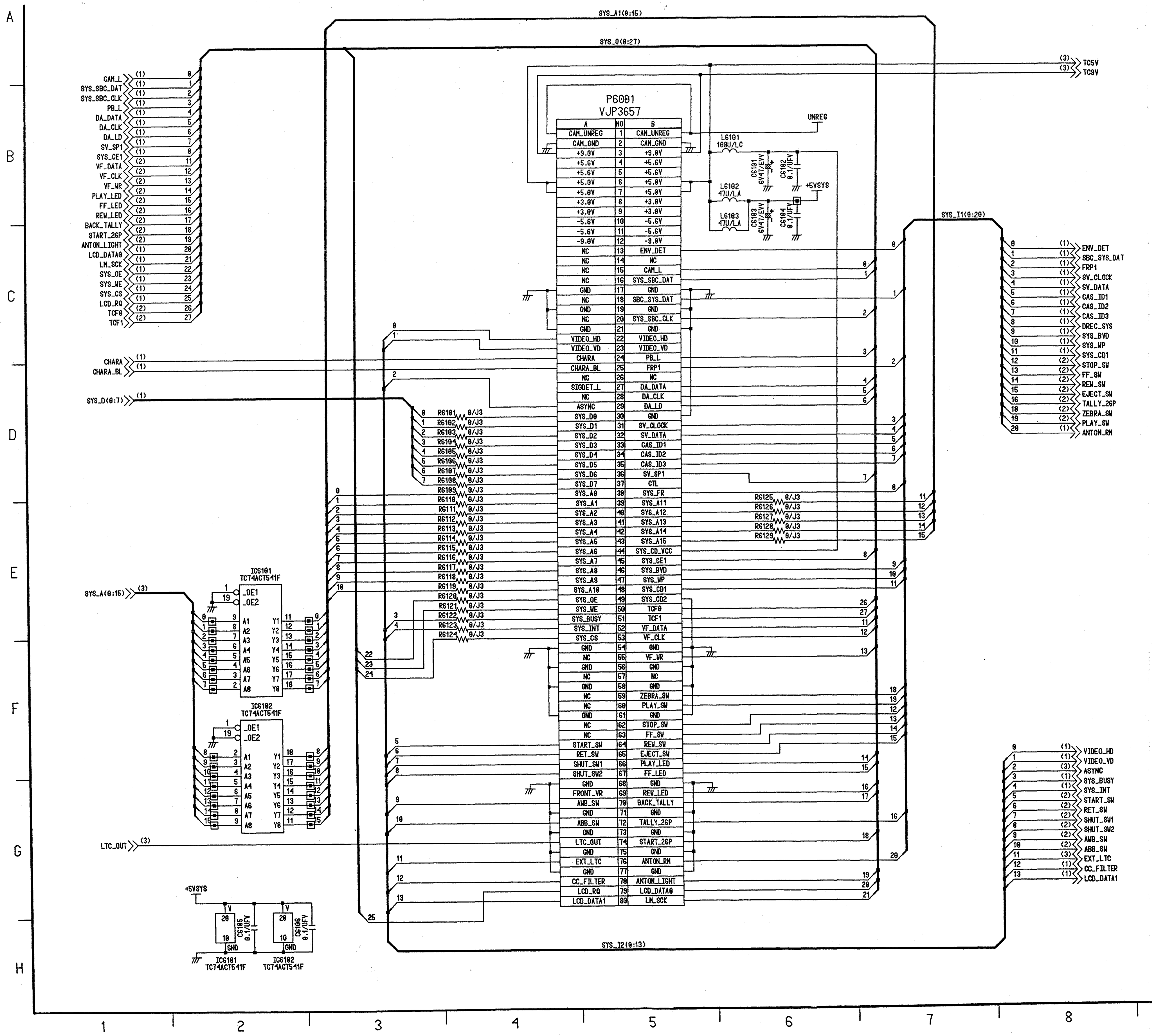

TC5V (4)
L6801 47U/LA
C6812 6V47/EVV
C6813 0.1/UFV
(2) EFP
R6804 220K/J3
C6807 0.1/UFV
C6809 27P/UV
X6802
C6802 0.1/UFV
C6810
R6803 220K/J3
(1) TCG_INT
TC_D(0:7) (2)
_A_RC(0:7) (2)
R6802
C6811 0.1/UFV
(1) LTCR_INT
C6801 0.1/UFV
IC6801
MN51040VPI
R6839 3900/RE
R6840 1000/RE
TC_CT(0:2) (2)
CP6802
ASYNC (4)
CP6801
R6806 12K/J3
C6814 0.1/UFV
R6808 12K/J3
R6805 22K/J3
C6815 1000P/USV
R6807 10K/J3
IC6802 UPC393G2-T1
R6801 1M/J3
XS801 VSX0498
C6803 10P/UV
C6804 10P/UV
C6805 0.1/UFV
R6827 0/J3
R6828 0/J3
C6806 0.1/UFV
C6822 16V10/EVN
IC6803 NJM4558M-T1
R6823 3300/J3
C6821 16V10/EVN
R6826 47/J3
(4) LTC_OUT
R6822 15K/J3
R6824 6800/J3
R6829 3900/J3
TC9V (4)
L6802 100U/LC
Q6801 2SD1819A-RTX
C6816 16V47/EVV
R6809 6800/RE
C6817 16V10/EVV
R6810 9100/RE
R6811 3900/J3
R6812 15K/J3
R6813 15K/J3
C6819 0.1/UFV
R6815 *PAT/J3
C6820 1/UFN
EXT_LTC (4)
C6818 16V10/EVN
R6845 560/J3
R6814 47K/J3
IC6803 NJM4558M-T1
R6816 390K/J3
D6801 MA143-TX
R6818 2200/J3
R6817 100K/J3
D6802 MA8024-TX
R6819 1500/J3
R6820 15K/J3
R6821 560/J3
IC6802 UPC393G2-T1
A
B
C
D
E
1
2
3
4
5
6
7
8
9

	T,P	E
R6802	0/J3	*PAT
C6810	18P/UV	22P/UV
X6802	VSX0614-T	VSX0615-T

*PAT=PATTERN ONLY
*=REFER TO THE COMPARISON CHART

REVERSE SIDE
VTR SYSCON 2/5

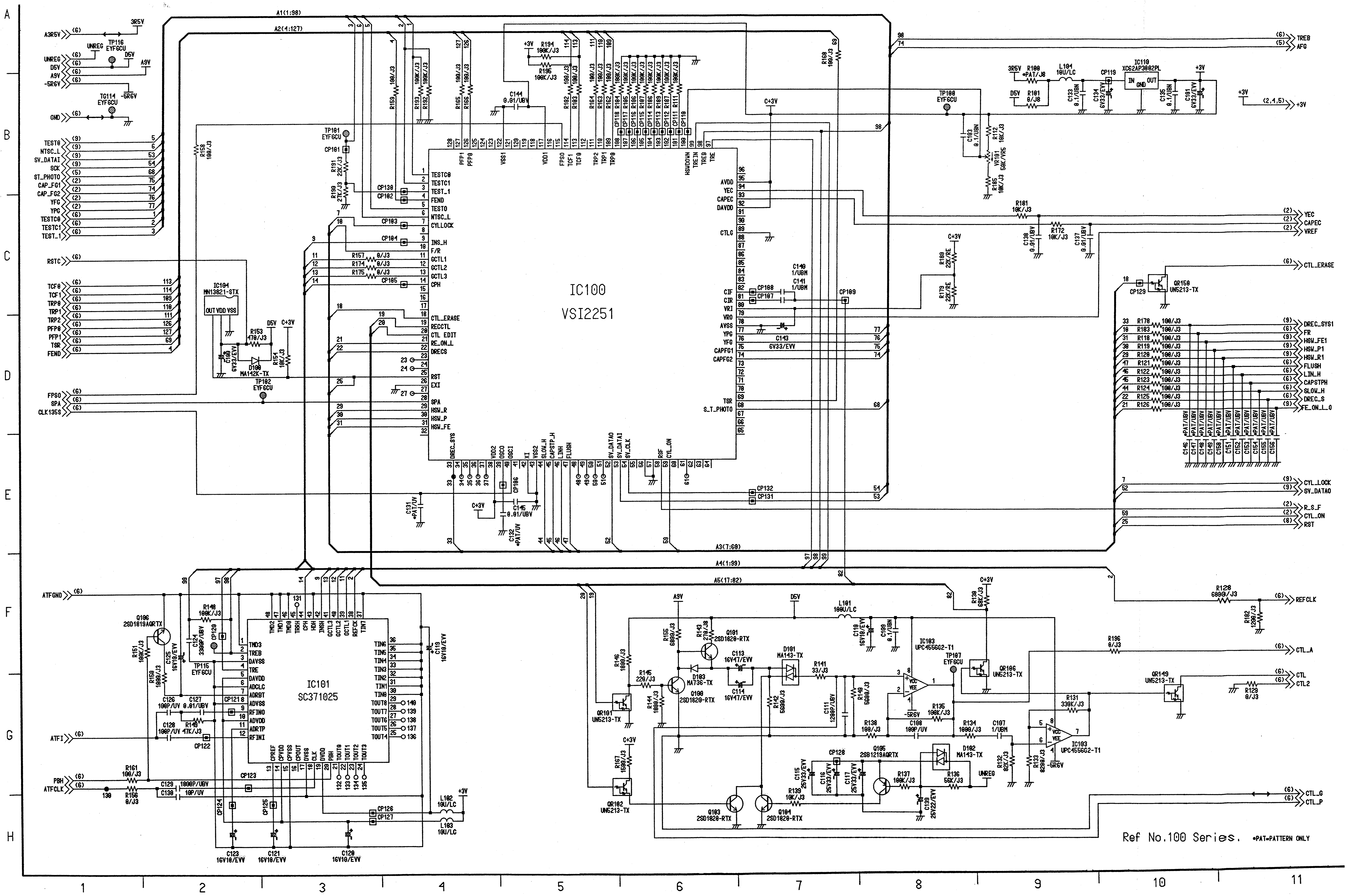
VTR SYSCON (4/5) CONNECTOR SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
SYS_A1(0:15)
SYS_O(0:27)
SYS_I1(0:20)
SYS_I2(0:13)
CAM_L (1) 0
SYS_SBC_DAT (1) 1
SYS_SBC_CLK (1) 2
PB_L (1) 3
DA_DATA (1) 4
DA_CLK (1) 5
DA_LD (1) 6
SV_SP1 (1) 7
SYS_CE1 (1) 8
VF_DATA (2) 11
VF_CLK (2) 12
VF_WR (2) 13
PLAY_LED (2) 14
FF_LED (2) 15
REW_LED (2) 16
BACK_TALLY (2) 17
START_26P (2) 18
ANTON_LIGHT (2) 19
LCD_DATA0 (1) 20
LM_SCK (1) 21
SYS_OE (1) 22
SYS_WE (1) 23
SYS_CS (1) 24
LCD_RQ (1) 25
TCF0 (2) 26
TCF1 (2) 27
CHARA (1)
CHARA_BL (1)
SYS_D(0:7) (1)
SYS_A(0:15) (3)
LTC_OUT (3)
(3) TC5V
(3) TC9V
P6001
VJP3657
A NO B
CAM_UNREG 1 CAM_UNREG
CAM_GND 2 CAM_GND
+9.0V 3 +9.0V
+5.6V 4 +5.6V
+5.6V 5 +5.6V
+5.0V 6 +5.0V
+5.0V 7 +5.0V
+3.0V 8 +3.0V
+3.0V 9 +3.0V
-5.6V 10 -5.6V
-5.6V 11 -5.6V
-9.0V 12 -9.0V
NC 13 ENV_DET
NC 14 NC
NC 15 CAM_L
NC 16 SYS_SBC_DAT
GND 17 GND
NC 18 SBC_SYS_DAT
GND 19 GND
NC 20 SYS_SBC_CLK
GND 21 GND
VIDEO_HD 22 VIDEO_HD
VIDEO_VD 23 VIDEO_VD
CHARA 24 PB_L
CHARA_BL 25 FRP1
NC 26 NC
SIGDET_L 27 DA_DATA
NC 28 DA_CLK
ASYNC 29 DA_LD
SYS_D0 30 GND
SYS_D1 31 SV_CLOCK
SYS_D2 32 SV_DATA
SYS_D3 33 CAS_ID1
SYS_D4 34 CAS_ID2
SYS_D5 35 CAS_ID3
SYS_D6 36 SV_SP1
SYS_D7 37 CTL
SYS_A0 38 SYS_FR
SYS_A1 39 SYS_A11
SYS_A2 40 SYS_A12
SYS_A3 41 SYS_A13
SYS_A4 42 SYS_A14
SYS_A5 43 SYS_A15
SYS_A6 44 SYS_CD_VCC
SYS_A7 45 SYS_CE1
SYS_A8 46 SYS_BVD
SYS_A9 47 SYS_WP
SYS_A10 48 SYS_CD1
SYS_OE 49 SYS_CD2
SYS_WE 50 TCF0
SYS_BUSY 51 TCF1
SYS_INT 52 VF_DATA
SYS_CS 53 VF_CLK
GND 54 GND
NC 55 VF_WR
GND 56 GND
NC 57 NC
GND 58 GND
NC 59 ZEBRA_SW
NC 60 PLAY_SW
GND 61 GND
NC 62 STOP_SW
NC 63 FF_SW
START_SW 64 REW_SW
RET_SW 65 EJECT_SW
SHUT_SW1 66 PLAY_LED
SHUT_SW2 67 FF_LED
GND 68 GND
FRONT_VR 69 REW_LED
AWB_SW 70 BACK_TALLY
GND 71 GND
ABB_SW 72 TALLY_26P
GND 73 GND
LTC_OUT 74 START_26P
GND 75 GND
EXT_LTC 76 ANTON_RM
GND 77 GND
CC_FILTER 78 ANTON_LIGHT
LCD_RQ 79 LCD_DATA0
LCD_DATA1 80 LM_SCK
UNREG
L6101
100U/LC
L6102
47U/LA
L6103
47U/LA
C6101
6V47/EVV
C6102
0.1/UFV
C6103
6V47/EVV
C6104
0.1/UFV
+5VSYS
R6101 0/J3
R6102 0/J3
R6103 0/J3
R6104 0/J3
R6105 0/J3
R6106 0/J3
R6107 0/J3
R6108 0/J3
R6109 0/J3
R6110 0/J3
R6111 0/J3
R6112 0/J3
R6113 0/J3
R6114 0/J3
R6115 0/J3
R6116 0/J3
R6117 0/J3
R6118 0/J3
R6119 0/J3
R6120 0/J3
R6121 0/J3
R6122 0/J3
R6123 0/J3
R6124 0/J3
R6125 0/J3
R6126 0/J3
R6127 0/J3
R6128 0/J3
R6129 0/J3
IC6101
TC74ACT541F
_OE1
_OE2
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
IC6102
TC74ACT541F
+5VSYS
V
20
10
GND
C6105
0.1/UFV
C6106
0.1/UFV
IC6101
TC74ACT541F
IC6102
TC74ACT541F
0 (1) ENV_DET
1 (1) SBC_SYS_DAT
2 (1) FRP1
3 (1) SV_CLOCK
4 (1) SV_DATA
5 (1) CAS_ID1
6 (1) CAS_ID2
7 (1) CAS_ID3
8 (1) DREC_SYS
9 (1) SYS_BVD
10 (1) SYS_WP
11 (1) SYS_CD1
12 (2) STOP_SW
13 (2) FF_SW
14 (2) REW_SW
15 (2) EJECT_SW
16 (2) TALLY_26P
18 (2) ZEBRA_SW
19 (2) PLAY_SW
20 (1) ANTON_RM
0 (1) VIDEO_HD
1 (1) VIDEO_VD
2 (3) ASYNC
3 (1) SYS_BUSY
4 (1) SYS_INT
5 (2) START_SW
6 (2) RET_SW
7 (2) SHUT_SW1
8 (2) SHUT_SW2
9 (2) AWB_SW
10 (2) ABB_SW
11 (3) EXT_LTC
12 (1) CC_FILTER
13 (1) LCD_DATA1

VTR SYSCON (5/5)
COMPARISON CHART BETWEEN MODELS

REF	T	P	E	ON
C6011	*PAT/UV	*PAT/UV	*PAT/UV	33P/UV
C6020	*PAT/UV	*PAT/UV	*PAT/UV	33P/UV
C6810	18P/UV	18P/UV	22P/UV	18P/UV
D6005	*PAT	*PAT	*PAT	MA728-TX
D6006	*PAT	*PAT	*PAT	MA728-TX
D6010	*PAT	*PAT	*PAT	MA728-TX
D6011	*PAT	*PAT	*PAT	MA728-TX
D6019	*PAT	*PAT	*PAT	MA728-TX
D6020	*PAT	*PAT	*PAT	MA728-TX
R6027	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R6028	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R6245	0/J3	*PAT/J3	*PAT/J3	0/J3
R6246	*PAT/J3	*PAT/J3	0/J3	0/J3
R6802	0/J3	0/J3	*PAT/J3	0/J3
R6815	*PAT/J3	*PAT/J3	*PAT/J3	100K/J3
X6802	VSX0614-T	VSX0614-T	VSX0615-T	VSX0614-T

SERVO (1/9) SCHEMATIC DIAGRAM


IC100
VSI2251
IC101
SC371025
IC104
MN13821-STX
IC110
XC62AP3002PL
IC103
UPC4556G2-T1
A1(1:98)
A2(4:127)
A3(7:60)
A4(1:99)
A5(17:82)
A3R5V
UNREG
D5V
A9V
-5R6V
GND
TEST0
NTSC_L
SV_DATAI
SCK
ST_PHOTO
CAP_FG1
CAP_FG2
YFG
YPG
TESTC0
TESTC1
TEST_1
RSTC
TCF0
TCF1
TRP0
TRP1
TRP2
PFP0
PFP1
TSR
FEND
FPSO
SPA
CLK135S
TREB
AFG
YEC
CAPEC
VREF
CTL_ERASE
DREC_SYS1
FR
HSW_FE1
HSW_P1
HSW_R1
FLUSH
LIN_H
CAPSTPH
SLOW_H
DREC_S
FE_ON_L_0
CYL_LOCK
SV_DATAO
R_S_F
CYL_ON
RST
REFCLK
CTL_A
CTL
CTL2
CTL_G
CTL_P
ATFGND
ATFI
PBH
ATFCLK
Q106 2SD1819AQRTX
Q100 2SD1820-RTX
Q101 2SD1820-RTX
Q103 2SD1820-RTX
Q104 2SD1820-RTX
Q105 2SB1219AQRTX
QR101 UN5213-TX
QR102 UN5213-TX
QR106 UN5213-TX
QR149 UN5213-TX
QR150 UN5213-TX
D100 MA142K-TX
D101 MA143-TX
D102 MA143-TX
D103 MA736-TX
Ref No.100 Series.
*PAT=PATTERN ONLY
A
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C
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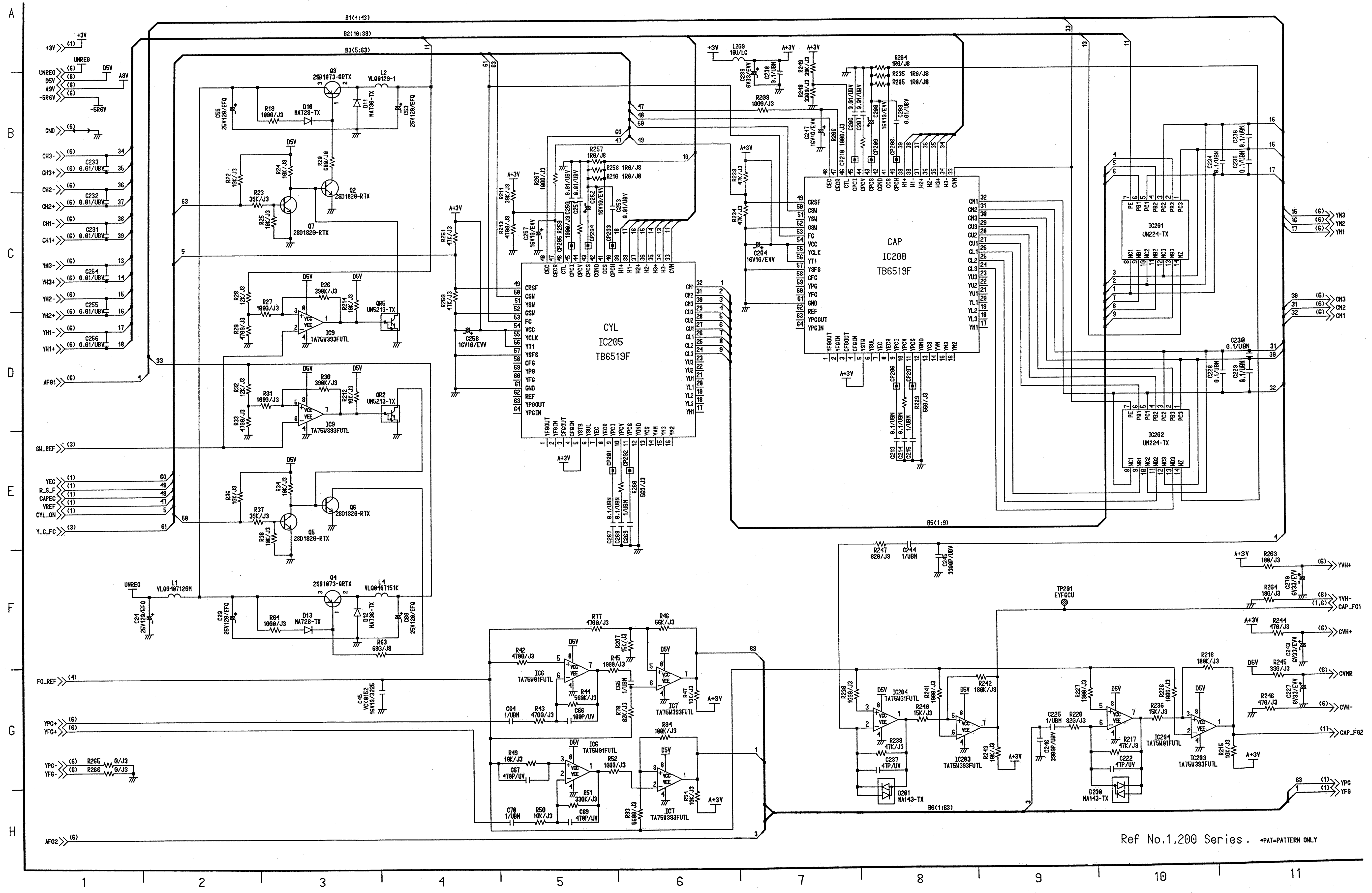
SERVO (2/9) SCHEMATIC DIAGRAM



A
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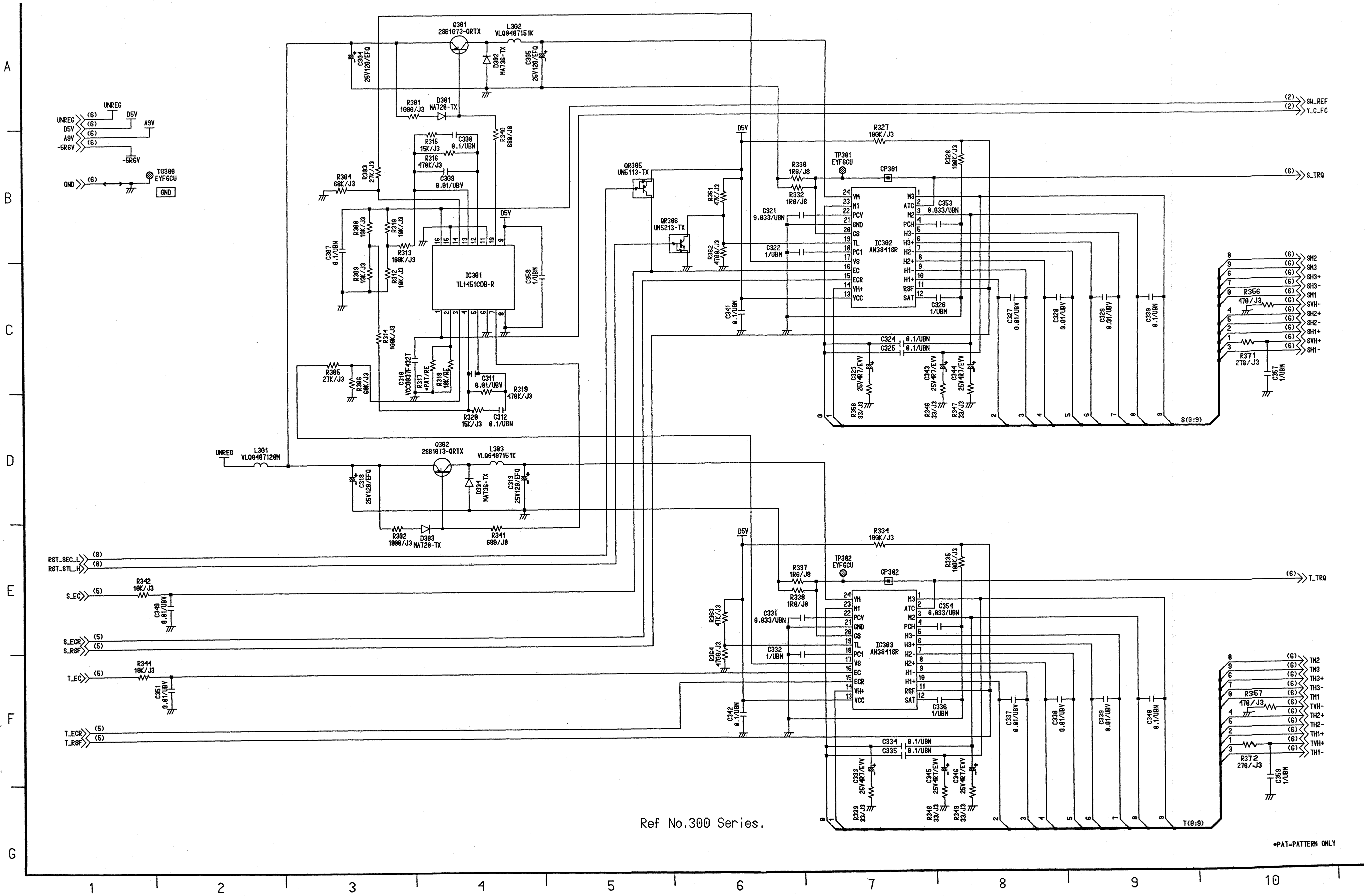
11
+3V
UNREG
D5V
A9V
-5R6V
GND
CH3-
CH3+
CH2-
CH2+
CH1-
CH1+
YH3-
YH3+
YH2-
YH2+
YH1-
YH1+
AFG1
SW_REF
YEC
R_S_F
CAPEC
VREF
CYL_ON
Y_C_FC
FG_REF
YPG+
YFG+
YPG-
YFG-
AFG2
B1(1:43)
B2(10:39)
B3(5:63)
B5(1:9)
B6(1:63)
Q3 2SB1073-QRTX
L2 VLQ0129-1
D10 MA728-TX
D11 MA736-TX
Q2 2SD1820-RTX
Q7 2SD1820-RTX
IC9 TA75W393FUTL
QR5 UN5213-TX
QR2 UN5213-TX
Q6 2SD1820-RTX
Q5 2SD1820-RTX
Q4 2SB1073-QRTX
L1 VLQ0407120M
L4 VLQ0407151K
D13 MA728-TX
D12 MA736-TX
CYL IC205 TB6519F
CAP IC200 TB6519F
IC201 UN224-TX
IC202 UN224-TX
IC6 TA75W01FUTL
IC7 TA75W393FUTL
IC204 TA75W01FUTL
IC203 TA75W393FUTL
D201 MA143-TX
D200 MA143-TX
TP201 EYF6CU
L200 10U/LC
YVH+
YVH-
CAP_FG1
CVH+
CVMR
CVH-
CAP_FG2
YPG
YFG
YH3
YH2
YH1
CM3
CM2
CM1
Ref No.1,200 Series.
*PAT=PATTERN ONLY

REVERSE SIDE

SERVO 1/9

SERVO (3/9) SCHEMATIC DIAGRAM


A
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9
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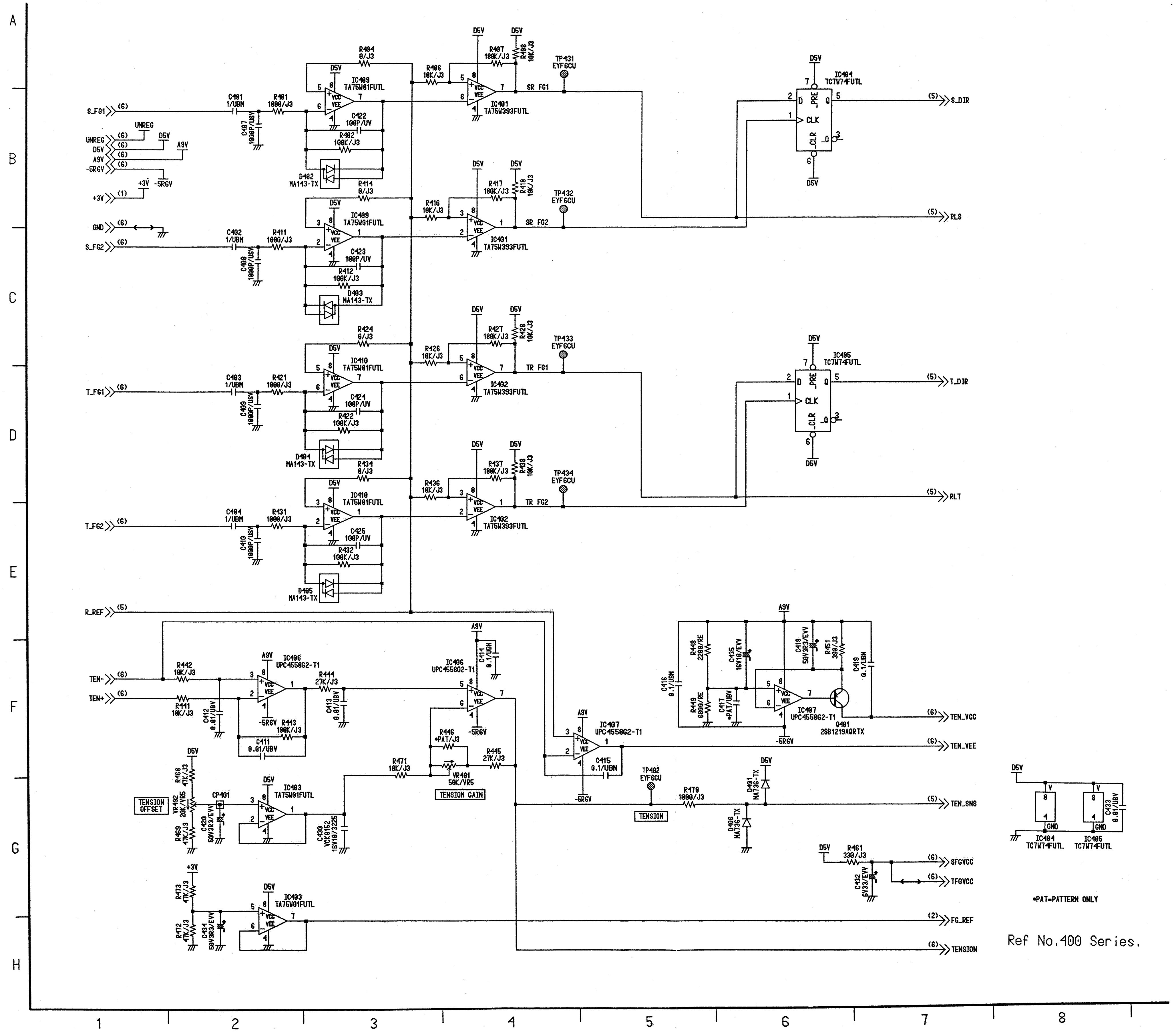
UNREG
D5V
A9V
-5R6V
GND
TG300
EYF6CU
Q301
2SB1073-QRTX
L302
VLQ0407151K
C304
25V120/EFQ
D302
MA736-TX
C305
25V120/EFQ
R301
1000/J3
D301
MA728-TX
R340
680/J8
R315
15K/J3
C308
0.1/UBN
R316
470K/J3
C309
0.01/UBV
R304
68K/J3
R303
27K/J3
C307
0.1/UBN
R308
10K/J3
R310
10K/J3
R313
100K/J3
R309
10K/J3
R312
10K/J3
IC301
TL1451CDB-R
C350
1/UBN
R314
100K/J3
R305
27K/J3
R306
68K/J3
C310
VCC0037F432T
R317
*PAT/RE
R318
10K/RE
C311
0.01/UBV
R319
470K/J3
R320
15K/J3
C312
0.1/UBN
QR305
UN5113-TX
QR306
UN5213-TX
R361
47K/J3
R362
4700/J3
C321
0.033/UBN
C322
1/UBN
C341
0.1/UBN
R330
1R0/J8
R332
1R0/J8
TP301
EYF6CU
CP301
R327
100K/J3
R328
100K/J3
IC302
AN3841SR
VH
M1
PCV
GND
CS
TL
PC1
VS
EC
ECR
VH+
VCC
M3
ATC
M2
PCH
H3-
H3+
H2-
H2+
H1-
H1+
RSF
SAT
C353
0.033/UBN
C326
1/UBN
C324
0.1/UBN
C325
0.1/UBN
C323
25V4R7/EVW
C343
25V4R7/EVW
C344
25V4R7/EVW
R358
33/J3
R346
33/J3
R347
33/J3
C327
0.01/UBV
C328
0.01/UBV
C329
0.01/UBV
C330
0.1/UBN
S(0:9)
R356
470/J3
R371
270/J3
C357
1/UBN
SW_REF
Y_C_FC
S_TRQ
SM2
SM3
SH3+
SH3-
SM1
SVH-
SH2+
SH2-
SH1+
SVH+
SH1-
UNREG
L301
VLQ0407120M
Q302
2SB1073-QRTX
L303
VLQ0407151K
C316
25V120/EFQ
D304
MA736-TX
C319
25V120/EFQ
R302
1000/J3
D303
MA728-TX
R341
680/J8
RST_SEC_L
RST_STL_H
R342
10K/J3
S_EC
C349
0.01/UBV
S_ECR
S_RSF
R344
10K/J3
T_EC
C351
0.01/UBV
T_ECR
T_RSF
D5V
R334
100K/J3
R335
100K/J3
R337
1R0/J8
R338
1R0/J8
TP302
EYF6CU
CP302
R363
47K/J3
R364
4700/J3
C331
0.033/UBN
C332
1/UBN
C342
0.1/UBN
IC303
AN3841SR
C354
0.033/UBN
C336
1/UBN
C334
0.1/UBN
C335
0.1/UBN
C333
25V4R7/EVW
C345
25V4R7/EVW
C346
25V4R7/EVW
R339
33/J3
R348
33/J3
R349
33/J3
C337
0.01/UBV
C338
0.01/UBV
C339
0.01/UBV
C340
0.1/UBN
T(0:9)
R357
470/J3
R372
270/J3
C359
1/UBN
T_TRQ
TM2
TM3
TH3+
TH3-
TM1
TVH-
TH2+
TH2-
TH1+
TVH+
TH1-
Ref No.300 Series.
*PAT=PATTERN ONLY

SERVO (4/9) SCHEMATIC DIAGRAM


A
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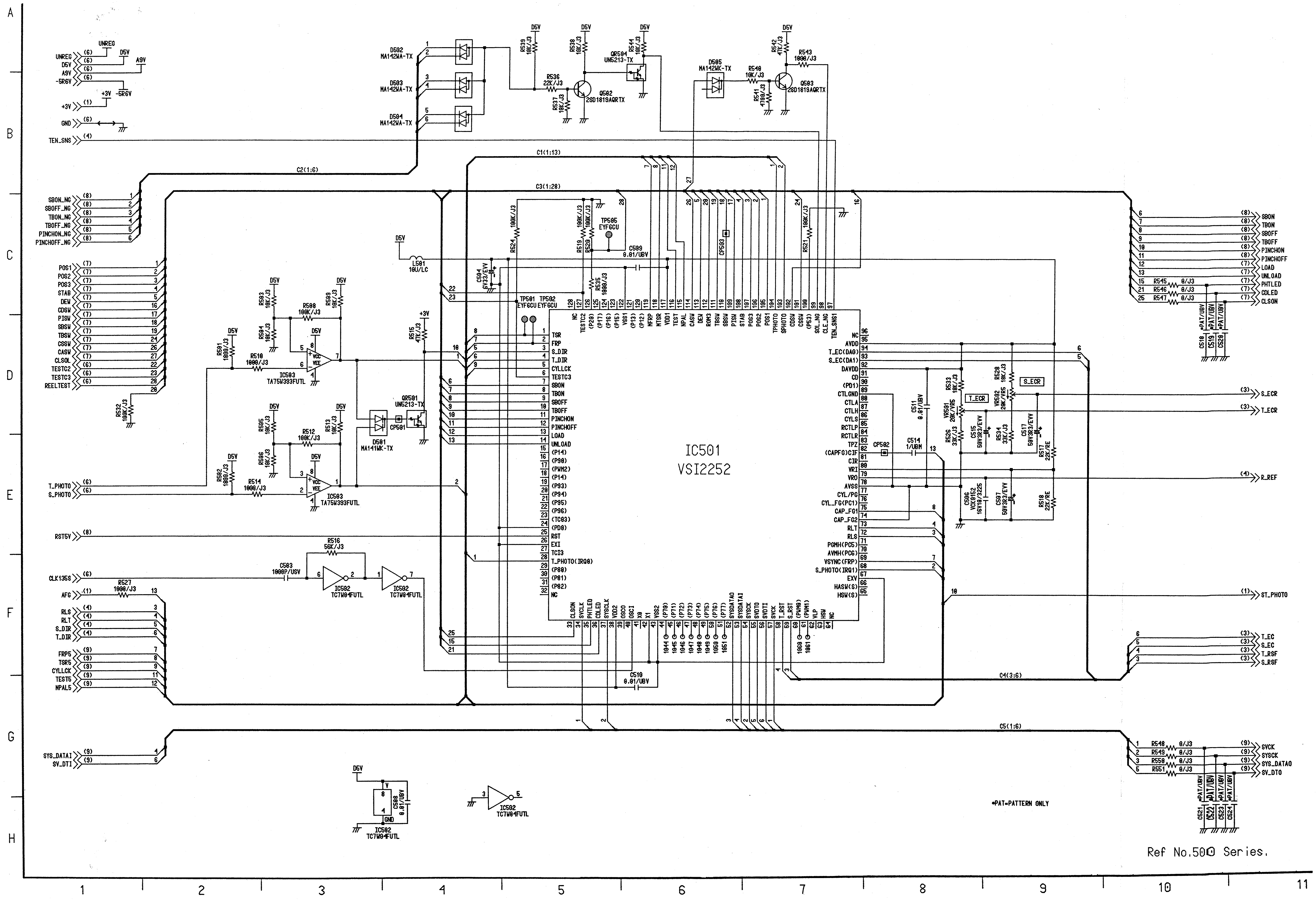
8
S_FG1
UNREG
D5V
A9V
-5R6V
+3V
GND
S_FG2
T_FG1
T_FG2
R_REF
TEN-
TEN+
C401 1/UBN
R401 1000/J3
C407 1000P/USV
R404 0/J3
IC409 TA75W01FUTL
C422 100P/UV
R402 100K/J3
D402 MA143-TX
R406 10K/J3
R407 100K/J3
R408 10K/J3
IC401 TA75W393FUTL
TP431 EYF6CU
SR FG1
IC404 TC7W74FUTL
D
CLK
PRE
CLR
Q
S_DIR
RLS
R414 0/J3
C402 1/UBN
R411 1000/J3
C408 1000P/USV
C423 100P/UV
R412 100K/J3
D403 MA143-TX
R416 10K/J3
R417 100K/J3
R418 10K/J3
TP432 EYF6CU
SR FG2
R424 0/J3
IC410 TA75W01FUTL
C403 1/UBN
R421 1000/J3
C409 1000P/USV
C424 100P/UV
R422 100K/J3
D404 MA143-TX
R426 10K/J3
R427 100K/J3
R428 10K/J3
IC402 TA75W393FUTL
TP433 EYF6CU
TR FG1
IC405 TC7W74FUTL
T_DIR
R434 0/J3
C404 1/UBN
R431 1000/J3
C410 1000P/USV
C425 100P/UV
R432 100K/J3
D405 MA143-TX
R436 10K/J3
R437 100K/J3
R438 10K/J3
TP434 EYF6CU
TR FG2
RLT
R442 10K/J3
R441 10K/J3
IC406 UPC4558G2-T1
R444 27K/J3
C412 0.01/UBV
C413 0.01/UBV
R443 100K/J3
C411 0.01/UBV
C414 0.1/UBN
R446 *PAT/J3
VR401 50K/VR5
R445 27K/J3
TENSION GAIN
R471 10K/J3
R468 4.7K/J3
VR402 20K/VR5
R469 4.7K/J3
TENSION OFFSET
CP401
C420 50V3R3/EVV
IC403 TA75W01FUTL
C430 VCK0152 16V10/3225
IC407 UPC4558G2-T1
C415 0.1/UBN
TP402 EYF6CU
R470 1000/J3
TENSION
D401 MA736-TX
D406 MA736-TX
R448 2200/RE
R449 6800/RE
C416 0.1/UBN
C435 16V10/EVV
C417 *PAT/UBV
C418 50V3R3/EVV
R451 390/J3
C419 0.1/UBN
Q401 2SB1219AQRTX
TEN_VCC
TEN_VEE
TEN_SNS
R461 330/J3
C432 6V33/EVV
SFGVCC
TFGVCC
R473 47K/J3
R472 47K/J3
C434 50V3R3/EVV
FG_REF
TENSION
IC404 TC7W74FUTL
IC405 TC7W74FUTL
C433 0.01/UBV
GND
*PAT=PATTERN ONLY
Ref No.400 Series.

REVERSE SIDE

SERVO 3/9

SERVO (5/9) SCHEMATIC DIAGRAM


IC501
VSI2252
IC503 TA75W393FUTL
IC502 TC7W04FUTL
D501 MA141WK-TX
D502 MA142WA-TX
D503 MA142WA-TX
D504 MA142WA-TX
D505 MA142WK-TX
Q502 2SD1819AQRTX
Q503 2SD1819AQRTX
QR501 UN5213-TX
QR504 UN5213-TX
L501 10U/LC
TP505 EYF6CU
TP501 TP502 EYF6CU EYF6CU
C1(1:13)
C2(1:6)
C3(1:28)
C4(3:6)
C5(1:6)
UNREG
D5V
A9V
-5R6V
+3V
GND
TEN_SNS
SBON_NG
SBOFF_NG
TBON_NG
TBOFF_NG
PINCHON_NG
PINCHOFF_NG
POS1
POS2
POS3
STAB
DEW
CDSW
PISW
SBSW
TBSW
CSSW
CASW
CLSOL
TESTC2
TESTC3
REELTEST
T_PHOTO
S_PHOTO
RST5V
CLK135S
AFG
RLS
RLT
S_DIR
T_DIR
FRP5
TSR5
CYLLCK
TEST5
NPAL5
SYS_DATAI
SV_DTI
SBON
TBON
SBOFF
TBOFF
PINCHON
PINCHOFF
LOAD
UNLOAD
PHTLED
CDLED
CLSON
S_ECR
T_ECR
R_REF
ST_PHOTO
T_EC
S_EC
T_RSF
S_RSF
SVCK
SYSCK
SYS_DATAO
SV_DTO
*PAT=PATTERN ONLY
Ref No.500 Series.
A
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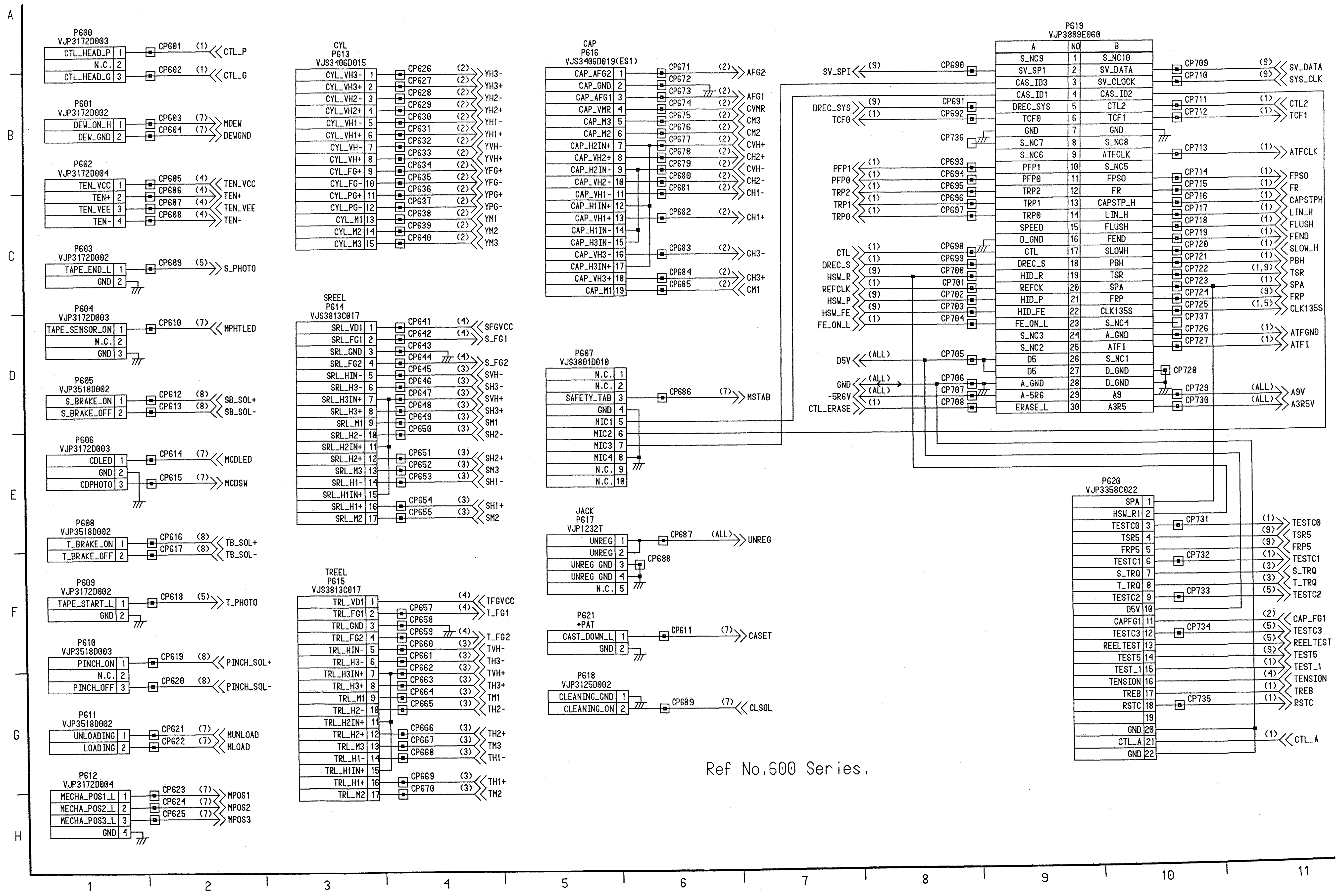
SERVO (6/9) CONNECTOR SCHEMATIC DIAGRAM



A
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G
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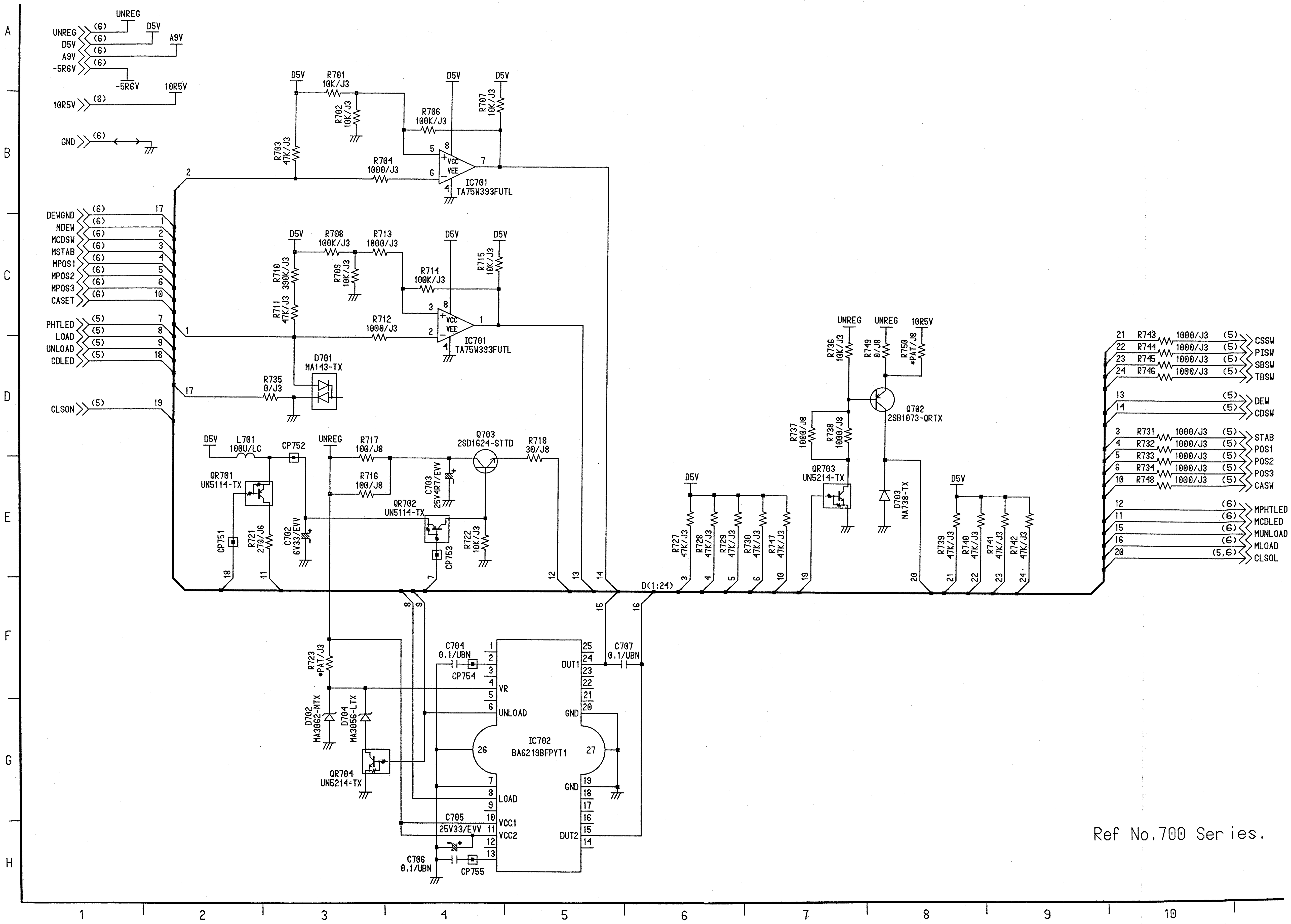
11
P600
VJP3172D003
CTL_HEAD_P 1
N.C. 2
CTL_HEAD_G 3
CP601 (1) CTL_P
CP602 (1) CTL_G
P601
VJP3172D002
DEW_ON_H 1
DEW_GND 2
CP603 (7) MDEW
CP604 (7) DEWGND
P602
VJP3172D004
TEN_VCC 1
TEN+ 2
TEN_VEE 3
TEN- 4
CP605 (4) TEN_VCC
CP606 (4) TEN+
CP607 (4) TEN_VEE
CP608 (4) TEN-
P603
VJP3172D002
TAPE_END_L 1
GND 2
CP609 (5) S_PHOTO
P604
VJP3172D003
TAPE_SENSOR_ON 1
N.C. 2
GND 3
CP610 (7) MPHTLED
P605
VJP3518D002
S_BRAKE_ON 1
S_BRAKE_OFF 2
CP612 (8) SB_SOL+
CP613 (8) SB_SOL-
P606
VJP3172D003
CDLED 1
GND 2
CDPHOTO 3
CP614 (7) MCDLED
CP615 (7) MCDSW
P608
VJP3518D002
T_BRAKE_ON 1
T_BRAKE_OFF 2
CP616 (8) TB_SOL+
CP617 (8) TB_SOL-
P609
VJP3172D002
TAPE_START_L 1
GND 2
CP618 (5) T_PHOTO
P610
VJP3518D003
PINCH_ON 1
N.C. 2
PINCH_OFF 3
CP619 (8) PINCH_SOL+
CP620 (8) PINCH_SOL-
P611
VJP3518D002
UNLOADING 1
LOADING 2
CP621 (7) MUNLOAD
CP622 (7) MLOAD
P612
VJP3172D004
MECHA_POS1_L 1
MECHA_POS2_L 2
MECHA_POS3_L 3
GND 4
CP623 (7) MPOS1
CP624 (7) MPOS2
CP625 (7) MPOS3
CYL
P613
VJS3406D015
CYL_VH3- 1
CYL_VH3+ 2
CYL_VH2- 3
CYL_VH2+ 4
CYL_VH1- 5
CYL_VH1+ 6
CYL_VH- 7
CYL_VH+ 8
CYL_FG+ 9
CYL_FG- 10
CYL_PG+ 11
CYL_PG- 12
CYL_M1 13
CYL_M2 14
CYL_M3 15
CP626 (2) YH3-
CP627 (2) YH3+
CP628 (2) YH2-
CP629 (2) YH2+
CP630 (2) YH1-
CP631 (2) YH1+
CP632 (2) YVH-
CP633 (2) YVH+
CP634 (2) YFG+
CP635 (2) YFG-
CP636 (2) YPG+
CP637 (2) YPG-
CP638 (2) YM1
CP639 (2) YM2
CP640 (2) YM3
SREEL
P614
VJS3813C017
SRL_VD1 1
SRL_FG1 2
SRL_GND 3
SRL_FG2 4
SRL_HIN- 5
SRL_H3- 6
SRL_H3IN+ 7
SRL_H3+ 8
SRL_M1 9
SRL_H2- 10
SRL_H2IN+ 11
SRL_H2+ 12
SRL_M3 13
SRL_H1- 14
SRL_H1IN+ 15
SRL_H1+ 16
SRL_M2 17
CP641 (4) SFGVCC
CP642 (4) S_FG1
CP643
CP644 (4) S_FG2
CP645 (3) SVH-
CP646 (3) SH3-
CP647 (3) SVH+
CP648 (3) SH3+
CP649 (3) SM1
CP650 (3) SH2-
CP651 (3) SH2+
CP652 (3) SM3
CP653 (3) SH1-
CP654 (3) SH1+
CP655 (3) SM2
TREEL
P615
VJS3813C017
TRL_VD1 1
TRL_FG1 2
TRL_GND 3
TRL_FG2 4
TRL_HIN- 5
TRL_H3- 6
TRL_H3IN+ 7
TRL_H3+ 8
TRL_M1 9
TRL_H2- 10
TRL_H2IN+ 11
TRL_H2+ 12
TRL_M3 13
TRL_H1- 14
TRL_H1IN+ 15
TRL_H1+ 16
TRL_M2 17
(4) TFGVCC
CP657 (4) T_FG1
CP658
CP659 (4) T_FG2
CP660 (3) TVH-
CP661 (3) TH3-
CP662 (3) TVH+
CP663 (3) TH3+
CP664 (3) TM1
CP665 (3) TH2-
CP666 (3) TH2+
CP667 (3) TM3
CP668 (3) TH1-
CP669 (3) TH1+
CP670 (3) TM2
CAP
P616
VJS3406D019(ES1)
CAP_AFG2 1
CAP_GND 2
CAP_AFG1 3
CAP_VMR 4
CAP_M3 5
CAP_M2 6
CAP_H2IN+ 7
CAP_VH2+ 8
CAP_H2IN- 9
CAP_VH2- 10
CAP_VH1- 11
CAP_H1IN+ 12
CAP_VH1+ 13
CAP_H1IN- 14
CAP_H3IN- 15
CAP_VH3- 16
CAP_H3IN+ 17
CAP_VH3+ 18
CAP_M1 19
CP671 (2) AFG2
CP672
CP673 (2) AFG1
CP674 (2) CVMR
CP675 (2) CM3
CP676 (2) CM2
CP677 (2) CVH+
CP678 (2) CH2+
CP679 (2) CVH-
CP680 (2) CH2-
CP681 (2) CH1-
CP682 (2) CH1+
CP683 (2) CH3-
CP684 (2) CH3+
CP685 (2) CM1
P607
VJS3801D010
N.C. 1
N.C. 2
SAFETY_TAB 3
GND 4
MIC1 5
MIC2 6
MIC3 7
MIC4 8
N.C. 9
N.C. 10
CP686 (7) MSTAB
JACK
P617
VJP1232T
UNREG 1
UNREG 2
UNREG GND 3
UNREG GND 4
N.C. 5
CP687 (ALL) UNREG
CP688
P621
*PAT
CAST_DOWN_L 1
GND 2
CP611 (7) CASET
P618
VJP3125D002
CLEANING_GND 1
CLEANING_ON 2
CP689 (7) CLSOL
P619
VJP3809E060
A NO B
S_NC9 1 S_NC10
SV_SP1 2 SV_DATA
CAS_ID3 3 SV_CLOCK
CAS_ID1 4 CAS_ID2
DREC_SYS 5 CTL2
TCF0 6 TCF1
GND 7 GND
S_NC7 8 S_NC8
S_NC6 9 ATFCLK
PFP1 10 S_NC5
PFP0 11 FPS0
TRP2 12 FR
TRP1 13 CAPSTP_H
TRP0 14 LIN_H
SPEED 15 FLUSH
D_GND 16 FEND
CTL 17 SLOWH
DREC_S 18 PBH
HID_R 19 TSR
REFCK 20 SPA
HID_P 21 FRP
HID_FE 22 CLK135S
FE_ON_L 23 S_NC4
S_NC3 24 A_GND
S_NC2 25 ATFI
D5 26 S_NC1
D5 27 D_GND
A_GND 28 D_GND
A-5R6 29 A9
ERASE_L 30 A3R5
SV_SPI (9) CP690
DREC_SYS (9) CP691
TCF0 (1) CP692
CP736
PFP1 (1) CP693
PFP0 (1) CP694
TRP2 (1) CP695
TRP1 (1) CP696
TRP0 (1) CP697
CTL (1) CP698
DREC_S (1) CP699
HSW_R (9) CP700
REFCLK (1) CP701
HSW_P (9) CP702
HSW_FE (9) CP703
FE_ON_L (1) CP704
D5V (ALL) CP705
GND (ALL) CP706
-5R6V (ALL) CP707
CTL_ERASE (1) CP708
CP709 (9) SV_DATA
CP710 (9) SYS_CLK
CP711 (1) CTL2
CP712 (1) TCF1
CP713 (1) ATFCLK
CP714 (1) FPS0
CP715 (1) FR
CP716 (1) CAPSTPH
CP717 (1) LIN_H
CP718 (1) FLUSH
CP719 (1) FEND
CP720 (1) SLOW_H
CP721 (1) PBH
CP722 (1,9) TSR
CP723 (1) SPA
CP724 (9) FRP
CP725 (1,5) CLK135S
CP737
CP726 (1) ATFGND
CP727 (1) ATFI
CP728
CP729 (ALL) A9V
CP730 (ALL) A3R5V
P620
VJP3358C022
SPA 1
HSW_R1 2
TESTC0 3
TSR5 4
FRP5 5
TESTC1 6
S_TRQ 7
T_TRQ 8
TESTC2 9
D5V 10
CAPFG1 11
TESTC3 12
REELTEST 13
TEST5 14
TEST_1 15
TENSION 16
TREB 17
RSTC 18
19
GND 20
CTL_A 21
GND 22
CP731 (1) TESTC0
(9) TSR5
(9) FRP5
CP732 (1) TESTC1
(3) S_TRQ
(3) T_TRQ
CP733 (5) TESTC2
(2) CAP_FG1
CP734 (5) TESTC3
(5) REELTEST
(9) TEST5
(1) TEST_1
(4) TENSION
(1) TREB
CP735 (1) RSTC
(1) CTL_A

Ref No.600 Series.

REVERSE SIDE

SERVO 5/9

SERVO (7/9) SCHEMATIC DIAGRAM


A
B
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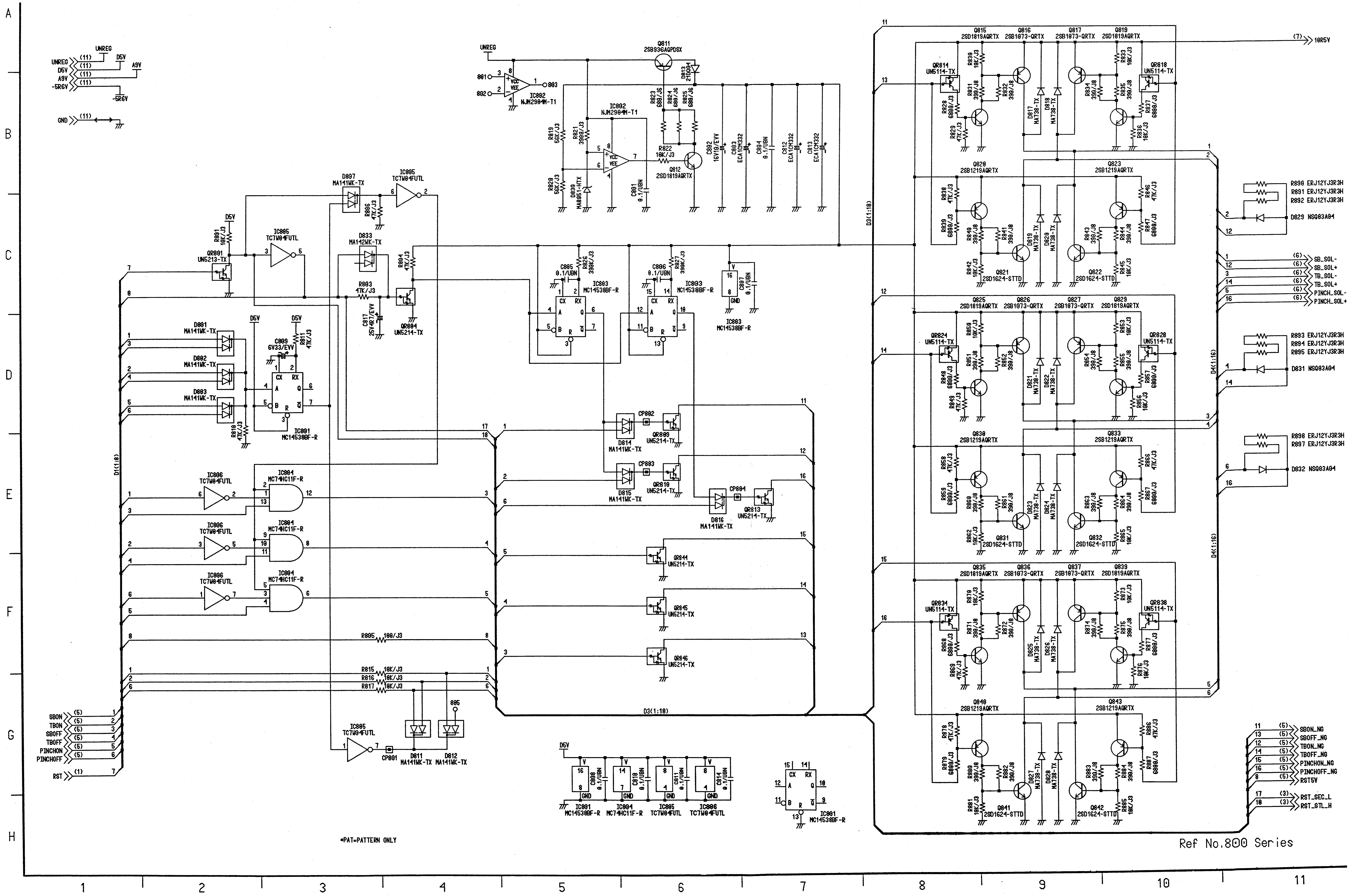
8
9
10
UNREG
D5V
A9V
-5R6V
10R5V
GND
DEWGND
MDEW
MCDSW
MSTAB
MPOS1
MPOS2
MPOS3
CASET
PHTLED
LOAD
UNLOAD
CDLED
CLSON
R701 10K/J3
R702 10K/J3
R703 47K/J3
R704 1000/J3
R706 100K/J3
R707 10K/J3
IC701 TA75W393FUTL
R708 100K/J3
R713 1000/J3
R709 10K/J3
R710 390K/J3
R711 47K/J3
R714 100K/J3
R715 10K/J3
R712 1000/J3
D701 MA143-TX
R735 0/J3
L701 100U/LC
CP752
R717 100/J8
Q703 2SD1624-STTD
R718 30/J8
R716 100/J8
C703 25V4R7/EVV
QR701 UN5114-TX
QR702 UN5114-TX
CP751
R721 270/J6
C702 6V33/EVV
CP753
R722 10K/J3
D(1:24)
R727 47K/J3
R728 47K/J3
R729 47K/J3
R730 47K/J3
R747 47K/J3
R736 10K/J3
R749 0/J8
R750 *PAT/J8
Q702 2SB1073-QRTX
R737 1000/J8
R738 1000/J8
QR703 UN5214-TX
D703 MA738-TX
R739 47K/J3
R740 47K/J3
R741 47K/J3
R742 47K/J3
R743 1000/J3
R744 1000/J3
R745 1000/J3
R746 1000/J3
R731 1000/J3
R732 1000/J3
R733 1000/J3
R734 1000/J3
R748 1000/J3
CSSW
PISW
SBSW
TBSW
DEW
CDSW
STAB
POS1
POS2
POS3
CASW
MPHTLED
MCDLED
MUNLOAD
MLOAD
CLSOL
R723 *PAT/J3
D702 MA3062-MTX
D704 MA3056-LTX
QR704 UN5214-TX
C704 0.1/UBN
CP754
C705 25V33/EVV
C706 0.1/UBN
CP755
C707 0.1/UBN
IC702 BA6219BFPYT1
VR
UNLOAD
LOAD
VCC1
VCC2
GND
OUT1
OUT2

Ref No.700 Series.

SERVO (8/9) SCHEMATIC DIAGRAM


A
B
C
D
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G
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3
4
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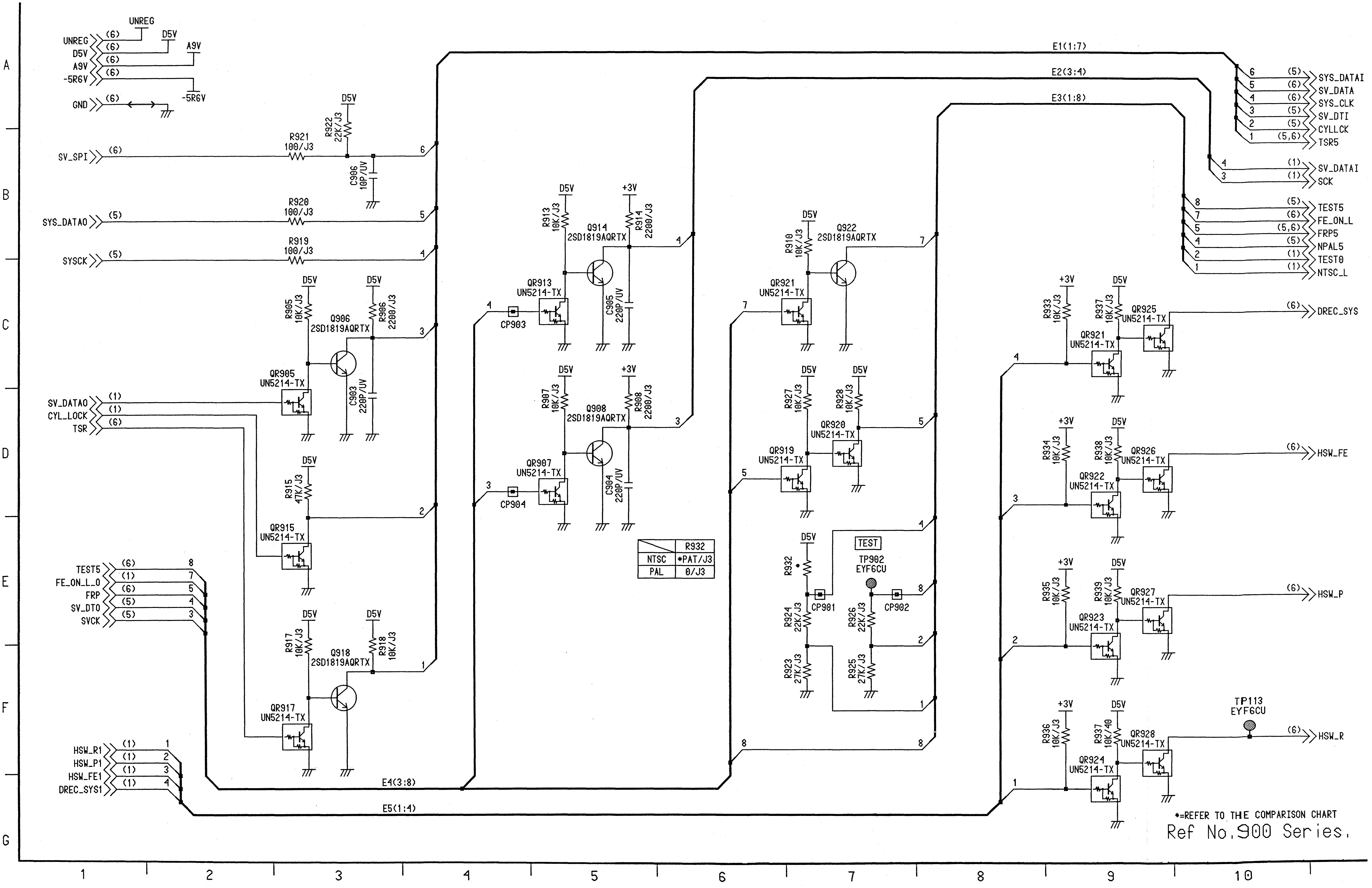
7
8
9
10
11
UNREG
D5V
A9V
-5R6V
GND
SBON
TBON
SBOFF
TBOFF
PINCHON
PINCHOFF
RST
IC802 NJM2904M-T1
Q811 2SB936AQPDSX
Q812 2SD1819AQRTX
IC805 TC7W04FUTL
IC806 TC7W04FUTL
IC801 MC14538BF-R
IC803 MC14538BF-R
IC804 MC74HC11F-R
D807 MA141WK-TX
D833 MA142WK-TX
D814 MA141WK-TX
D815 MA141WK-TX
D816 MA141WK-TX
D811 MA141WK-TX
D812 MA141WK-TX
QR801 UN5213-TX
QR804 UN5214-TX
QR809 UN5214-TX
QR810 UN5214-TX
QR813 UN5214-TX
QR844 UN5214-TX
QR845 UN5214-TX
QR846 UN5214-TX
D1(1:8)
D3(1:18)
D4(1:16)
10R5V
SB_SOL-
SB_SOL+
TB_SOL-
TB_SOL+
PINCH_SOL-
PINCH_SOL+
R890 ERJ12YJ3R3H
R891 ERJ12YJ3R3H
R892 ERJ12YJ3R3H
D829 NSQ03A04
R893 ERJ12YJ3R3H
R894 ERJ12YJ3R3H
R895 ERJ12YJ3R3H
D831 NSQ03A04
R896 ERJ12YJ3R3H
R897 ERJ12YJ3R3H
D832 NSQ03A04
SBON_NG
SBOFF_NG
TBON_NG
TBOFF_NG
PINCHON_NG
PINCHOFF_NG
RST5V
RST_SEC_L
RST_STL_H
Q815 2SD1819AQRTX
Q816 2SB1073-QRTX
Q817 2SB1073-QRTX
Q819 2SD1819AQRTX
QR814 UN5114-TX
QR818 UN5114-TX
Q820 2SB1219AQRTX
Q823 2SB1219AQRTX
Q821 2SD1624-STTD
Q822 2SD1624-STTD
*PAT=PATTERN ONLY
Ref No.800 Series

REVERSE SIDE
SERVO 7/9

SERVO (9/9) SCHEMATIC DIAGRAM



UNREG
D5V
A9V
-5R6V
GND
SV_SPI
SYS_DATAO
SYSCK
SV_DATAO
CYL_LOCK
TSR
TEST5
FE_ON_L_O
FRP
SV_DTO
SVCK
HSW_R1
HSW_P1
HSW_FE1
DREC_SYS1
R921 100/J3
R922 22K/J3
C906 10P/UV
R920 100/J3
R919 100/J3
R905 10K/J3
Q906 2SD1819AQRTX
R906 2200/J3
QR905 UN5214-TX
C903 220P/UV
R915 47K/J3
QR915 UN5214-TX
R917 10K/J3
Q918 2SD1819AQRTX
R918 10K/J3
QR917 UN5214-TX
E4(3:8)
E5(1:4)
E1(1:7)
E2(3:4)
E3(1:8)
R913 10K/J3
Q914 2SD1819AQRTX
R914 2200/J3
QR913 UN5214-TX
CP903
C905 220P/UV
R907 10K/J3
Q908 2SD1819AQRTX
R908 2200/J3
QR907 UN5214-TX
CP904
C904 220P/UV
R910 10K/J3
Q922 2SD1819AQRTX
QR921 UN5214-TX
R927 10K/J3
R928 10K/J3
QR920 UN5214-TX
QR919 UN5214-TX
TEST
TP902 EYF6CU
R932 *
CP901
CP902
R924 22K/J3
R926 22K/J3
R923 27K/J3
R925 27K/J3
SYS_DATAI
SV_DATA
SYS_CLK
SV_DTI
CYLLCK
TSR5
SV_DATAI
SCK
TEST5
FE_ON_L
FRP5
NPAL5
TEST0
NTSC_L
R933 10K/J3
R937 10K/J3
QR925 UN5214-TX
QR921 UN5214-TX
DREC_SYS
R934 10K/J3
R938 10K/J3
QR926 UN5214-TX
QR922 UN5214-TX
HSW_FE
R935 10K/J3
R939 10K/J3
QR927 UN5214-TX
QR923 UN5214-TX
HSW_P
R936 10K/J3
R937 10K/40
QR928 UN5214-TX
QR924 UN5214-TX
TP113 EYF6CU
HSW_R
A
B
C
D
E
F
G
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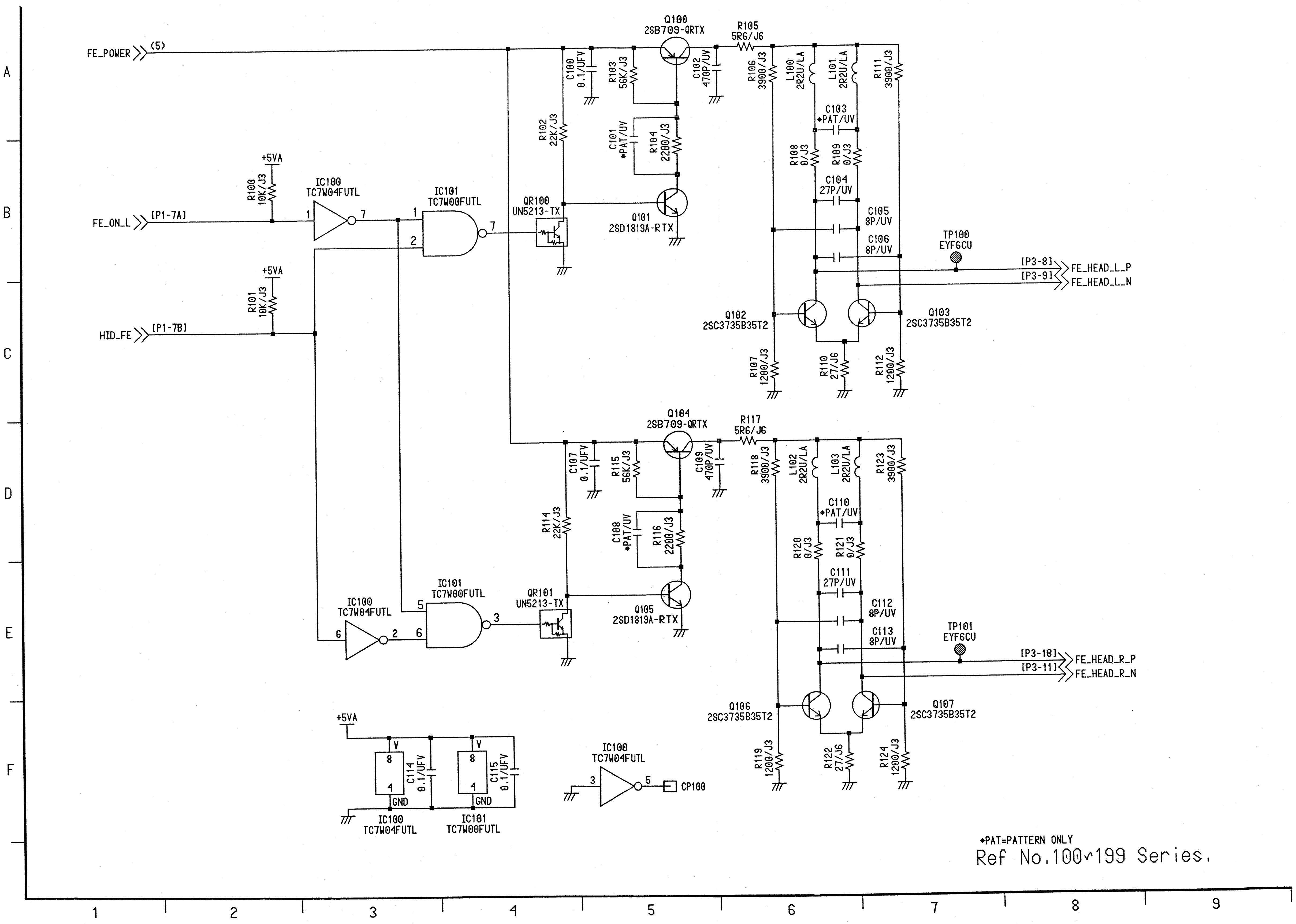
10

	R932
NTSC	*PAT/J3
PAL	0/J3

*=REFER TO THE COMPARISON CHART

Ref No.900 Series.

RF (1/5) SCHEMATIC DIAGRAM


FE_POWER
(5)
FE_ON_L
[P1-7A]
HID_FE
[P1-7B]
+5VA
R100
10K/J3
R101
10K/J3
IC100
TC7W04FUTL
IC101
TC7W00FUTL
QR100
UN5213-TX
QR101
UN5213-TX
R102
22K/J3
R114
22K/J3
C100
0.1/UFV
C107
0.1/UFV
R103
56K/J3
R115
56K/J3
Q100
2SB709-QRTX
Q104
2SB709-QRTX
C101
*PAT/UV
R104
2200/J3
C108
*PAT/UV
R116
2200/J3
C102
470P/UV
C109
470P/UV
Q101
2SD1819A-RTX
Q105
2SD1819A-RTX
R105
5R6/J6
R117
5R6/J6
R106
3900/J3
R118
3900/J3
L100
2R2U/LA
L101
2R2U/LA
L102
2R2U/LA
L103
2R2U/LA
R111
3900/J3
R123
3900/J3
C103
*PAT/UV
C110
*PAT/UV
R108
0/J3
R109
0/J3
R120
0/J3
R121
0/J3
C104
27P/UV
C111
27P/UV
C105
8P/UV
C106
8P/UV
C112
8P/UV
C113
8P/UV
TP100
EYF6CU
TP101
EYF6CU
[P3-8]
FE_HEAD_L_P
[P3-9]
FE_HEAD_L_N
[P3-10]
FE_HEAD_R_P
[P3-11]
FE_HEAD_R_N
Q102
2SC3735B35T2
Q103
2SC3735B35T2
Q106
2SC3735B35T2
Q107
2SC3735B35T2
R107
1200/J3
R110
27/J6
R112
1200/J3
R119
1200/J3
R122
27/J6
R124
1200/J3
V
GND
C114
0.1/UFV
C115
0.1/UFV
CP100
*PAT=PATTERN ONLY
Ref No.100~199 Series.
A
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C
D
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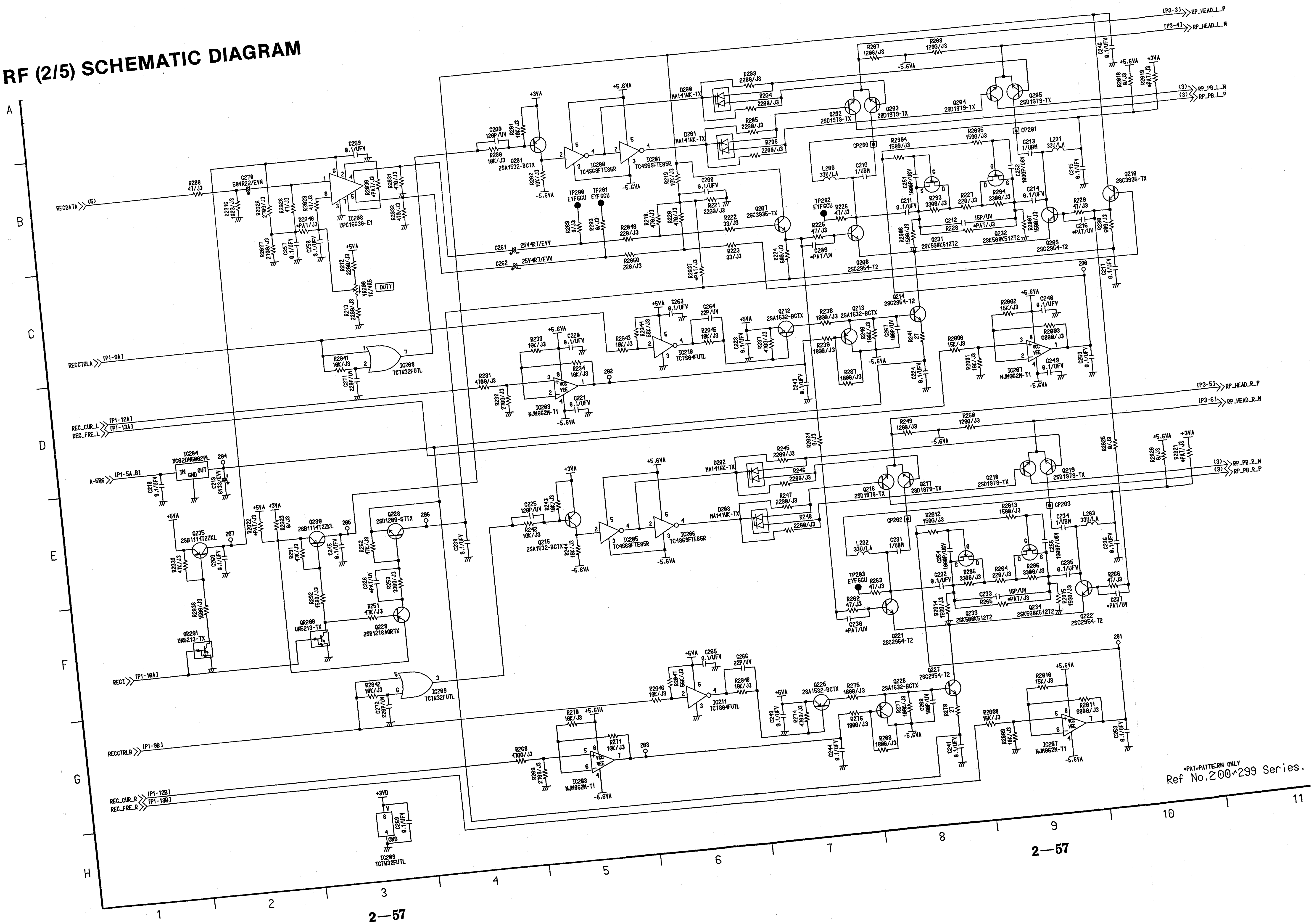
REVERSE SIDE

SERVO 9/9

RF (2/5) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
1
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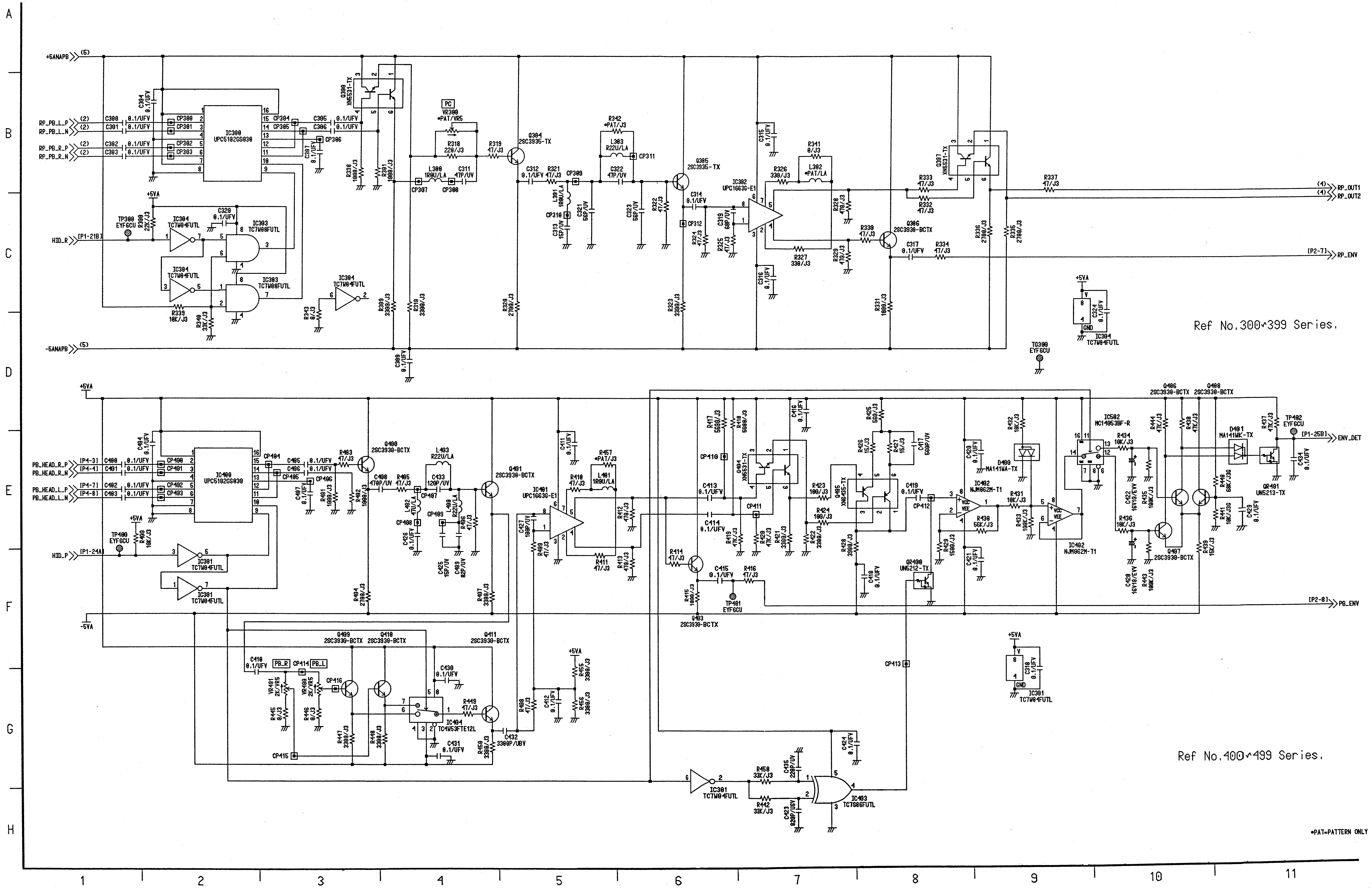
3
4
5
6
7
8
9
10
11
RECDATA
RECCTRLA
REC_CUR_L
REC_FRE_L
A-5R6
RECI
RECCTRLB
REC_CUR_R
REC_FRE_R
RP_HEAD_L_P
RP_HEAD_L_N
RP_PB_L_N
RP_PB_L_P
RP_HEAD_R_P
RP_HEAD_R_N
RP_PB_R_N
RP_PB_R_P
IC208 UPC1663G-E1
IC200 TC4S69FTE85R
IC201 TC4S69FTE85R
IC209 TC7W32FUTL
IC204 XC62DN5002PL
IC210 TC7S04FUTL
IC203 NJM062M-T1
IC207 NJM062M-T1
IC205 TC4S69FTE85R
IC206 TC4S69FTE85R
IC211 TC7S04FUTL
DUTY
+5.6VA
-5.6VA
+3VA
+5VA
+3VD

*PAT=PATTERN ONLY

Ref No.200~299 Series.

RF (3/5) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
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3
4
5
6
7
8
9
10
11
+5ANAPB (5)
-5ANAPB (5)
RP_PB_L_P (2)
RP_PB_L_N (2)
RP_PB_R_P (2)
RP_PB_R_N (2)
C300 0.1/UFV
C301 0.1/UFV
C302 0.1/UFV
C303 0.1/UFV
C304 0.1/UFV
CP300
CP301
CP302
CP303
IC300
UPC5102GS030
CP304
CP305
CP306
C305 0.1/UFV
C306 0.1/UFV
C307 0.1/UFV
Q300
XN5531-TX
R300 1000/J3
R301 1000/J3
PC
VR300
*PAT/VR5
R318 220/J3
R319 47/J3
L300 1R0U/LA
C311 47P/UV
CP307
CP308
Q304
2SC3935-TX
C312 0.1/UFV
R321 47/J3
CP309
L301 1R0U/LA
CP310
C313 15P/UV
C321 56P/UV
R342 *PAT/J3
L303 R22U/LA
CP311
C322 47P/UV
C323 56P/UV
R322 47/J3
Q305
2SC3935-TX
C314 0.1/UFV
CP312
R324 47/J3
C319 68P/UV
R325 47/J3
IC302
UPC1663G-E1
C315 0.1/UFV
C316 0.1/UFV
R326 330/J3
R341 0/J3
L302 *PAT/LA
R327 330/J3
R328 470/J3
R329 470/J3
R330 47/J3
Q306
2SC3930-BCTX
C317 0.1/UFV
R334 47/J3
R331 1800/J3
Q307
XN5531-TX
R333 47/J3
R332 47/J3
R336 2700/J3
R335 2700/J3
R337 47/J3
(4) RP_OUT1
(4) RP_OUT2
[P2-7] RP_ENV
+5VA
TP300
EYF6CU
R300 22K/J3
HID_R [P1-21B]
IC304
TC7W04FUTL
C320 0.1/UFV
IC303
TC7W08FUTL
R339 10K/J3
R340 33K/J3
R343 0/J3
R309 3300/J3
R310 3300/J3
C309 0.1/UFV
R320 2700/J3
R323 3300/J3
V
GND
C324 0.1/UFV
TG300
EYF6CU
PB_HEAD_R_P [P4-3]
PB_HEAD_R_N [P4-4]
PB_HEAD_L_P [P4-7]
PB_HEAD_L_N [P4-8]
C400 0.1/UFV
C401 0.1/UFV
C402 0.1/UFV
C403 0.1/UFV
C404 0.1/UFV
CP400
CP401
CP402
CP403
IC400
UPC5102GS030
CP404
CP405
CP406
C405 0.1/UFV
C406 0.1/UFV
C407 0.1/UFV
R401 1000/J3
R402 1000/J3
R403 47/J3
Q400
2SC3930-BCTX
C408 470P/UV
R405 47/J3
L403 R22U/LA
C433 120P/UV
CP407
L402 47U/LA
CP408
C426 0.1/UFV
CP409
L400 R22U/LA
R406 47/J3
C425 15P/UV
C409 82P/UV
Q401
2SC3930-BCTX
R404 2700/J3
R407 3300/J3
IC401
UPC1663G-E1
C411 0.1/UFV
R457 *PAT/J3
R410 47/J3
L401 1R0U/LA
C427 100P/UV
R409 47/J3
R411 47/J3
R412 470/J3
R413 470/J3
TP400
EYF6CU
R400 10K/J3
HID_P [P1-24A]
IC301
TC7W04FUTL
-5VA
R417 5600/J3
R418 5600/J3
CP410
C413 0.1/UFV
C414 0.1/UFV
Q404
XN5531-TX
C416 0.1/UFV
CP411
R419 47K/J3
R420 47K/J3
R421 3300/J3
R414 47/J3
Q403
2SC3930-BCTX
C415 0.1/UFV
R416 47/J3
R415 1800/J3
TP401
EYF6CU
R423 100/J3
R424 100/J3
R422 3300/J3
R425 560/J3
R426 15/J3
R427 15/J3
C417 560P/UV
Q405
XN6435-TX
R428 3900/J3
C418 0.1/UFV
C419 0.1/UFV
CP412
QR400
UN5212-TX
R429 1500/J3
IC402
NJM062M-T1
VCC
VEE
R430 56K/J3
R431 10K/J3
R433 100K/J3
C420 0.1/UFV
C421 0.1/UFV
R432 10K/J3
D400
MA141WA-TX
IC502
MC14053BF-R
R434 10K/J3
C422 16V10/EVV
R435 100K/J3
R436 10K/J3
C428 16V10/EVV
R443 100K/J3
Q406
2SC3930-BCTX
Q408
2SC3930-BCTX
Q407
2SC3930-BCTX
R444 47K/J3
R438 47K/J3
R440 68K/J3G
R441 10K/J3G
R439 15K/J3
C429 0.1/UFV
D401
MA141WK-TX
R437 47K/J3
TP402
EYF6CU
[P1-25B] ENV_DET
C434 0.1/UFV
QR401
UN5213-TX
[P2-8] PB_ENV
CP413
C318 0.1/UFV
Q409
2SC3930-BCTX
Q410
2SC3930-BCTX
Q411
2SC3930-BCTX
C410 0.1/UFV
PB_R
CP414
PB_L
VR401 2K/VR5
VR400 2K/VR5
CP416
R445 0/J3
R446 0/J3
R447 3300/J3
R448 3300/J3
CP415
C430 0.1/UFV
IC404
TC4W53FTE12L
C431 0.1/UFV
R449 47/J3
R450 3300/J3
C432 3300P/UBV
R408 47/J3
C412 0.1/UFV
R455 3300/J3
R456 3300/J3
R458 33K/J3
R442 33K/J3
C435 220P/UV
C423 820P/USV
C424 0.1/UFV
IC403
TC7S86FUTL

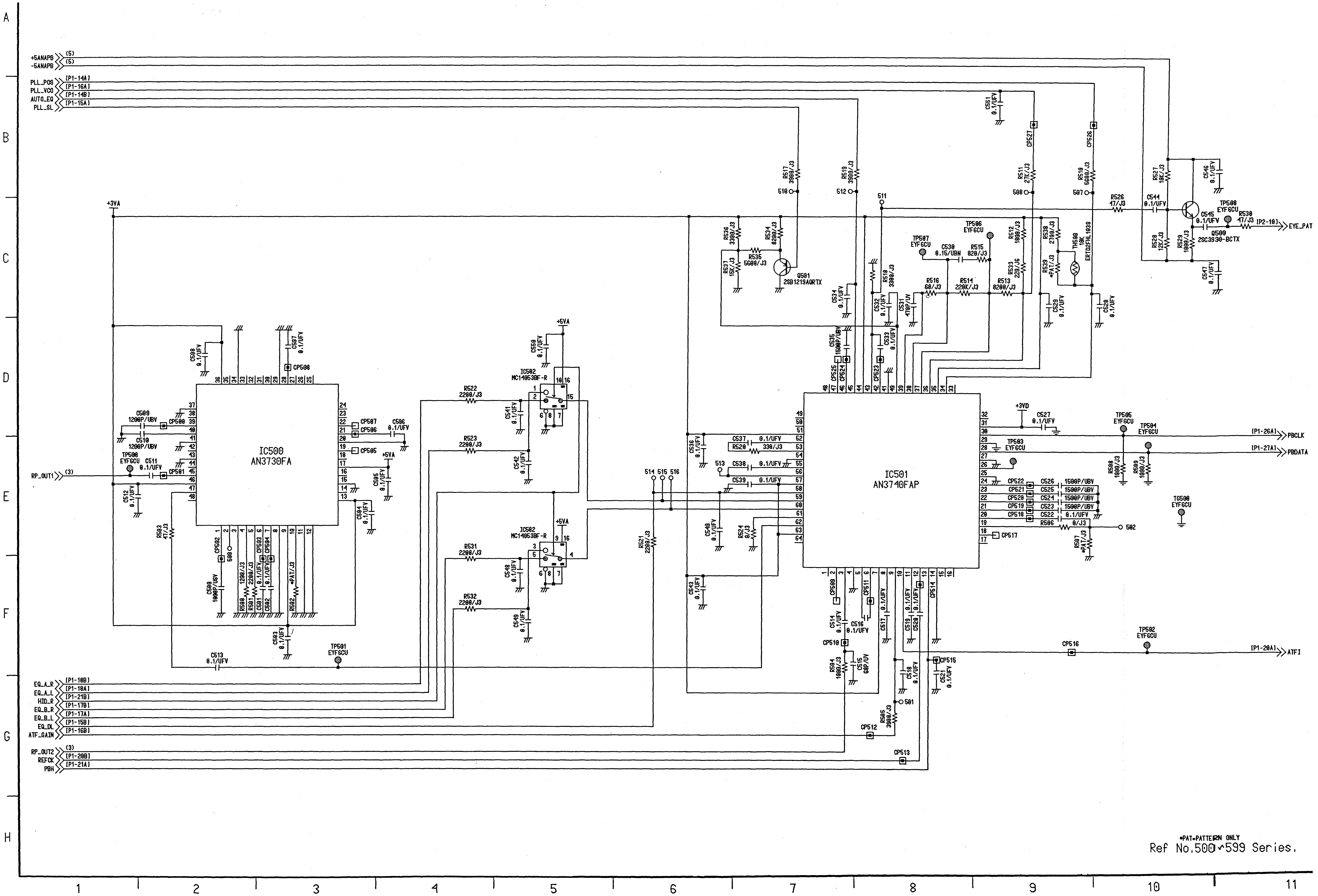
Ref No.300~399 Series.

Ref No.400~499 Series.

*PAT=PATTERN ONLY

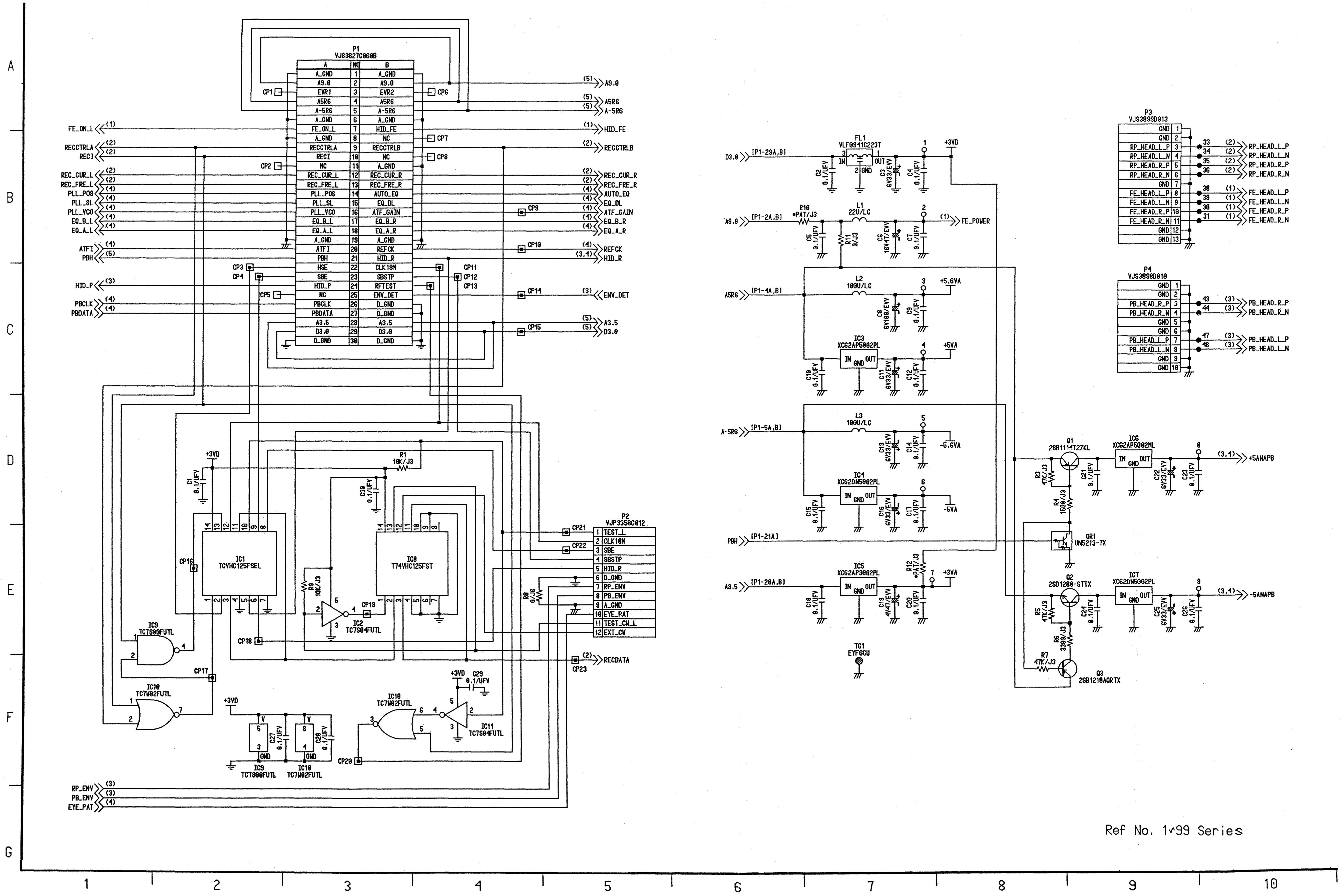
REVERSE SIDE
RF 2/5

RF (4/5) SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
+5ANAPB (5)
-5ANAPB (5)
PLL_POS [P1-14A]
PLL_VCO [P1-16A]
AUTO_EQ [P1-14B]
PLL_SL [P1-15A]
+3VA
+5VA
+3VD
IC500
AN3730FA
IC501
AN3740FAP
IC502
MC14053BF-R
Q501
2SB1219AQRTX
Q500
2SC3930-BCTX
TH500
ERTD2FHL103S
RP_OUT1 (3)
EQ_A_R [P1-18B]
EQ_A_L [P1-18A]
HID_R [P1-21B]
EQ_B_R [P1-17B]
EQ_B_L [P1-17A]
EQ_DL [P1-15B]
ATF_GAIN [P1-16B]
RP_OUT2 (3)
REFCK [P1-20B]
PBH [P1-21A]
EYE_PAT [P2-10]
PBCLK [P1-26A]
PBDATA [P1-27A]
ATFI [P1-20A]
TP500 EYF6CU
TP501 EYF6CU
TP502 EYF6CU
TP503 EYF6CU
TP504 EYF6CU
TP505 EYF6CU
TP506 EYF6CU
TP507 EYF6CU
TP508 EYF6CU
TG500 EYF6CU
R517 3900/J3
R519 3900/J3
R511 27K/J3
R510 5600/J3
R527 10K/J3
R526 47/J3
R528 12K/J3
R529 1000/J3
R530 47/J3
R536 3300/J3
R534 8200/J3
R535 5600/J3
R537 15K/J3
R518 3300/J3
R516 68/J3
R514 220K/J3
R515 820/J3
R513 8200/J3
R512 1000/J3
R533 220/J6
R538 2700/J3
R539 *PAT/J3
R522 2200/J3
R523 2200/J3
R531 2200/J3
R532 2200/J3
R521 2200/J3
R520 330/J3
R524 0/J3
R503 47/J3
R500 1200/J3
R501 2200/J3
R502 *PAT/J3
R504 1000/J3
R505 3900/J3
R506 0/J3
R507 *PAT/J3
R508 1000/J3
R509 1000/J3
C500 1000P/USV
C501 0.1/UFV
C502 0.1/UFV
C503 0.1/UFV
C504 0.1/UFV
C505 0.1/UFV
C506 0.1/UFV
C507 0.1/UFV
C508 0.1/UFV
C509 1200P/UBV
C510 1200P/UBV
C511 0.1/UFV
C512 0.1/UFV
C513 0.1/UFV
C514 0.1/UFV
C515 68P/UV
C516 0.1/UFV
C517 0.1/UFV
C518 0.1/UFV
C519 0.1/UFV
C520 0.1/UFV
C521 0.1/UFV
C522 0.1/UFV
C523 1500P/UBV
C524 1500P/UBV
C525 1500P/UBV
C526 1500P/UBV
C527 0.1/UFV
C528 0.1/UFV
C529 0.1/UFV
C530 0.15/UBN
C531 470P/UV
C532 0.1/UFV
C533 0.1/UFV
C534 0.1/UFV
C535 1000P/UBV
C536 0.1/UFV
C537 0.1/UFV
C538 0.1/UFV
C539 0.1/UFV
C540 0.1/UFV
C541 0.1/UFV
C542 0.1/UFV
C543 0.1/UFV
C544 0.1/UFV
C545 0.1/UFV
C546 0.1/UFV
C547 0.1/UFV
C548 0.1/UFV
C549 0.1/UFV
C550 0.1/UFV
C551 0.1/UFV
CP500
CP501
CP502
CP505
CP506
CP507
CP508
CP509
CP510
CP511
CP512
CP513
CP514
CP515
CP516
CP517
CP518
CP519
CP520
CP521
CP522
CP523
CP524
CP525
CP526
CP527
500
501
502
507
508
510
511
512
513
514 515 516

*PAT=PATTERN ONLY
Ref No.500~599 Series.

RF (5/5) CONNECTOR SCHEMATIC DIAGRAM



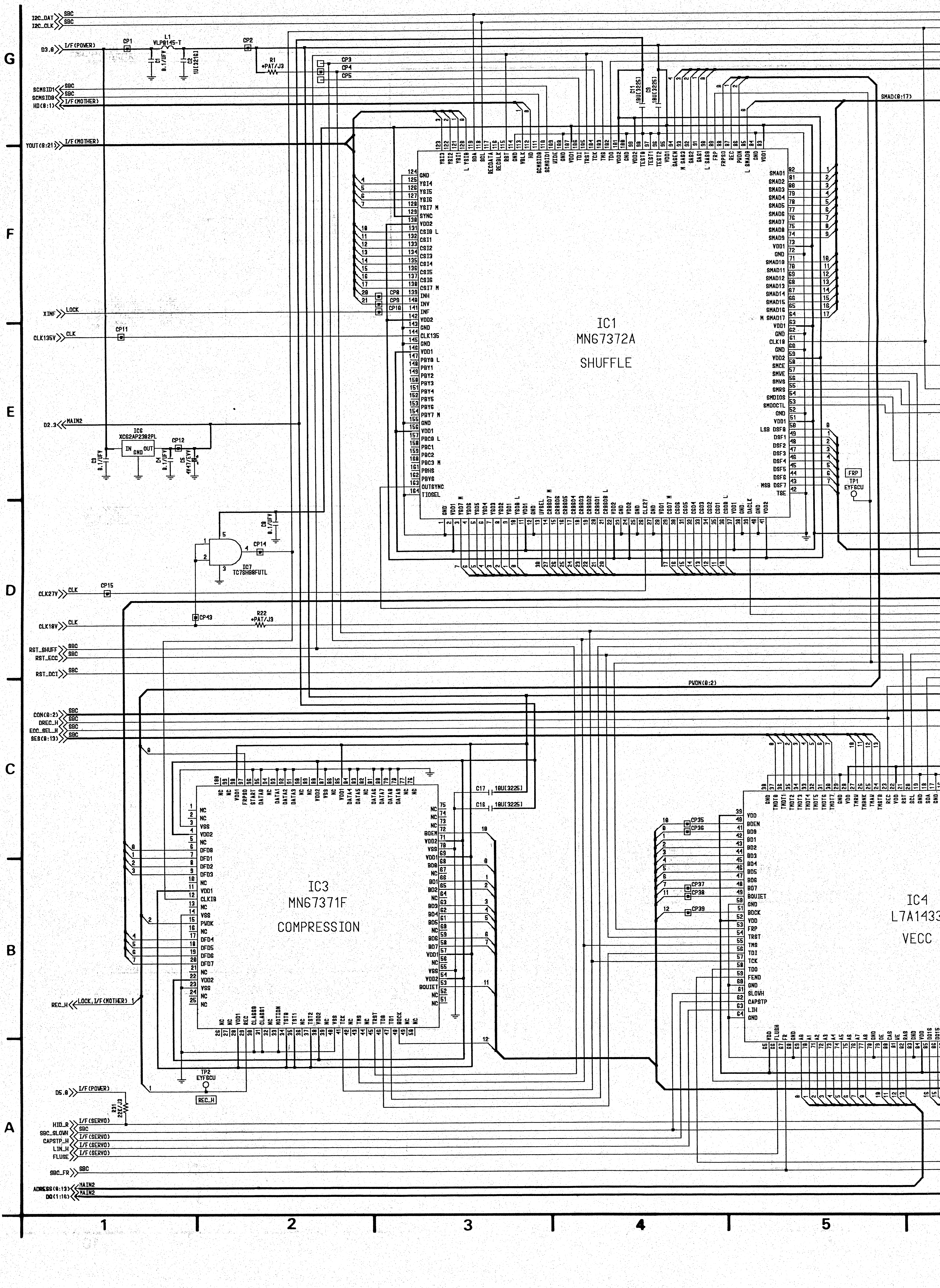
A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9
10
P1
VJS3827C0600
FE_ON_L
RECCTRLA
RECI
REC_CUR_L
REC_FRE_L
PLL_POS
PLL_SL
PLL_VCO
EQ_B_L
EQ_A_L
ATFI
PBH
HID_P
PBCLK
PBDATA
A9.0
A5R6
A-5R6
HID_FE
RECCTRLB
REC_CUR_R
REC_FRE_R
AUTO_EQ
EQ_DL
ATF_GAIN
EQ_B_R
EQ_A_R
REFCK
HID_R
ENV_DET
A3.5
D3.0
IC1
TCVHC125FSEL
IC8
T74VHC125FST
IC2
TC7S04FUTL
IC9
TC7S08FUTL
IC10
TC7W02FUTL
IC11
TC7S04FUTL
R1
10K/J3
P2
VJP3358C012
TEST_L
CLK18M
SBE
SBSTP
D_GND
RP_ENV
PB_ENV
A_GND
EYE_PAT
TEST_CW_L
EXT_CW
RECDATA
RP_ENV
PB_ENV
EYE_PAT
+3VD
FL1
VLF0941C223T
L1
22U/LC
L2
100U/LC
L3
100U/LC
IC3
XC62AP5002PL
IC4
XC62DN5002PL
IC5
XC62AP3002PL
FE_POWER
+5.6VA
+5VA
-5.6VA
-5VA
+3VA
TG1
EYF6CU
P3
VJS3899D013
RP_HEAD_L_P
RP_HEAD_L_N
RP_HEAD_R_P
RP_HEAD_R_N
FE_HEAD_L_P
FE_HEAD_L_N
FE_HEAD_R_P
FE_HEAD_R_N
P4
VJS3898D010
PB_HEAD_R_P
PB_HEAD_R_N
PB_HEAD_L_P
PB_HEAD_L_N
Q1
2SB1114T2ZKL
IC6
XC62AP5002ML
+5ANAPB
QR1
UN5213-TX
Q2
2SD1280-STTX
IC7
XC62DN5002PL
-5ANAPB
Q3
2SB1218AQRTX

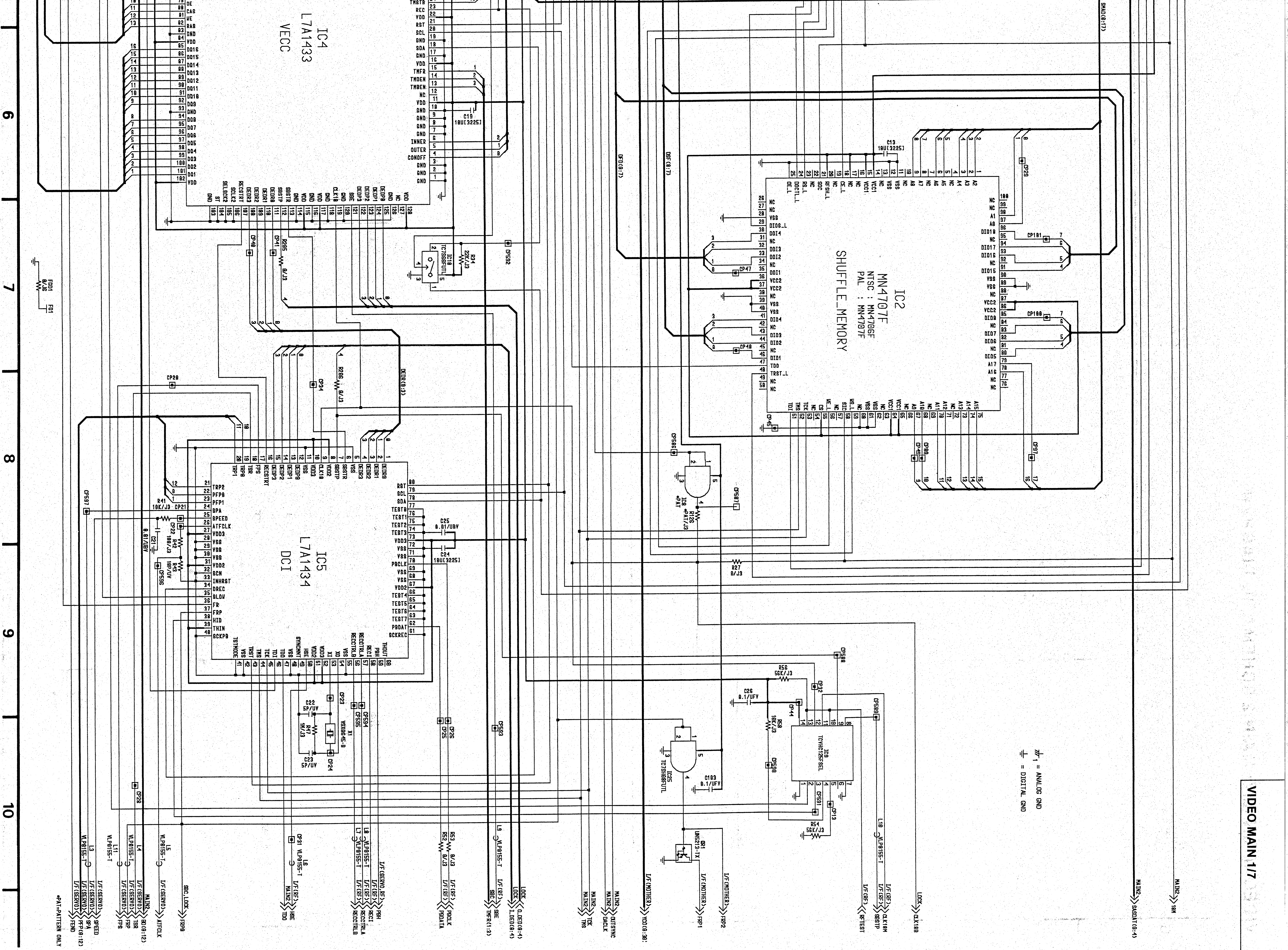
Ref No. 1~99 Series

REVERSE SIDE

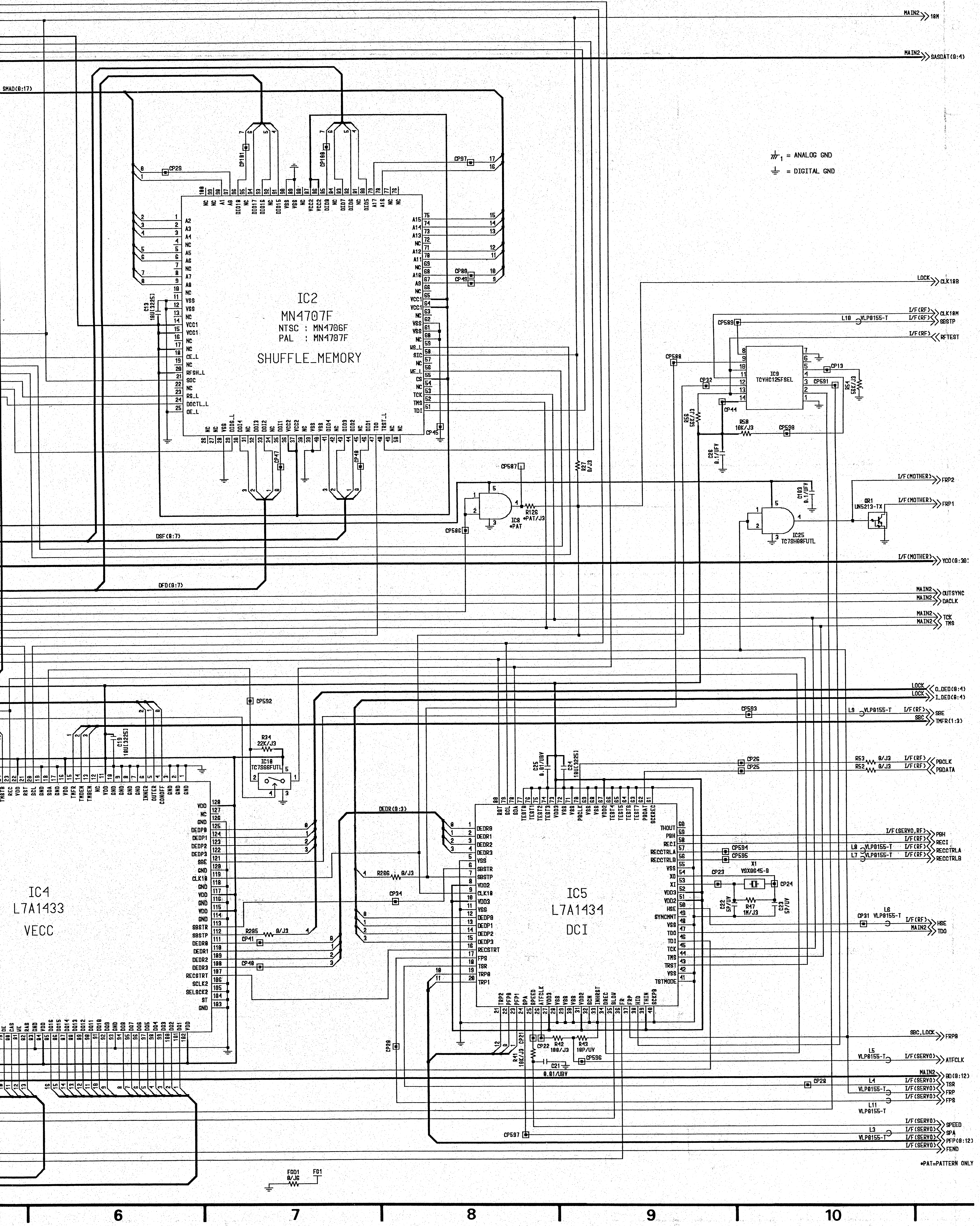
RF 4/5

VIDEO MAIN (1/7) MAIN 1 SCHEMATIC DIAGRAM


G
F
E
D
C
B
A
1
2
3
4
5
I2C_DAT SBC
I2C_CLK SBC
D3.0 I/F(POWER)
CP1
L1 VLP0145-T
C1 0.1/UFV
C2 1U[3216]
CP2
R1 *PAT/J3
CP3
CP4
CP5
SCMSID1 SBC
SCMSID0 SBC
HD(0:1) I/F(MOTHER)
YOUT(0:21) I/F(MOTHER)
SMAD(0:17)
C11 10U[3225]
C9 10U[3225]
XINF LOCK
CLK135V CLK
CP11
D2.3 MAIN2
IC6 XC62AP2302PL
IN GND OUT
CP12
C3 0.1/UFV
C4 0.1/UFV
C5 4V47/EVV
C8 0.1/UFV
CP14
IC7 TC7SH08FUTL
CLK27V CLK
CP15
CLK18V CLK
CP43
R22 *PAT/J3
RST_SHUFF SBC
RST_ECC SBC
RST_DCI SBC
PWDN(0:2)
CON(0:2) SBC
DREC_H SBC
ECC_SEL_H SBC
SE0(0:13) SBC
IC1
MN67372A
SHUFFLE
CP8
CP9
CP10
FRP
TP1 EYF6CU
IC3
MN67371F
COMPRESSION
C17 10U[3225]
C16 10U[3225]
CP35
CP36
CP37
CP38
CP39
IC4
L7A143
VECC
REC_H LOCK,I/F(MOTHER)
TP2 EYF6CU
REC_H
D5.0 I/F(POWER)
R31 22K/J3
HID_R I/F(SERVO)
SBC_SLOWH SBC
CAPSTP_H I/F(SERVO)
LIN_H I/F(SERVO)
FLUSE I/F(SERVO)
SBC_FR SBC
ADRESS(0:13) MAIN2
DQ(1:16) MAIN2


IC4
L7A1433
VECC
IC5
L7A1434
DCI
IC2
MN4707F
NTSC : MN4706F
PAL : MN4707F
SHUFFLE_MEMORY
IC10
TC7S66FU
IC8
IC25
IC9
TC74HC125FSEL
X1
Q1
UN5213-TX
= ANALOG GND
= DIGITAL GND
6
7
8
9
10

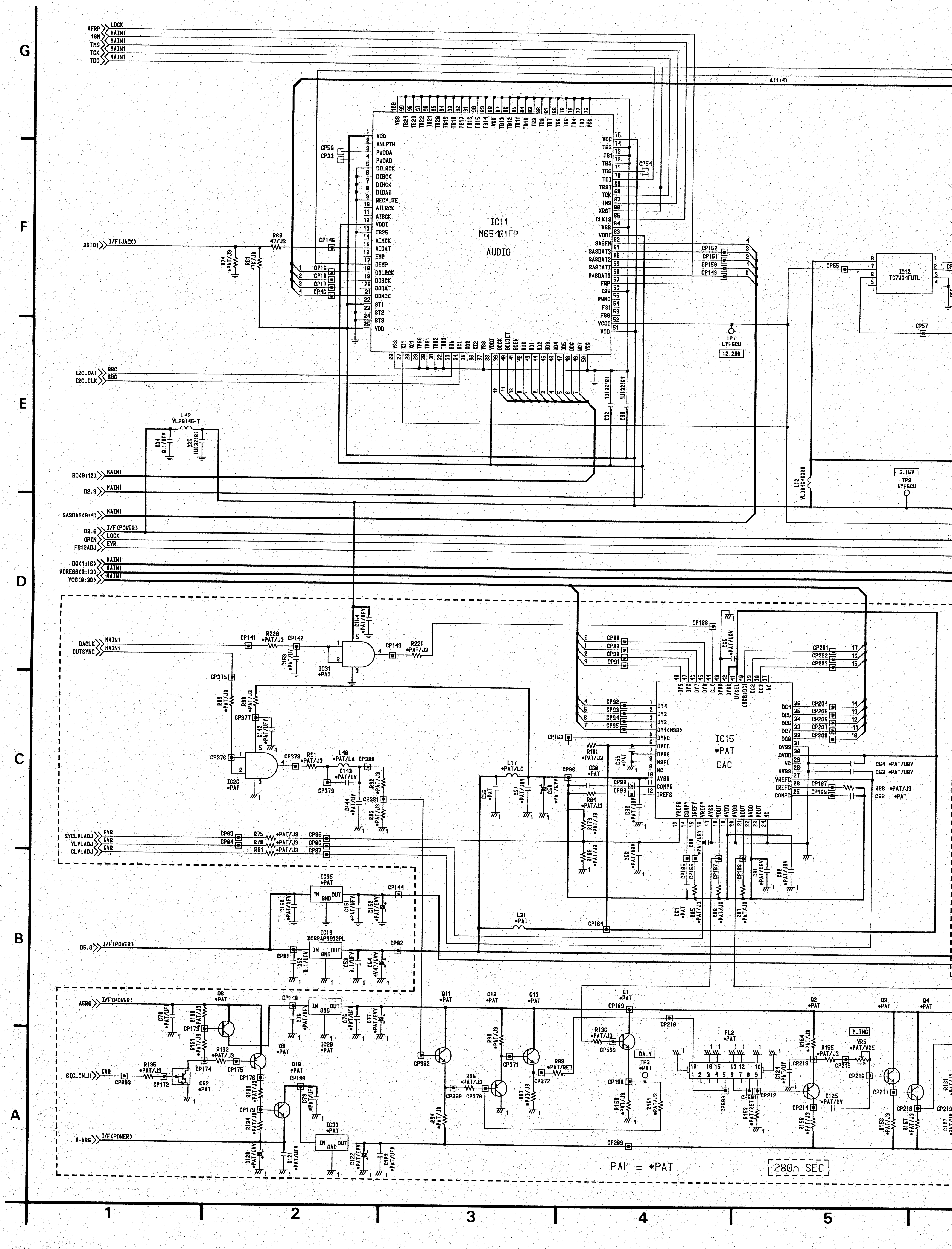
REVERSE SIDE
VIDEO MAIN 2/7

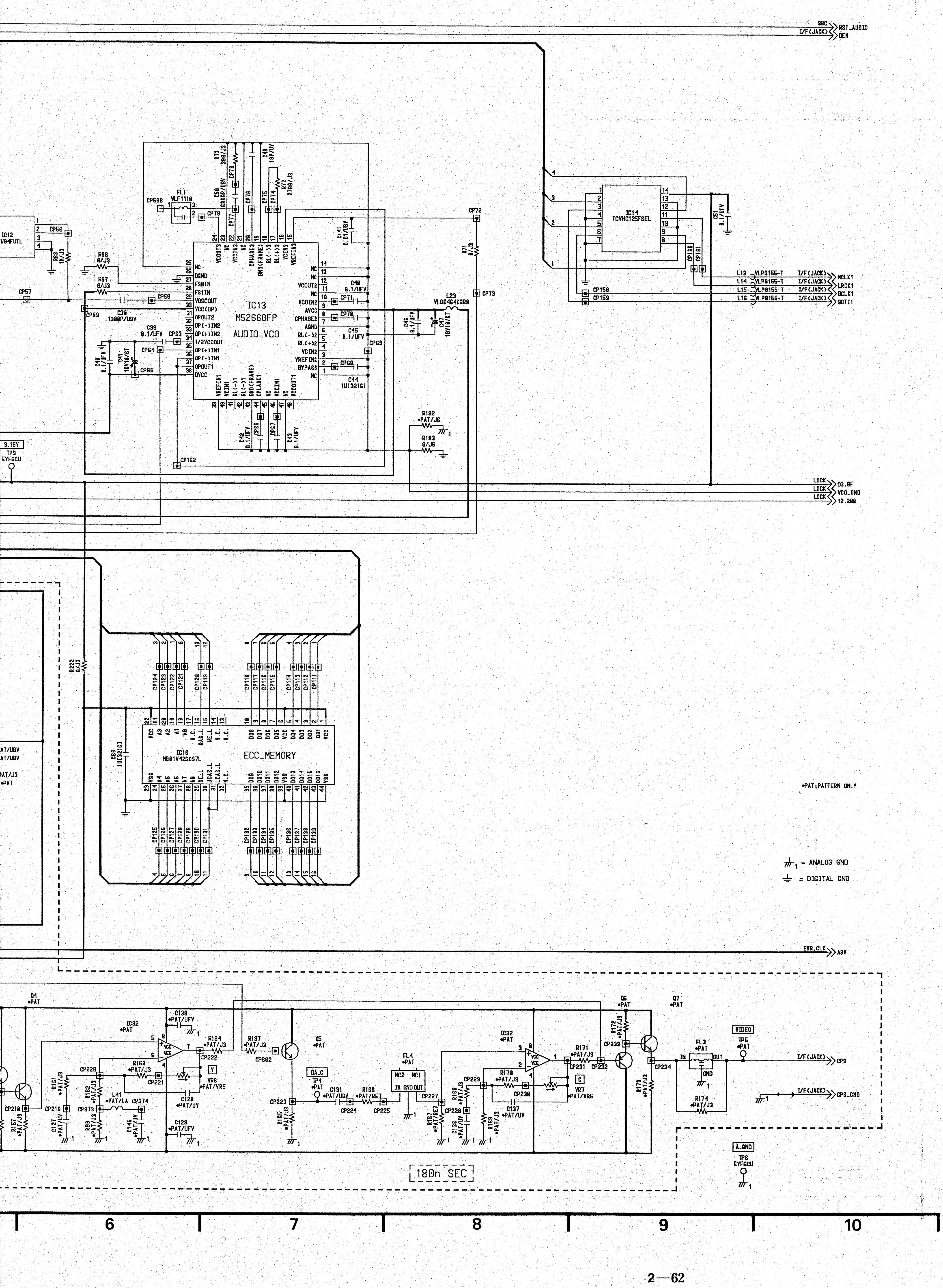

IC2
MN4707F
NTSC : MN4706F
PAL : MN4707F
SHUFFLE_MEMORY
IC4
L7A1433
VECC
IC5
L7A1434
DCI
IC8 *PAT
IC9 TC7WHC125FSEL
IC10 TC7S66FUTL
IC25 TC7SH08FUTL
QR1 UN5213-TX
X1 VSX0645-8
SMAD(0:17)
DSF(0:7)
DFD(0:7)
DEDR(0:3)
= ANALOG GND
= DIGITAL GND
MAIN2 10M
MAIN2 SASDAT(0:4)
LOCK CLK100
I/F(RF) CLK10M
I/F(RF) SBSTP
I/F(RF) RFTEST
I/F(MOTHER) FRP2
I/F(MOTHER) FRP1
I/F(MOTHER) YCO(0:30)
MAIN2 OUTSYNC
MAIN2 DACLK
MAIN2 TCK
MAIN2 TMS
LOCK O_DED(0:4)
LOCK I_DED(0:4)
I/F(RF) SBE
SBC TMFR(1:3)
I/F(RF) PBCLK
I/F(RF) PBDATA
I/F(SERVO,RF) PBH
I/F(RF) RECI
I/F(RF) RECCTRLA
I/F(RF) RECCTRLB
I/F(RF) HSE
MAIN2 TDO
SBC,LOCK FRP0
I/F(SERVO) ATFCLK
MAIN2 BD(0:12)
I/F(SERVO) TSR
I/F(SERVO) FRP
I/F(SERVO) FPS
I/F(SERVO) SPEED
I/F(SERVO) SPA
I/F(SERVO) PFP(0:12)
I/F(SERVO) FEND
*PAT=PATTERN ONLY
6
7
8
9
10

REVERSE SIDE

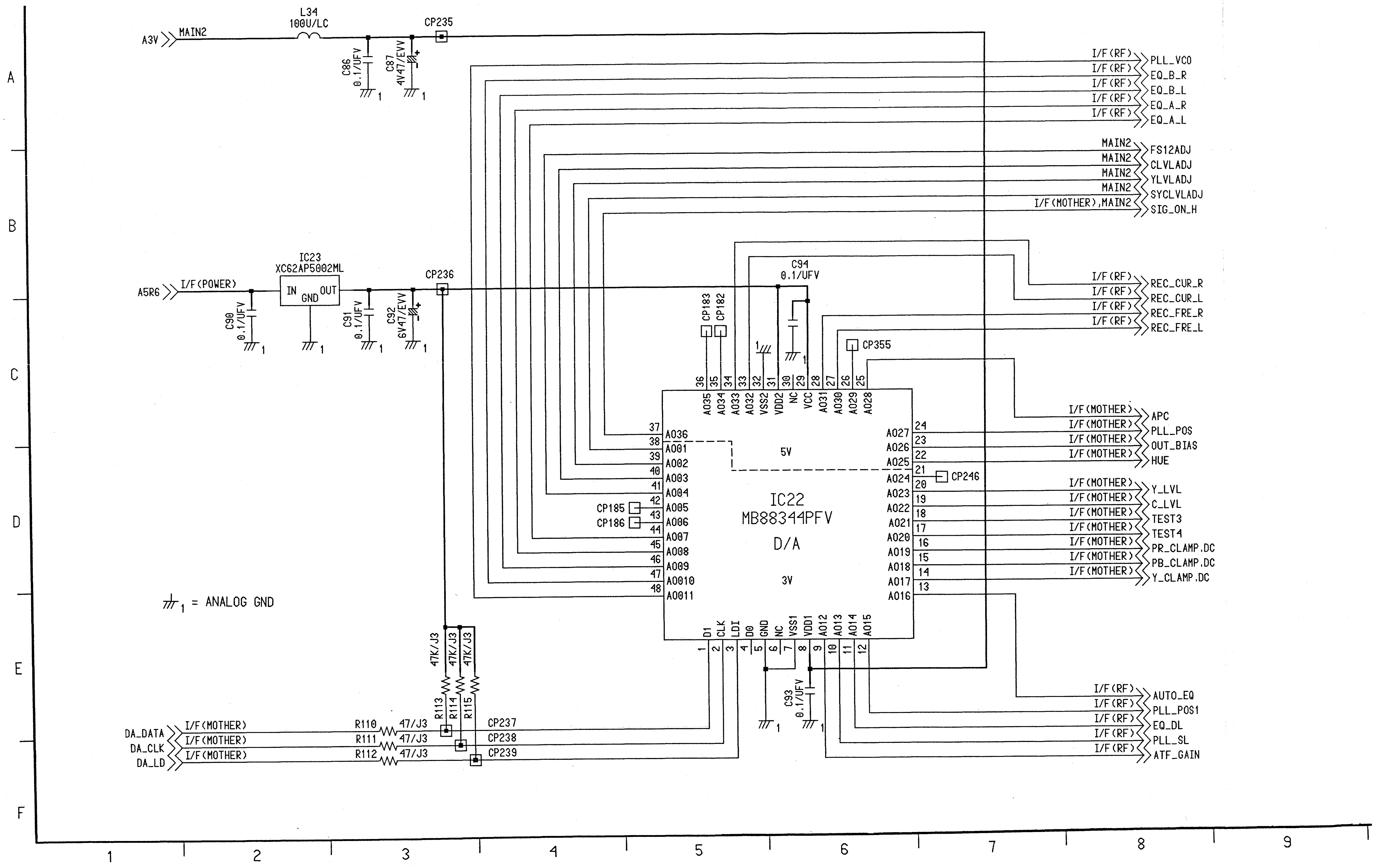
VIDEO MAIN 2/7

VIDEO MAIN (2/7) MAIN 2 SCHEMATIC DIAGRAM

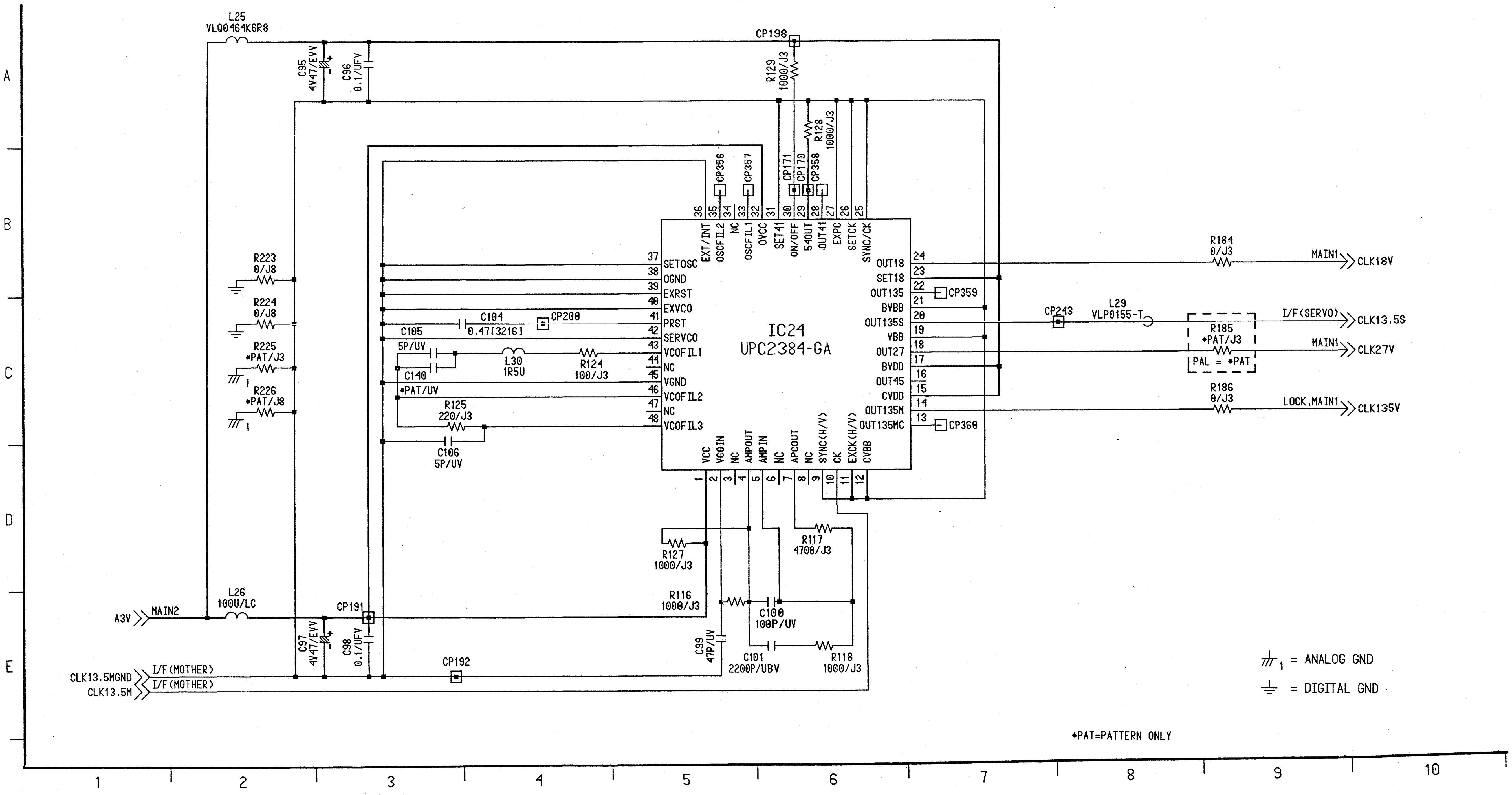

G
F
E
D
C
B
A
1
2
3
4
5
IC11
M65401FP
AUDIO
IC15
*PAT
DAC
IC12
TC7W04FUTL
IC26
*PAT
IC31
*PAT
IC35
*PAT
IC19
XC62AP3002PL
IC30
*PAT
IC20
*PAT
AFRP LOCK
18M MAIN1
TMS MAIN1
TCK MAIN1
TDO MAIN1
SDTO1 I/F(JACK)
I2C_DAT SBC
I2C_CLK SBC
BD(0:12) MAIN1
D2.3 MAIN1
SASDAT(0:4) MAIN1
D3.0 I/F(POWER)
OPIN LOCK
FS12ADJ EVR
DQ(1:16) MAIN1
ADRESS(0:13) MAIN1
YCD(0:30) MAIN1
DACLK MAIN1
OUTSYNC MAIN1
SYCLVLADJ EVR
YLVLADJ EVR
CLVLADJ EVR
D5.0 I/F(POWER)
A5R6 I/F(POWER)
SIG_ON_H EVR
A-5R6 I/F(POWER)
A(1:4)
L42
VLP0145-T
L12
VLD0464KG00
TP7
EYF6CU
12.288
TP9
EYF6CU
3.15V
TP3
*PAT
DA_Y
Y_TMG
FL2
*PAT
PAL = *PAT
280n SEC


IC13
M52660FP
AUDIO_VCO
IC14
TCVHC125FSEL
IC12
V94FUTL
IC16
MB81V4265S7L
ECC_MEMORY
IC32
*PAT
FL1
VLF1118
FL3
*PAT
FL4
*PAT
L23
VLQ0464KSR8
L13 VLP0155-T
L14 VLP0155-T
L15 VLP0155-T
L16 VLP0155-T
SBC
I/F(JACK)
RST_AUDIO
DEM
MCLK1
LRCK1
BCLK1
SDTI1
LOCK
D3.8F
VCO_GND
12.288
EVR_CLK
A3V
VIDEO
TP5
*PAT
I/F(JACK)
CPS
CPS_GND
A_GND
TP6
EYF6CU
3.15V
TP9
EYF6CU
DA_C
TP4
*PAT
180n SEC
Q4
*PAT
Q5
*PAT
Q6
*PAT
Q7
*PAT
VR6
*PAT/VR5
VR7
*PAT/VR5
*PAT=PATTERN ONLY
1 = ANALOG GND
= DIGITAL GND
6
7
8
9
10

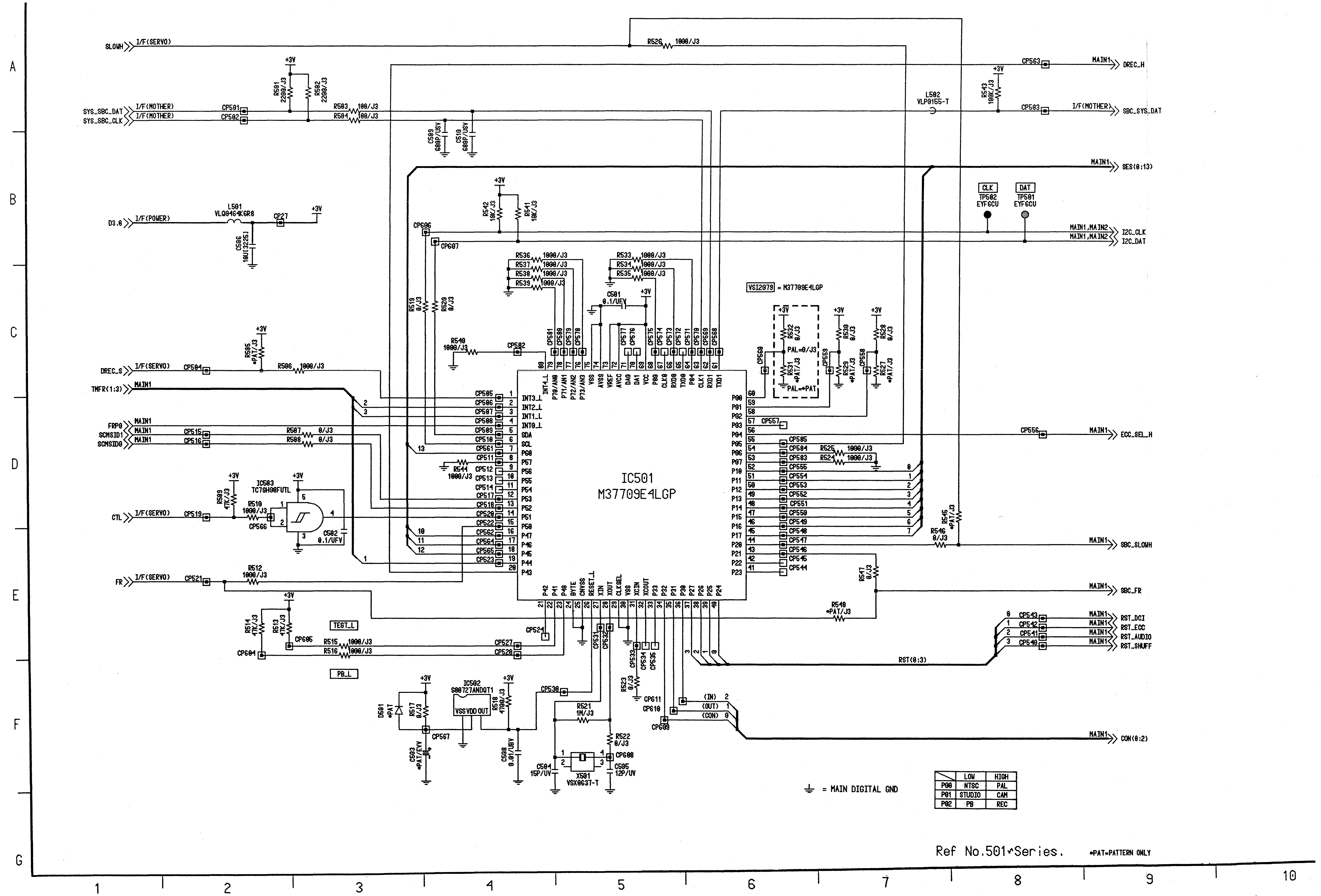
VIDEO MAIN (3/7) EVR SCHEMATIC DIAGRAM


A3V
MAIN2
L34
100U/LC
CP235
C86
0.1/UFV
C87
4V47/EVV
A5R6
I/F(POWER)
IC23
XC62AP5002ML
IN
GND
OUT
CP236
C90
0.1/UFV
C91
0.1/UFV
C92
6V47/EVV
C94
0.1/UFV
CP183
CP182
CP355
CP246
CP185
CP186
IC22
MB88344PFV
D/A
5V
3V
A035
A034
A033
A032
VSS2
VDD2
NC
VCC
A031
A030
A029
A028
A036
A001
A002
A003
A004
A005
A006
A007
A008
A009
A0010
A0011
A027
A026
A025
A024
A023
A022
A021
A020
A019
A018
A017
A016
D1
CLK
LDI
D0
GND
NC
VSS1
VDD1
A012
A013
A014
A015
C93
0.1/UFV
47K/J3
R113
R114
R115
R110
R111
R112
47/J3
CP237
CP238
CP239
DA_DATA
DA_CLK
DA_LD
I/F(MOTHER)
I/F(RF)
PLL_VCO
EQ_B_R
EQ_B_L
EQ_A_R
EQ_A_L
MAIN2
FS12ADJ
CLVLADJ
YLVLADJ
SYCLVLADJ
I/F(MOTHER),MAIN2
SIG_ON_H
REC_CUR_R
REC_CUR_L
REC_FRE_R
REC_FRE_L
APC
PLL_POS
OUT_BIAS
HUE
Y_LVL
C_LVL
TEST3
TEST4
PR_CLAMP.DC
PB_CLAMP.DC
Y_CLAMP.DC
AUTO_EQ
PLL_POS1
EQ_DL
PLL_SL
ATF_GAIN
1 = ANALOG GND
A
B
C
D
E
F
1
2
3
4
5
6
7
8
9

VIDEO MAIN (4/7) SYNC CLK SCHEMATIC DIAGRAM


A
B
C
D
E
1
2
3
4
5
6
7
8
9
10
L25
VLQ0464K6R8
C95
4V47/EVV
C96
0.1/UFV
CP198
R129
1000/J3
R128
1000/J3
CP356
CP357
CP171
CP170
CP358
IC24
UPC2384-GA
EXT/INT
OSCFIL2
NC
OSCFIL1
OVCC
SET41
ON/OFF
54OUT
OUT41
EXPC
SETCK
SYNC/CK
SETOSC
OGND
EXRST
EXVCO
PRST
SERVCO
VCOFIL1
NC
VGND
VCOFIL2
NC
VCOFIL3
OUT18
SET18
OUT135
BVBB
OUT135S
VBB
OUT27
BVDD
OUT45
CVDD
OUT135M
OUT135MC
VCC
VCOIN
NC
AMPOUT
AMPIN
NC
APCOUT
NC
SYNC(H/V)
CK
EXCK(H/V)
CVBB
CP359
CP360
CP200
C104
0.47[3216]
C105
5P/UV
C140
*PAT/UV
L30
1R5U
R124
100/J3
R125
220/J3
C106
5P/UV
R223
0/J8
R224
0/J8
R225
*PAT/J3
R226
*PAT/J8
R127
1000/J3
R116
1000/J3
R117
4700/J3
C100
100P/UV
C99
47P/UV
C101
2200P/UBV
R118
1000/J3
L26
100U/LC
CP191
CP192
C97
4V47/EVV
C98
0.1/UFV
A3V
MAIN2
CLK13.5MGND
CLK13.5M
I/F(MOTHER)
I/F(MOTHER)
R184
0/J3
MAIN1
CLK18V
CP243
L29
VLP0155-T
R185
*PAT/J3
PAL = *PAT
I/F(SERVO)
CLK13.5S
MAIN1
CLK27V
R186
0/J3
LOCK,MAIN1
CLK135V
= ANALOG GND
= DIGITAL GND
*PAT=PATTERN ONLY

VIDEO MAIN (5/7) SBC SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9
10
SLOWH
I/F(SERVO)
R526 1000/J3
SYS_SBC_DAT
SYS_SBC_CLK
I/F(MOTHER)
CP501
CP502
+3V
R501 2200/J3
R502 2200/J3
R503 100/J3
R504 100/J3
C509 680P/USV
C510 680P/USV
L502 VLP0155-T
R543 100K/J3
CP563
CP503
MAIN1
DREC_H
SBC_SYS_DAT
SES(0:13)
D3.8
I/F(POWER)
L501 VLQ0464K6R8
CP27
C596 10U(3225)
R542 10K/J3
R541 10K/J3
CP606
CP607
CLK
TP502 EYF6CU
DAT
TP501 EYF6CU
MAIN1,MAIN2
I2C_CLK
I2C_DAT
R536 1000/J3
R537 1000/J3
R538 1000/J3
R539 1000/J3
R533 1000/J3
R534 1000/J3
R535 1000/J3
C501 0.1/UFV
VSI2079 = M37709E4LGP
R519 0/J3
R520 0/J3
R540 1000/J3
CP582
R532 0/J3
PAL=0/J3
R531 *PAT/J3
PAL=*PAT
R530 0/J3
R528 0/J3
R529 *PAT/J3
R527 *PAT/J3
CP560
CP559
CP558
R505 *PAT/J3
DREC_S
CP504
R506 1000/J3
TMFR(1:3)
FRP0
SCMSID1
SCMSID0
CP515
CP516
R507 0/J3
R508 0/J3
R544 1000/J3
IC501
M37709E4LGP
INT3_L
INT2_L
INT1_L
INT0_L
SDA
SCL
P00
P01
P02
P03
P04
P05
P06
P07
P10
P11
P12
P13
P14
P15
P16
P17
P20
P21
P22
P23
VSS
AVSS
VREF
AVCC
DA0
DA1
VCC
P80
CLK0
RXD0
TXD0
P84
CLK1
RXD1
TXD1
P42
P41
P40
BYTE
CNVSS
RESET_L
XIN
XOUT
CLKSEL
XCIN
XCOUT
P24
P25
P26
P27
CP557
CP556
ECC_SEL_H
R525 1000/J3
R524 1000/J3
R545 *PAT/J3
R546 0/J3
SBC_SLOWH
R547 0/J3
SBC_FR
R548 *PAT/J3
CP543
CP542
CP541
CP540
RST_DCI
RST_ECC
RST_AUDIO
RST_SHUFF
RST(0:3)
IC503 TC7SH08FUTL
R593 4TK/J3
R510 1000/J3
CP566
C502 0.1/UFV
CTL
CP519
FR
CP521
R512 1000/J3
R514 4TK/J3
R513 4TK/J3
CP605
CP604
R515 1000/J3
R516 1000/J3
CP527
CP528
CP524
TEST_L
PB_L
D501 *PAT
R517 0/J3
IC502 S80727ANDOT1
VSS VDD OUT
R518 4700/J3
CP567
C503 *PAT/EVW
C508 0.01/UBV
CP538
R521 1M/J3
C504 15P/UV
X501 VSX0637-T
C505 12P/UV
R522 0/J3
CP608
CP531
CP532
R523 0/J3
CP533
CP534
CP535
CP611
CP610
CP609
(IN)
(OUT)
(CON)
CON(0:2)

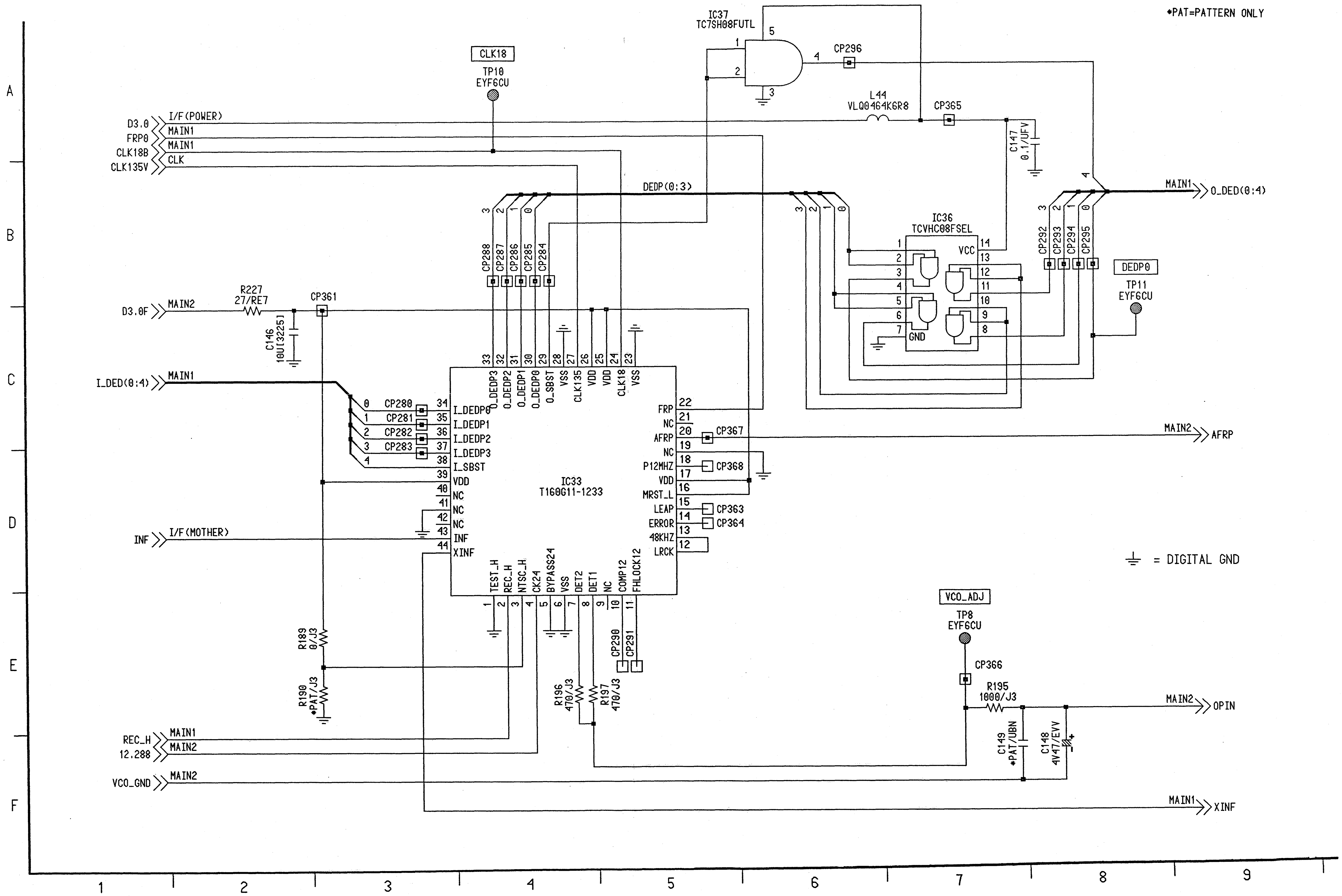
	LOW	HIGH
P00	NTSC	PAL
P01	STUDIO	CAM
P02	PB	REC

⏚ = MAIN DIGITAL GND

Ref No.501✓Series.

*PAT=PATTERN ONLY

VIDEO MAIN (6/7) LOCK SCHEMATIC DIAGRAM

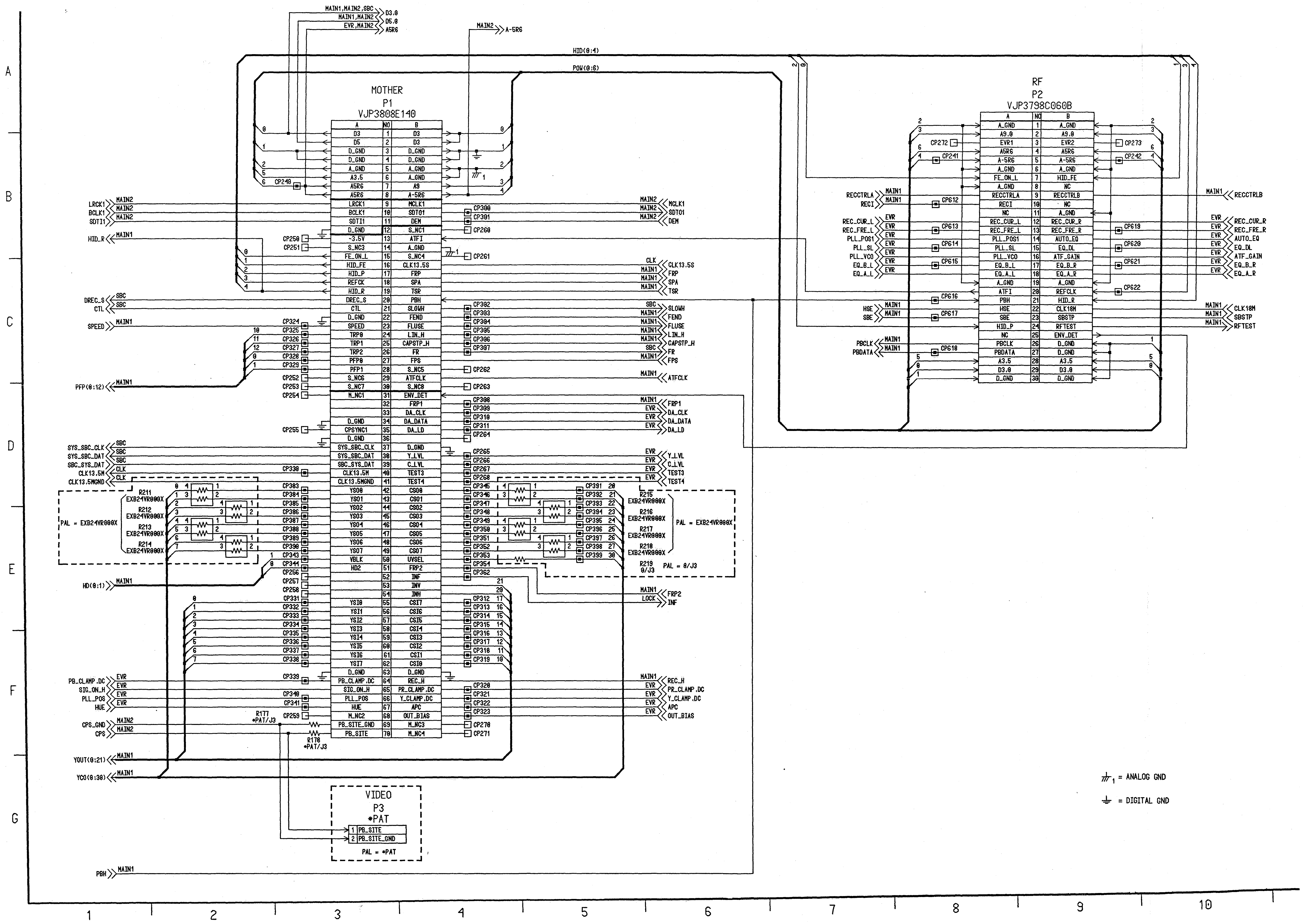


✱PAT=PATTERN ONLY
IC37
TC7SH08FUTL
CP296
L44
VLQ0464K6R8
CP365
C147
0.1/UFV
CLK18
TP10
EYF6CU
D3.0
FRP0
CLK18B
CLK135V
I/F(POWER)
MAIN1
MAIN1
CLK
DEDP(0:3)
MAIN1
O_DED(0:4)
IC36
TCVHC08FSEL
VCC
GND
CP292
CP293
CP294
CP295
DEDP0
TP11
EYF6CU
CP288
CP287
CP286
CP285
CP284
D3.0F
MAIN2
R227
27/RE7
CP361
C146
10U(3225)
I_DED(0:4)
MAIN1
CP280
CP281
CP282
CP283
IC33
T160G11-1233
O_DEDP3
O_DEDP2
O_DEDP1
O_DEDP0
O_SBST
VSS
CLK135
VDD
VDD
CLK18
VSS
I_DEDP0
I_DEDP1
I_DEDP2
I_DEDP3
I_SBST
VDD
NC
NC
NC
INF
XINF
FRP
NC
AFRP
NC
P12MHZ
VDD
MRST_L
LEAP
ERROR
48KHZ
LRCK
TEST_H
REC_H
NTSC_H
CK24
BYPASS24
VSS
DET2
DET1
NC
COMP12
FHLOCK12
CP367
CP368
CP363
CP364
MAIN2
AFRP
INF
I/F(MOTHER)
= DIGITAL GND
VCO_ADJ
TP8
EYF6CU
CP366
R195
1000/J3
MAIN2
OPIN
C149
✱PAT/UBN
C148
4V47/EVV
R189
0/J3
R190
✱PAT/J3
R196
470/J3
R197
470/J3
CP290
CP291
REC_H
12.288
MAIN1
MAIN2
VCO_GND
MAIN2
MAIN1
XINF
A
B
C
D
E
F
1
2
3
4
5
6
7
8
9

REVERSE SIDE

VIDEO MAIN 5/7

VIDEO MAIN (7/7) I/F SCHEMATIC DIAGRAM


MOTHER
P1
VJP3808E140
RF
P2
VJP3798C060B
VIDEO
P3
*PAT
1 PB_SITE
2 PB_SITE_GND
PAL = *PAT
HID(0:4)
POW(0:6)
MAIN1,MAIN2,SBC D3.0
MAIN1,MAIN2 D5.0
EVR,MAIN2 A5R6
MAIN2 A-5R6
LRCK1 MAIN2
BCLK1 MAIN2
SDTI1 MAIN2
HID_R MAIN1
DREC_S SBC
CTL SBC
SPEED MAIN1
PFP(0:12) MAIN1
SYS_SBC_CLK SBC
SYS_SBC_DAT SBC
SBC_SYS_DAT SBC
CLK13.5M CLK
CLK13.5MGND CLK
PAL = EXB24VR000X
R211 EXB24VR000X
R212 EXB24VR000X
R213 EXB24VR000X
R214 EXB24VR000X
R215 EXB24VR000X
R216 EXB24VR000X
R217 EXB24VR000X
R218 EXB24VR000X
R219 0/J3
PAL = 0/J3
HD(0:1) MAIN1
PB_CLAMP.DC EVR
SIG_ON_H EVR
PLL_POS EVR
HUE EVR
CPS_GND MAIN2
CPS MAIN2
YOUT(0:21) MAIN1
YCO(0:30) MAIN1
PBH MAIN1
R177 *PAT/J3
R178 *PAT/J3
MAIN2 MCLK1
MAIN2 SDTO1
MAIN2 DEM
CLK CLK13.5S
MAIN1 FRP
MAIN1 SPA
MAIN1 TSR
SBC SLOWH
MAIN1 FEND
MAIN1 FLUSE
MAIN1 LIN_H
MAIN1 CAPSTP_H
SBC FR
MAIN1 FPS
MAIN1 ATFCLK
MAIN1 FRP1
EVR DA_CLK
EVR DA_DATA
EVR DA_LD
EVR Y_LVL
EVR C_LVL
EVR TEST3
EVR TEST4
MAIN1 FRP2
LOCK INF
MAIN1 REC_H
EVR PR_CLAMP.DC
EVR Y_CLAMP.DC
EVR APC
EVR OUT_BIAS
RECCTRLA MAIN1
RECI MAIN1
REC_CUR_L EVR
REC_FRE_L EVR
PLL_POS1 EVR
PLL_SL EVR
PLL_VCO EVR
EQ_B_L EVR
EQ_A_L EVR
HSE MAIN1
SBE MAIN1
PBCLK MAIN1
PBDATA MAIN1
MAIN1 RECCTRLB
EVR REC_CUR_R
EVR REC_FRE_R
EVR AUTO_EQ
EVR EQ_DL
EVR ATF_GAIN
EVR EQ_B_R
EVR EQ_A_R
MAIN1 CLK18M
MAIN1 SBSTP
MAIN1 RFTEST
= ANALOG GND
= DIGITAL GND
A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9
10

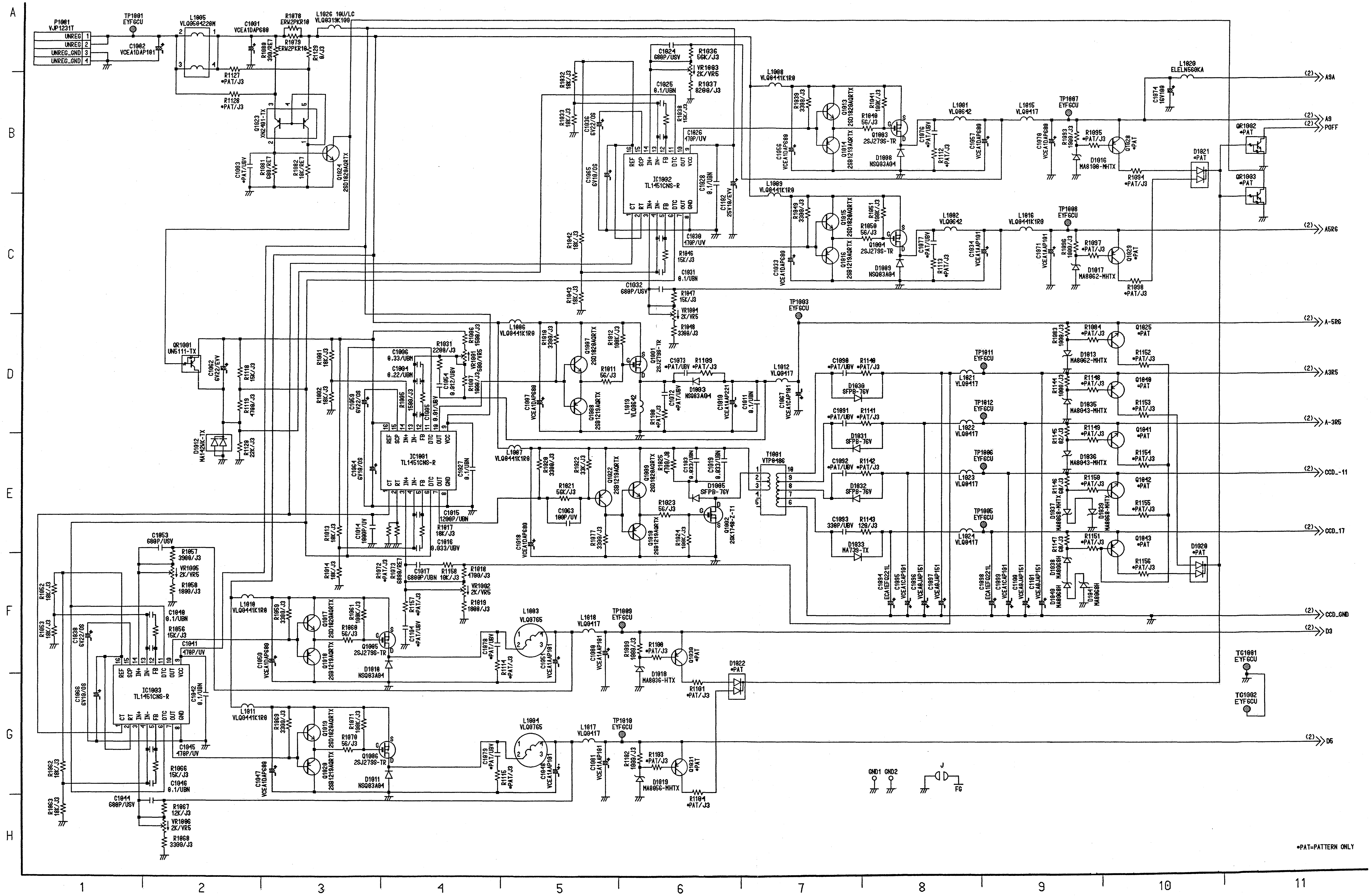
P1 (MOTHER):

A	NO	B
D3	1	D3
D5	2	D3
D_GND	3	D_GND
D_GND	4	D_GND
A_GND	5	A_GND
A3.5	6	A_GND
A5R6	7	A9
A5R6	8	A-5R6
LRCK1	9	MCLK1
BCLK1	10	SDTO1
SDTI1	11	DEM
D_GND	12	S_NC1
-3.5V	13	ATFI
S_NC3	14	A_GND
FE_ON_L	15	S_NC4
HID_FE	16	CLK13.5S
HID_P	17	FRP
REFCK	18	SPA
HID_R	19	TSR
DREC_S	20	PBH
CTL	21	SLOWH
D_GND	22	FEND
SPEED	23	FLUSE
TRP0	24	LIN_H
TRP1	25	CAPSTP_H
TRP2	26	FR
PFP0	27	FPS
PFP1	28	S_NC5
S_NC6	29	ATFCLK
S_NC7	30	S_NC8
M_NC1	31	ENV_DET
	32	FRP1
	33	DA_CLK
D_GND	34	DA_DATA
CPSYNC1	35	DA_LD
D_GND	36	
SYS_SBC_CLK	37	D_GND
SYS_SBC_DAT	38	Y_LVL
SBC_SYS_DAT	39	C_LVL
CLK13.5M	40	TEST3
CLK13.5MGND	41	TEST4
YS00	42	CS00
YS01	43	CS01
YS02	44	CS02
YS03	45	CS03
YS04	46	CS04
YS05	47	CS05
YS06	48	CS06
YS07	49	CS07
VBLK	50	UVSEL
HD2	51	FRP2
	52	INF
	53	INV
	54	INH
YSI0	55	CSI7
YSI1	56	CSI6
YSI2	57	CSI5
YSI3	58	CSI4
YSI4	59	CSI3
YSI5	60	CSI2
YSI6	61	CSI1
YSI7	62	CSI0
D_GND	63	D_GND
PB_CLAMP.DC	64	REC_H
SIG_ON_H	65	PR_CLAMP.DC
PLL_POS	66	Y_CLAMP.DC
HUE	67	APC
M_NC2	68	OUT_BIAS
PB_SITE_GND	69	M_NC3
PB_SITE	70	M_NC4

P2 (RF):

A	NO	B
A_GND	1	A_GND
A9.0	2	A9.0
EVR1	3	EVR2
A5R6	4	A5R6
A-5R6	5	A-5R6
A_GND	6	A_GND
FE_ON_L	7	HID_FE
A_GND	8	NC
RECCTRLA	9	RECCTRLB
RECI	10	NC
NC	11	A_GND
REC_CUR_L	12	REC_CUR_R
REC_FRE_L	13	REC_FRE_R
PLL_POS1	14	AUTO_EQ
PLL_SL	15	EQ_DL
PLL_VCO	16	ATF_GAIN
EQ_B_L	17	EQ_B_R
EQ_A_L	18	EQ_A_R
A_GND	19	A_GND
ATFI	20	REFCLK
PBH	21	HID_R
HSE	22	CLK18M
SBE	23	SBSTP
HID_P	24	RFTEST
NC	25	ENV_DET
PBCLK	26	D_GND
PBDATA	27	D_GND
A3.5	28	A3.5
D3.0	29	D3.0
D_GND	30	D_GND

POWER (1/2) SCHEMATIC DIAGRAM



P1001
VJP1231T
UNREG
UNREG
UNREG_GND
UNREG_GND
TP1001
EYF6CU
C1002
VCEA1DAP101
L1005
VLQ0584228M
C1001
VCEA1DAP680
R1078
ERW2PKR10
R1079
ERW2PKR10
L1026 10U/LC
VLQ0319K100
R1127
*PAT/J3
R1128
*PAT/J3
Q1023
XN2401-TX
Q1024
2SD1820AQRTX
IC1002
TL1451CNS-R
C1024
680P/USV
R1036
56K/J3
VR1003
2K/VR5
R1037
8200/J3
L1008
VLQ0441K1R0
L1009
VLQ0441K1R0
Q1013
2SD1820AQRTX
Q1014
2SB1219AQRTX
Q1003
2SJ279S-TR
D1008
NSQ03A04
L1001
VLQ0642
L1015
VLQ0417
TP1007
EYF6CU
Q1028
*PAT
D1016
MA8100-MHTX
L1020
ELELN560KA
QR1002
*PAT
QR1003
*PAT
D1021
*PAT
Q1015
2SD1820AQRTX
Q1016
2SB1219AQRTX
Q1004
2SJ279S-TR
D1009
NSQ03A04
L1002
VLQ0642
L1016
VLQ0441K1R0
TP1008
EYF6CU
Q1029
*PAT
D1017
MA8062-MHTX
(2) A9A
(2) A9
(2) POFF
(2) A5R6
(2) A-5R6
(2) A3R5
(2) A-3R5
(2) CCD_-11
(2) CCD_17
(2) CCD_GND
(2) D3
(2) D5
QR1001
UN5111-TX
D1012
MA142WK-TX
IC1001
TL1451CNS-R
L1006
VLQ0441K1R0
Q1007
2SD1820AQRTX
Q1008
2SB1219AQRTX
Q1001
2SJ279S-TR
D1003
NSQ03A04
L1012
VLQ0417
TP1003
EYF6CU
L1007
VLQ0441K1R0
Q1022
2SB1219AQRTX
Q1009
2SD1820AQRTX
Q1010
2SB1219AQRTX
D1005
SFPB-76V
Q1002
2SK1748-Z-T1
T1001
VTP0486
D1030
SFPB-76V
D1031
SFPB-76V
D1032
SFPB-76V
D1033
MA739-TX
TP1011
EYF6CU
L1021
VLQ0417
TP1012
EYF6CU
L1022
VLQ0417
TP1006
EYF6CU
L1023
VLQ0417
TP1005
EYF6CU
L1024
VLQ0417
Q1025
*PAT
D1013
MA8062-MHTX
Q1040
*PAT
D1035
MA8043-MHTX
Q1041
*PAT
D1036
MA8043-MHTX
Q1042
*PAT
Q1043
*PAT
D1020
*PAT
IC1003
TL1451CNS-R
L1010
VLQ0441K1R0
Q1017
2SD1820AQRTX
Q1018
2SB1219AQRTX
Q1005
2SJ279S-TR
D1010
NSQ03A04
L1003
VLQ0765
L1018
VLQ0417
TP1009
EYF6CU
Q1030
*PAT
D1018
MA8036-HTX
D1022
*PAT
L1011
VLQ0441K1R0
Q1019
2SD1820AQRTX
Q1020
2SB1219AQRTX
Q1006
2SJ279S-TR
D1011
NSQ03A04
L1004
VLQ0765
L1017
VLQ0417
TP1010
EYF6CU
Q1031
*PAT
D1019
MA8056-MHTX
TG1001
EYF6CU
TG1002
EYF6CU
GND1
GND2
J
FG
*PAT=PATTERN ONLY
A
B
C
D
E
F
G
H
1
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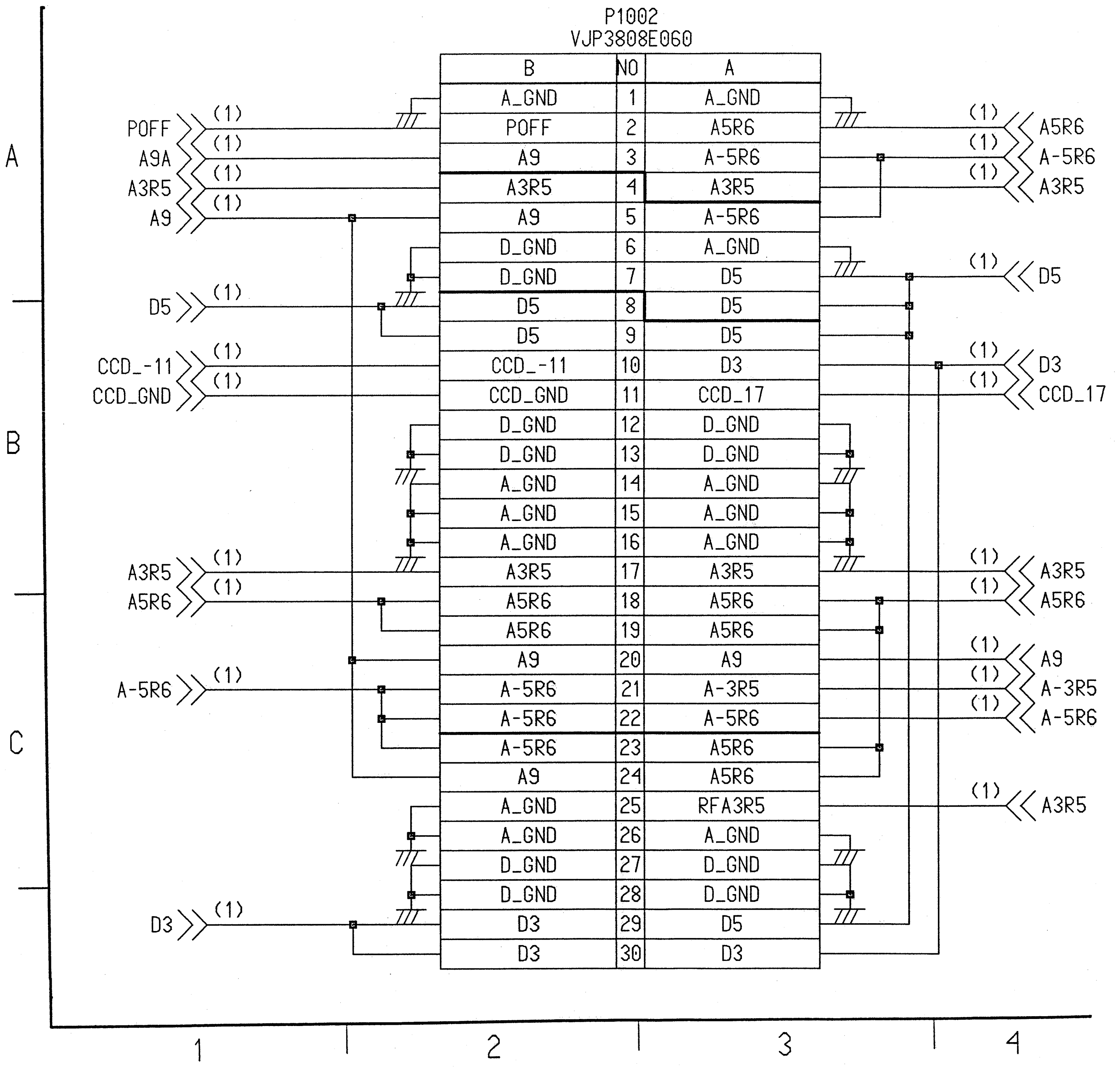
11

REVERSE SIDE

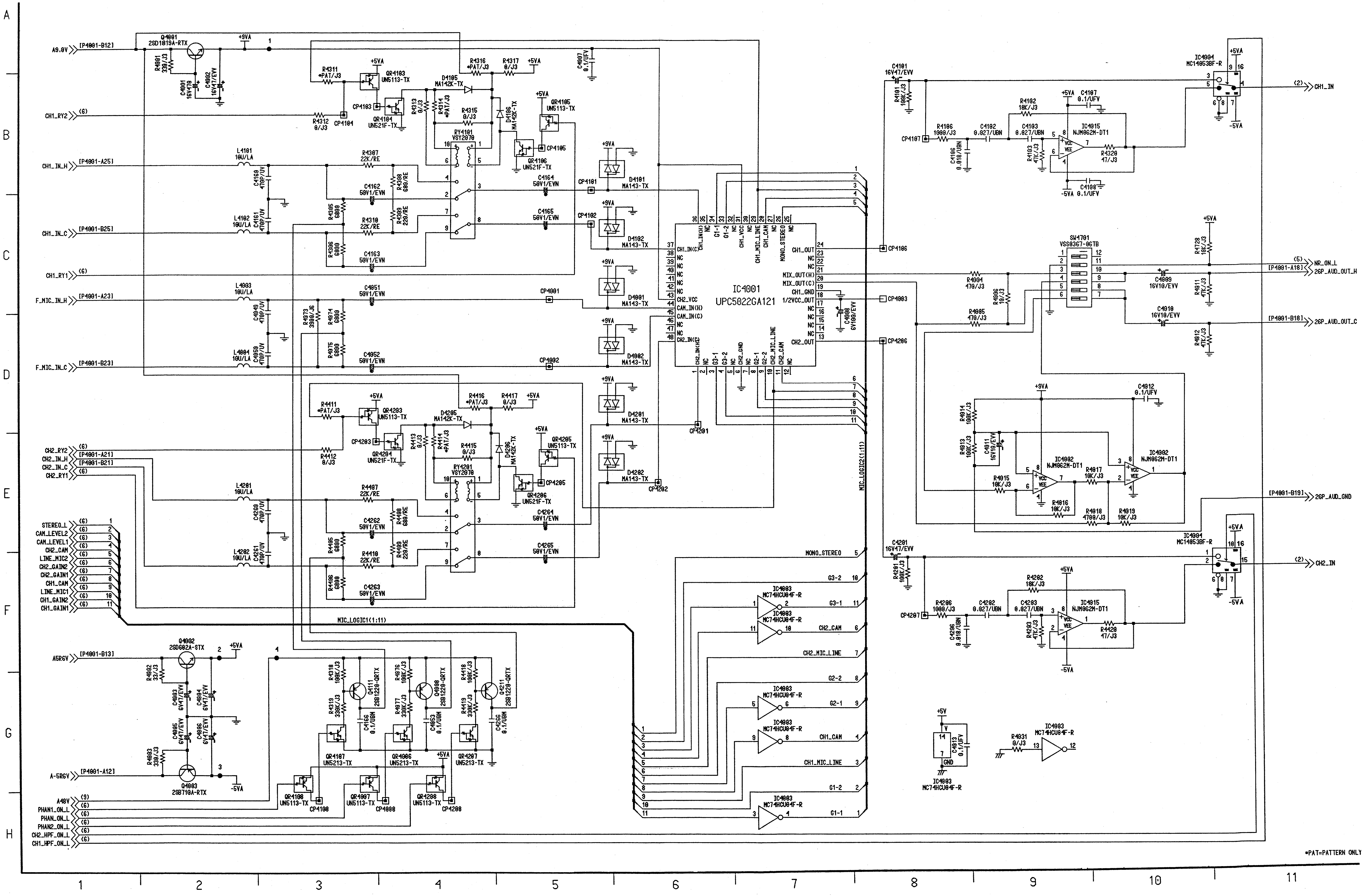
VIDEO MAIN 7/7

POWER (2/2) CONNECTOR SCHEMATIC DIAGRAM


P1002
VJP3808E060
A
B
C
1
2
3
4
POFF
A9A
A3R5
A9
D5
CCD_-11
CCD_GND
A3R5
A5R6
A-5R6
D3
(1)
A5R6
A-5R6
A3R5
D5
D3
CCD_17
A3R5
A5R6
A9
A-3R5
A-5R6
A3R5

B	NO	A
A_GND	1	A_GND
POFF	2	A5R6
A9	3	A-5R6
A3R5	4	A3R5
A9	5	A-5R6
D_GND	6	A_GND
D_GND	7	D5
D5	8	D5
D5	9	D5
CCD_-11	10	D3
CCD_GND	11	CCD_17
D_GND	12	D_GND
D_GND	13	D_GND
A_GND	14	A_GND
A_GND	15	A_GND
A_GND	16	A_GND
A3R5	17	A3R5
A5R6	18	A5R6
A5R6	19	A5R6
A9	20	A9
A-5R6	21	A-3R5
A-5R6	22	A-5R6
A-5R6	23	A5R6
A9	24	A5R6
A_GND	25	RFA3R5
A_GND	26	A_GND
D_GND	27	D_GND
D_GND	28	D_GND
D3	29	D5
D3	30	D3

AUDIO LCD (1/9) AUDIO INPUT SCHEMATIC DIAGRAM

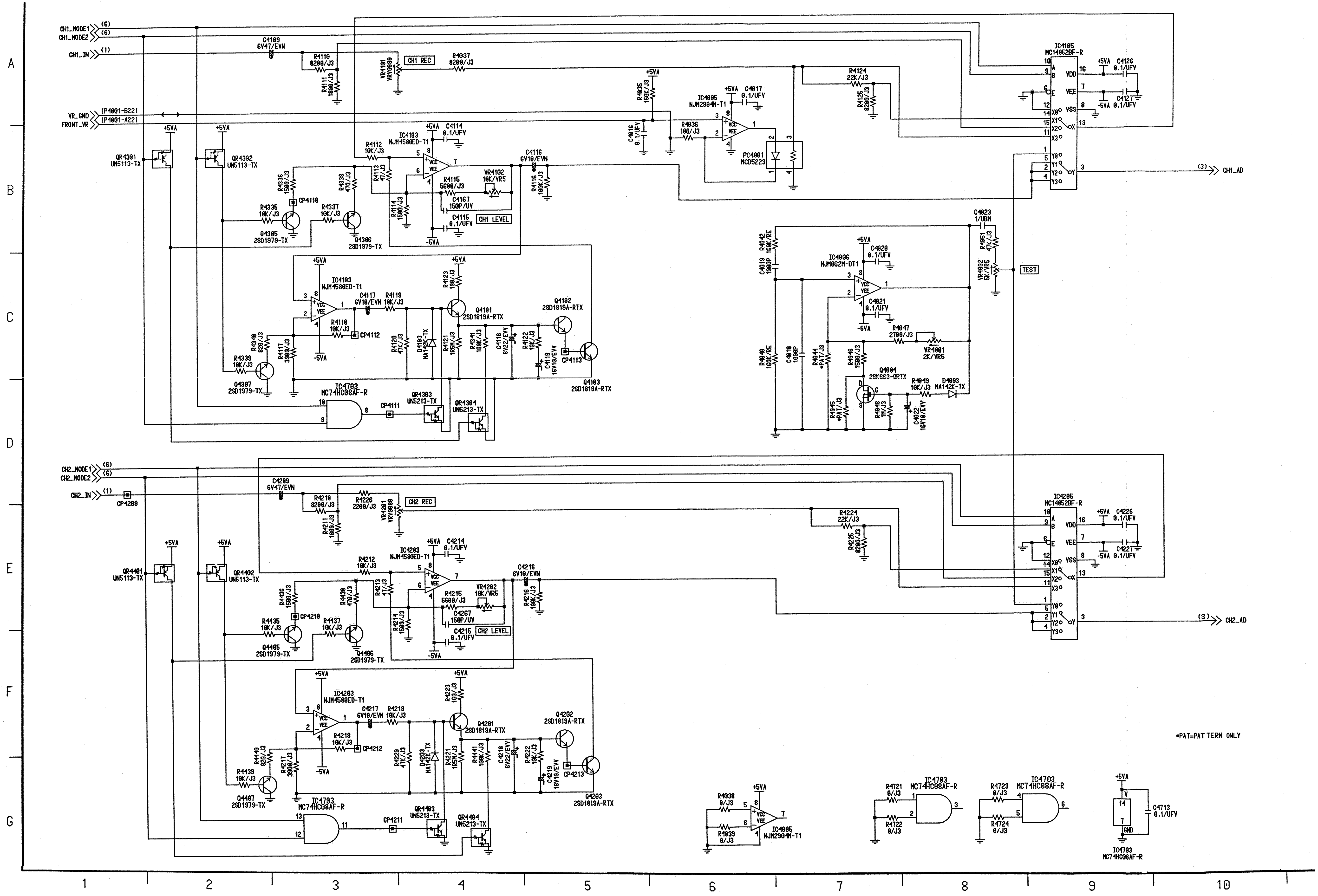

A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
A9.0V [P4001-B12]
Q4001 2SD1819A-RTX
+9VA
CH1_RY2 (6)
CH1_IN_H [P4001-A25]
CH1_IN_C [P4001-B25]
CH1_RY1 (6)
F_MIC_IN_H [P4001-A23]
F_MIC_IN_C [P4001-B23]
CH2_RY2 (6)
CH2_IN_H [P4001-A21]
CH2_IN_C [P4001-B21]
CH2_RY1 (6)
STEREO_L (6)
CAM_LEVEL2 (6)
CAM_LEVEL1 (6)
CH2_CAM (6)
LINE_MIC2 (6)
CH2_GAIN2 (6)
CH2_GAIN1 (6)
CH1_CAM (6)
LINE_MIC1 (6)
CH1_GAIN2 (6)
CH1_GAIN1 (6)
A5R6V [P4001-B13]
Q4002 2SD602A-STX
A-5R6V [P4001-A12]
Q4003 2SB710A-RTX
+5VA
-5VA
A48V (9)
PHAN1_ON_L (6)
PHAN_ON_L (6)
PHAN2_ON_L (6)
CH2_HPF_ON_L (6)
CH1_HPF_ON_L (6)
RY4101 VS12070
RY4201 VS12070
D4105 MA142K-TX
D4205 MA142K-TX
QR4103 UN5113-TX
QR4104 UN521F-TX
QR4105 UN5113-TX
QR4106 UN521F-TX
QR4203 UN5113-TX
QR4204 UN521F-TX
QR4205 UN5113-TX
QR4206 UN521F-TX
D4101 MA143-TX
D4102 MA143-TX
D4001 MA143-TX
D4002 MA143-TX
D4201 MA143-TX
D4202 MA143-TX
L4101 10U/LA
L4102 10U/LA
L4003 10U/LA
L4004 10U/LA
L4201 10U/LA
L4202 10U/LA
IC4001
UPC5022GA121
CH1_IN(C)
CH1_IN(H)
G1-1
G1-2
CH1_VCC
CH1_MIC_LINE
CH1_CAM
MONO_STEREO
CH1_OUT
MIX_OUT(H)
MIX_OUT(C)
CH1_GND
1/2VCC_OUT
CH2_OUT
CH2_VCC
CAM_IN(H)
CAM_IN(C)
CH2_IN(C)
CH2_IN(H)
CH2_GND
G2-1
G2-2
CH2_MIC_LINE
CH2_CAM
MIC_LOGIC2(1:11)
MIC_LOGIC1(1:11)
IC4003 MC74HCU04F-R
Q4111 2SB1228-QRTX
Q4008 2SB1228-QRTX
Q4211 2SB1228-QRTX
QR4107 UN5213-TX
QR4006 UN5213-TX
QR4207 UN5213-TX
QR4108 UN5113-TX
QR4007 UN5113-TX
QR4208 UN5113-TX
CP4108
CP4008
CP4208
IC4004 MC14053BF-R
(2) CH1_IN
(2) CH2_IN
IC4015 NJM062M-DT1
SW4701 VSS0367-06TB
(5) NR_ON_L
[P4001-A18] 2GP_AUD_OUT_H
[P4001-B18] 2GP_AUD_OUT_C
[P4001-B19] 2GP_AUD_GND
IC4002 NJM062M-DT1
CP4106
CP4003
CP4206
CP4107
CP4207
+5V
IC4003 MC74HCU04F-R

*PAT=PATTERN ONLY

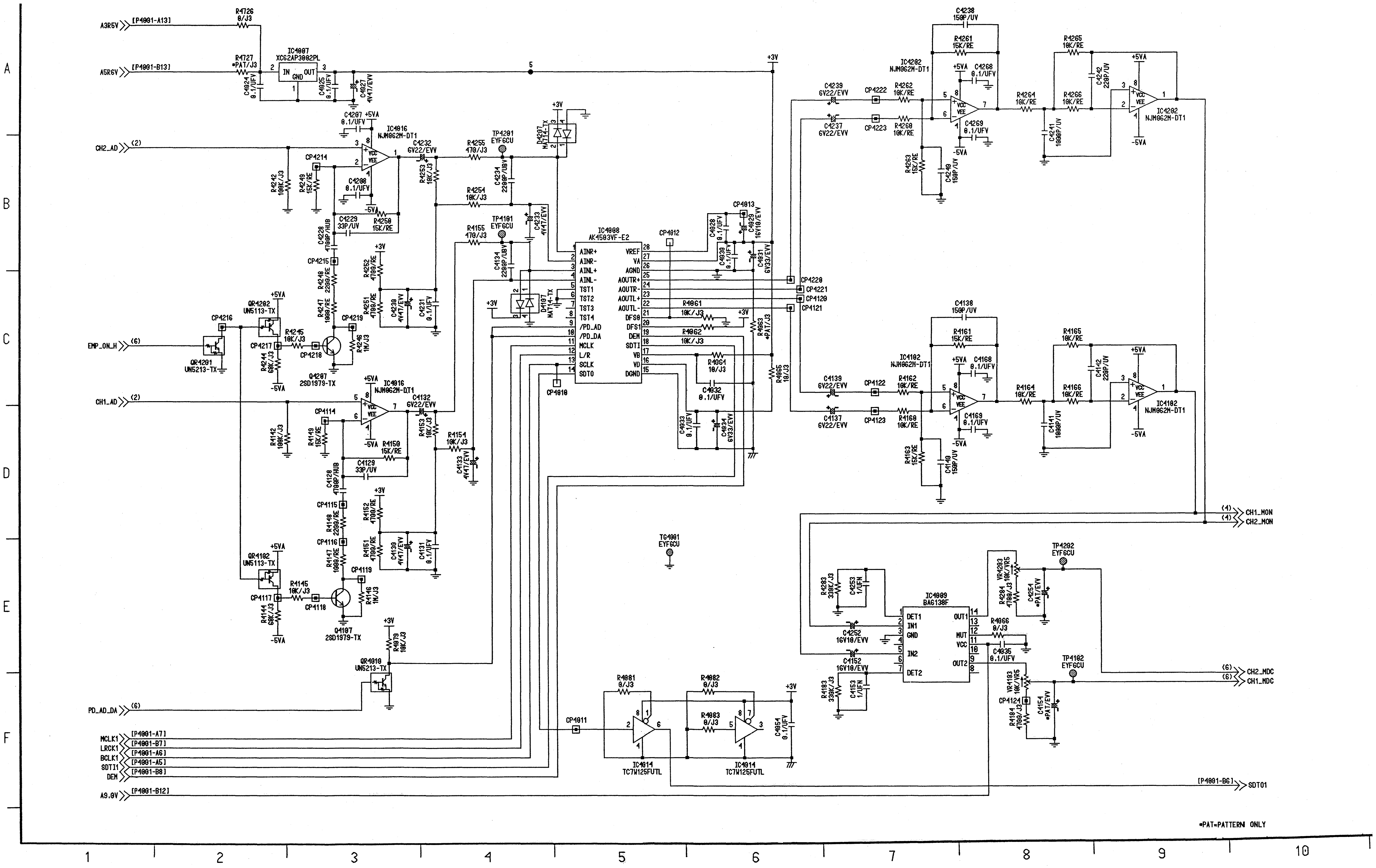
REVERSE SIDE

POWER 2/2

AUDIO LCD (2/9) AUDIO AGC SCHEMATIC DIAGRAM


CH1_MODE1 (6)
CH1_MODE2 (6)
CH1_IN (1)
VR_GND [P4001-B22]
FRONT_VR [P4001-A22]
CH1 REC
CH1 LEVEL
IC4105 MC14052BF-R
IC4103 NJM4580ED-T1
IC4005 NJM2904M-T1
PC4001 MCD5223
IC4703 MC74HC08AF-R
(3) CH1_AD
TEST
IC4006 NJM062M-DT1
Q4004 2SK663-QRTX
CH2_MODE1 (6)
CH2_MODE2 (6)
CH2_IN (1)
CH2 REC
CH2 LEVEL
IC4205 MC14052BF-R
IC4203 NJM4580ED-T1
(3) CH2_AD
*PAT=PATTERN ONLY
A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9
10

AUDIO LCD (3/9) AUDIO A/D D/A SCHEMATIC DIAGRAM


A3R5V
[P4001-A13]
R4726
0/J3
A5R6V
[P4001-B13]
R4727
*PAT/J3
IC4007
XC62AP3002PL
IN
OUT
GND
C4024
0.1/UFV
C4025
0.1/UFV
C4027
4V47/EVV
+3V
C4207 +5VA
0.1/UFV
IC4016
NJM062M-DT1
CH2_AD
(2)
CP4214
C4208
0.1/UFV
R4242
100K/J3
R4249
15K/RE
C4232
6V22/EVV
R4255
470/J3
TP4201
EYF6CU
R4253
10K/J3
D4207
MA714-TX
R4254
10K/J3
C4234
2200P/UBV
C4229
33P/UV
R4250
15K/RE
C4228
4700P/HUB
TP4101
EYF6CU
R4155
470/J3
C4233
4V47/EVV
CP4215
R4248
2200/RE
R4252
4700/RE
C4230
4V47/EVV
C4231
0.1/UFV
C4134
2200P/UBV
D4107
MA714-TX
R4247
1000/RE
R4251
4700/RE
CP4219
R4246
1M/J3
QR4202
UN5113-TX
CP4216
EMP_ON_H
(6)
QR4201
UN5213-TX
CP4217
R4245
10K/J3
CP4218
R4244
68K/J3
Q4207
2SD1979-TX
IC4008
AK4503VF-E2
AINR+
AINR-
AINL+
AINL-
TST1
TST2
TST3
TST4
/PD_AD
/PD_DA
MCLK
L/R
SCLK
SDTO
VREF
VA
AGND
AOUTR+
AOUTR-
AOUTL+
AOUTL-
DFS0
DFS1
DEM
SDTI
VB
VD
DGND
CP4010
CP4012
CP4013
C4028
0.1/UFV
C4029
16V10/EVV
C4030
0.1/UFV
C4031
6V33/EVV
CP4220
CP4221
CP4120
CP4121
R4061
10K/J3
R4062
10K/J3
R4063
*PAT/J3
R4064
10/J3
R4065
10/J3
C4032
0.1/UFV
C4033
0.1/UFV
C4034
6V33/EVV
CH1_AD
(2)
IC4016
NJM062M-DT1
CP4114
C4132
6V22/EVV
R4142
100K/J3
R4149
15K/RE
R4150
15K/RE
R4153
10K/J3
R4154
10K/J3
C4133
4V47/EVV
C4129
33P/UV
C4128
4700P/HUB
CP4115
R4148
2200/RE
R4152
4700/RE
CP4116
R4147
1000/RE
R4151
4700/RE
C4130
4V47/EVV
C4131
0.1/UFV
QR4102
UN5113-TX
CP4117
R4145
10K/J3
CP4118
CP4119
R4146
1M/J3
R4144
68K/J3
Q4107
2SD1979-TX
R4079
10K/J3
QR4010
UN5213-TX
PD_AD_DA
(6)
MCLK1
LRCK1
BCLK1
SDTI1
DEM
[P4001-A7]
[P4001-B7]
[P4001-A6]
[P4001-A5]
[P4001-B8]
A9.0V
[P4001-B12]
C4238
150P/UV
R4261
15K/RE
IC4202
NJM062M-DT1
C4268
0.1/UFV
C4239
6V22/EVV
CP4222
R4262
10K/RE
C4237
6V22/EVV
CP4223
R4260
10K/RE
C4269
0.1/UFV
R4263
15K/RE
C4240
150P/UV
R4265
10K/RE
C4242
220P/UV
R4264
10K/RE
R4266
10K/RE
C4241
1000P/UV
IC4202
NJM062M-DT1
C4138
150P/UV
R4161
15K/RE
IC4102
NJM062M-DT1
C4168
0.1/UFV
C4139
6V22/EVV
CP4122
R4162
10K/RE
C4137
6V22/EVV
CP4123
R4160
10K/RE
C4169
0.1/UFV
R4163
15K/RE
C4140
150P/UV
R4165
10K/RE
C4142
220P/UV
R4164
10K/RE
R4166
10K/RE
C4141
1000P/UV
IC4102
NJM062M-DT1
CH1_MON
CH2_MON
TC4001
EYF6CU
R4203
330K/J3
C4253
1/UFN
IC4009
BA6138F
DET1
IN1
GND
IN2
DET2
OUT1
MUT
VCC
OUT2
C4252
16V10/EVV
C4152
16V10/EVV
R4103
330K/J3
C4153
1/UFN
VR4203
10K/VR5
R4204
4700/J3
C4254
*PAT/EVV
TP4202
EYF6CU
R4066
0/J3
C4035
0.1/UFV
VR4103
10K/VR5
TP4102
EYF6CU
CP4124
R4104
4700/J3
C4154
*PAT/EVV
CH2_MDC
CH1_MDC
R4081
0/J3
R4082
0/J3
R4083
0/J3
CP4011
IC4014
TC7W125FUTL
IC4014
TC7W125FUTL
C4054
0.1/UFV
[P4001-B6]
SDTO1
*PAT=PATTERN ONLY
A
B
C
D
E
F
1
2
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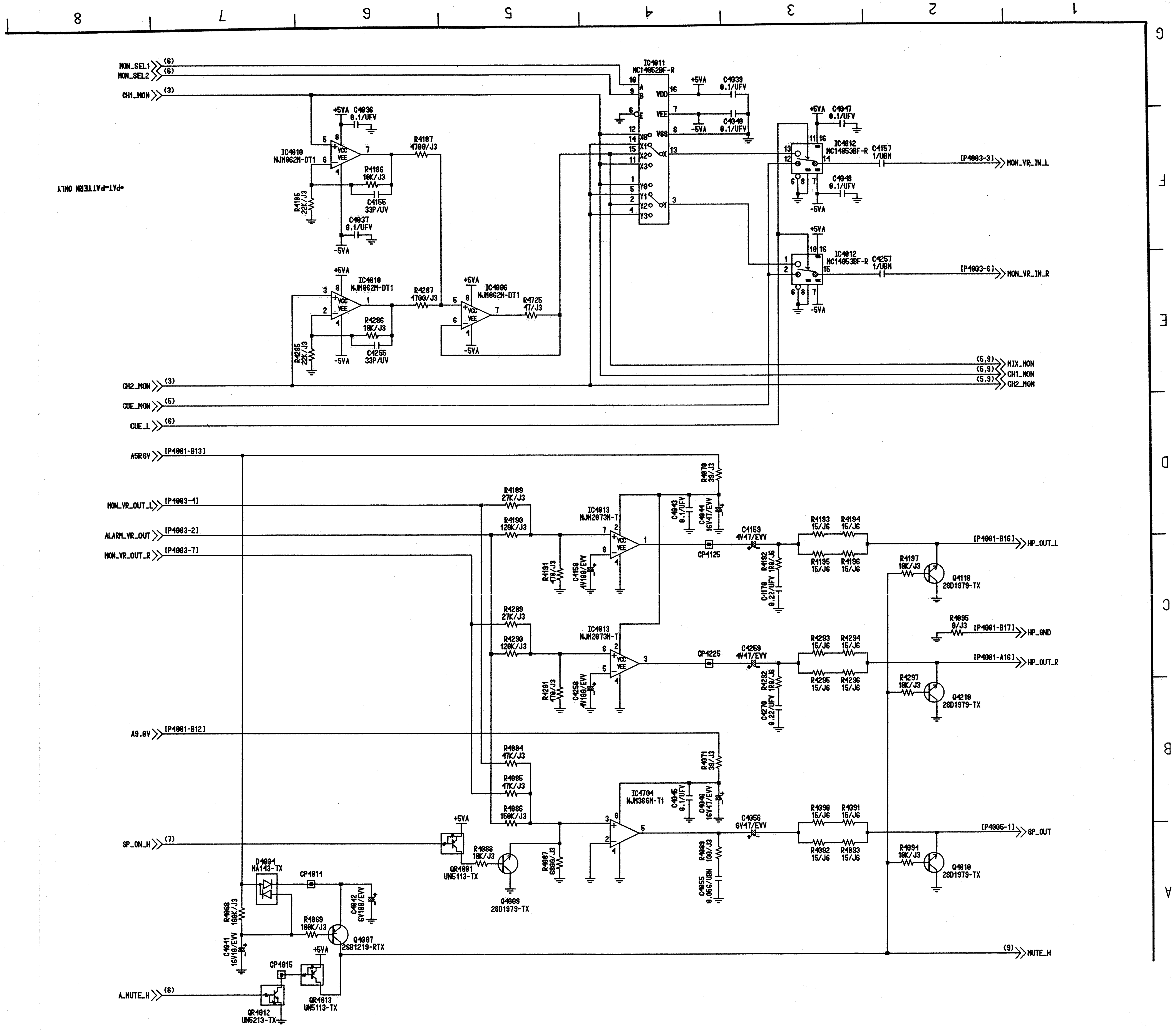
10

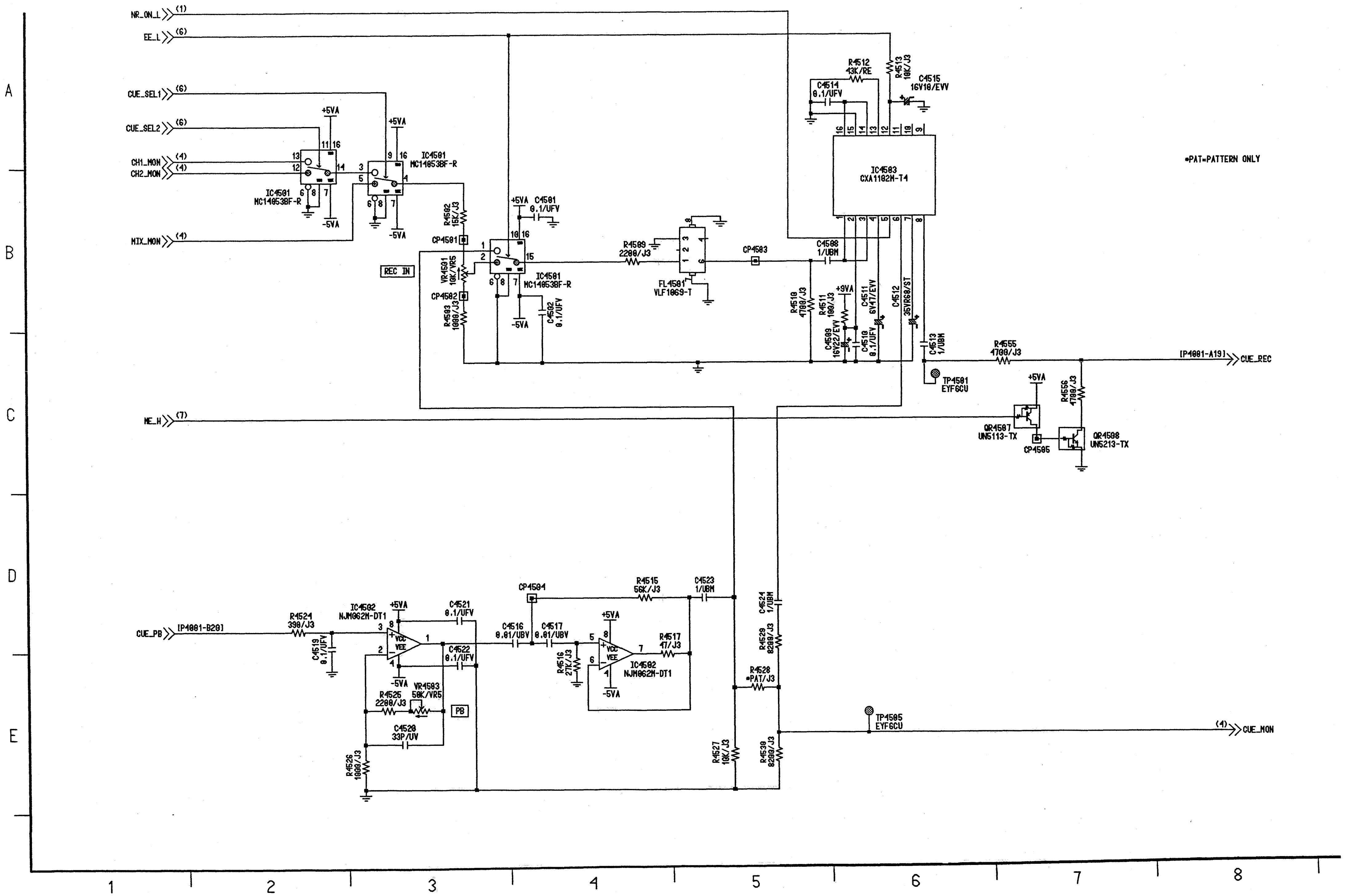
REVERSE SIDE

AUDIO LCD 2/9

AUDIO LCD (4/9) AUDIO MONITOR SCHEMATIC DIAGRAM


A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
MON_SEL1 (6)
MON_SEL2 (6)
CH1_MON (3)
IC4811
MC14052BF-R
+5VA
C4839
0.1/UFV
C4840
0.1/UFV
-5VA
VDD
VEE
VSS
X0
X1
X2
X3
Y0
Y1
Y2
Y3
X
Y
A
B
E
IC4812
MC14053BF-R
+5VA
C4847
0.1/UFV
C4848
0.1/UFV
-5VA
C4157
1/UBN
[P4003-3]
MON_VR_IN_L
C4257
1/UBN
[P4003-6]
MON_VR_IN_R
*PAT=PATTERN ONLY
IC4810
NJM062M-DT1
C4836
0.1/UFV
R4187
4700/J3
R4186
10K/J3
C4155
33P/UV
R4185
22K/J3
C4837
0.1/UFV
R4287
4700/J3
R4286
10K/J3
C4255
33P/UV
R4285
22K/J3
IC4806
NJM062M-DT1
R4725
47/J3
(5,9) MIX_MON
(5,9) CH1_MON
(5,9) CH2_MON
CH2_MON (3)
CUE_MON (5)
CUE_L (6)
A5R6V [P4001-B13]
MON_VR_OUT_L [P4003-4]
ALARM_VR_OUT [P4003-2]
MON_VR_OUT_R [P4003-7]
A9.0V [P4001-B12]
SP_ON_H (7)
A_MUTE_H (6)
R4189
27K/J3
R4190
120K/J3
IC4813
NJM2073M-T1
R4191
470/J3
C4158
4V100/EVV
C4043
0.1/UFV
C4044
16V47/EVV
R4070
39/J3
C4159
4V47/EVV
CP4125
R4192
100/J6
C4170
0.22/UFV
R4193
15/J6
R4194
15/J6
R4195
15/J6
R4196
15/J6
[P4001-B16]
HP_OUT_L
R4197
10K/J3
Q4110
2SD1979-TX
R4095
0/J3
[P4001-B17]
HP_GND
R4289
27K/J3
R4290
120K/J3
R4231
470/J3
C4258
4V100/EVV
CP4225
C4259
4V47/EVV
R4232
100/J6
C4270
0.22/UFV
R4293
15/J6
R4294
15/J6
R4295
15/J6
R4296
15/J6
[P4001-A16]
HP_OUT_R
R4297
10K/J3
Q4210
2SD1979-TX
R4084
47K/J3
R4085
47K/J3
R4086
150K/J3
IC4704
NJM386M-T1
C4045
0.1/UFV
C4046
16V47/EVV
R4071
39/J3
C4056
6V47/EVV
R4090
15/J6
R4091
15/J6
R4092
15/J6
R4093
15/J6
[P4005-1]
SP_OUT
R4094
10K/J3
Q4010
2SD1979-TX
R4089
100/J3
C4055
0.056/UBN
R4087
5600/J3
Q4089
2SD1979-TX
R4088
10K/J3
QR4081
UN5113-TX
+5VA
D4084
MA143-TX
CP4014
C4042
6V100/EVV
R4068
100K/J3
R4069
100K/J3
C4041
16V10/EVV
Q4087
2SB1219-RTX
CP4015
QR4013
UN5113-TX
QR4012
UN5213-TX
(9) MUTE_H
VCC
VEE

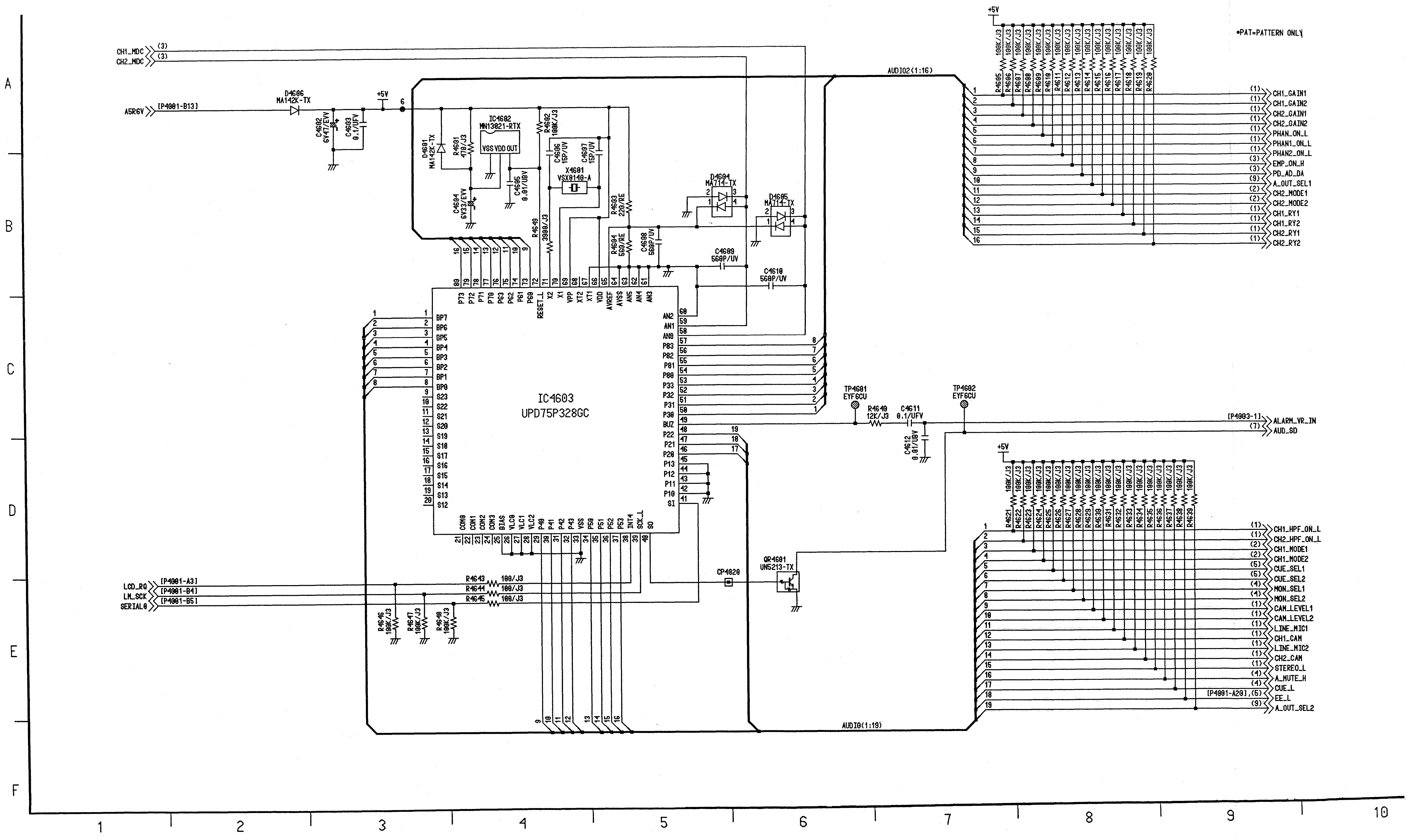
AUDIO LCD (5/9) AUDIO CUE SCHEMATIC DIAGRAM


A
B
C
D
E
1
2
3
4
5
6
7
8
NR_ON_L (1)
EE_L (6)
CUE_SEL1 (6)
CUE_SEL2 (6)
CH1_MON (4)
CH2_MON (4)
MIX_MON (4)
ME_H (7)
+5VA
-5VA
IC4501 MC14053BF-R
IC4501 MC14053BF-R
IC4501 MC14053BF-R
R4502 15K/J3
CP4501
CP4502
VR4501 10K/VR5
R4503 1000/J3
REC IN
C4501 0.1/UFV
C4502 0.1/UFV
R4509 2200/J3
FL4501 VLF1069-T
CP4503
C4508 1/UBM
IC4503 CXA1102M-T4
R4512 43K/RE
R4513 10K/J3
C4514 0.1/UFV
C4515 16V10/EVV
R4510 4700/J3
R4511 100/J3
+9VA
C4509 16V22/EVV
C4510 0.1/UFV
C4511 6V47/EVV
C4512 35VR68/ST
C4513 1/UBM
TP4501 EYF6CU
R4555 4700/J3
[P4001-A19] CUE_REC
R4556 4700/J3
QR4507 UN5113-TX
CP4505
QR4508 UN5213-TX
*PAT=PATTERN ONLY
CUE_PB [P4001-B20]
R4524 390/J3
C4519 0.1/UFV
IC4502 NJM062M-DT1
C4521 0.1/UFV
C4522 0.1/UFV
VCC
VEE
R4525 2200/J3
VR4503 50K/VR5
PB
C4520 33P/UV
R4526 1000/J3
CP4504
C4516 0.01/UBV
C4517 0.01/UBV
R4516 27K/J3
IC4502 NJM062M-DT1
R4515 56K/J3
R4517 47/J3
C4523 1/UBM
C4524 1/UBM
R4529 8200/J3
R4528 *PAT/J3
R4527 10K/J3
R4530 8200/J3
TP4505 EYF6CU
(4) CUE_MON

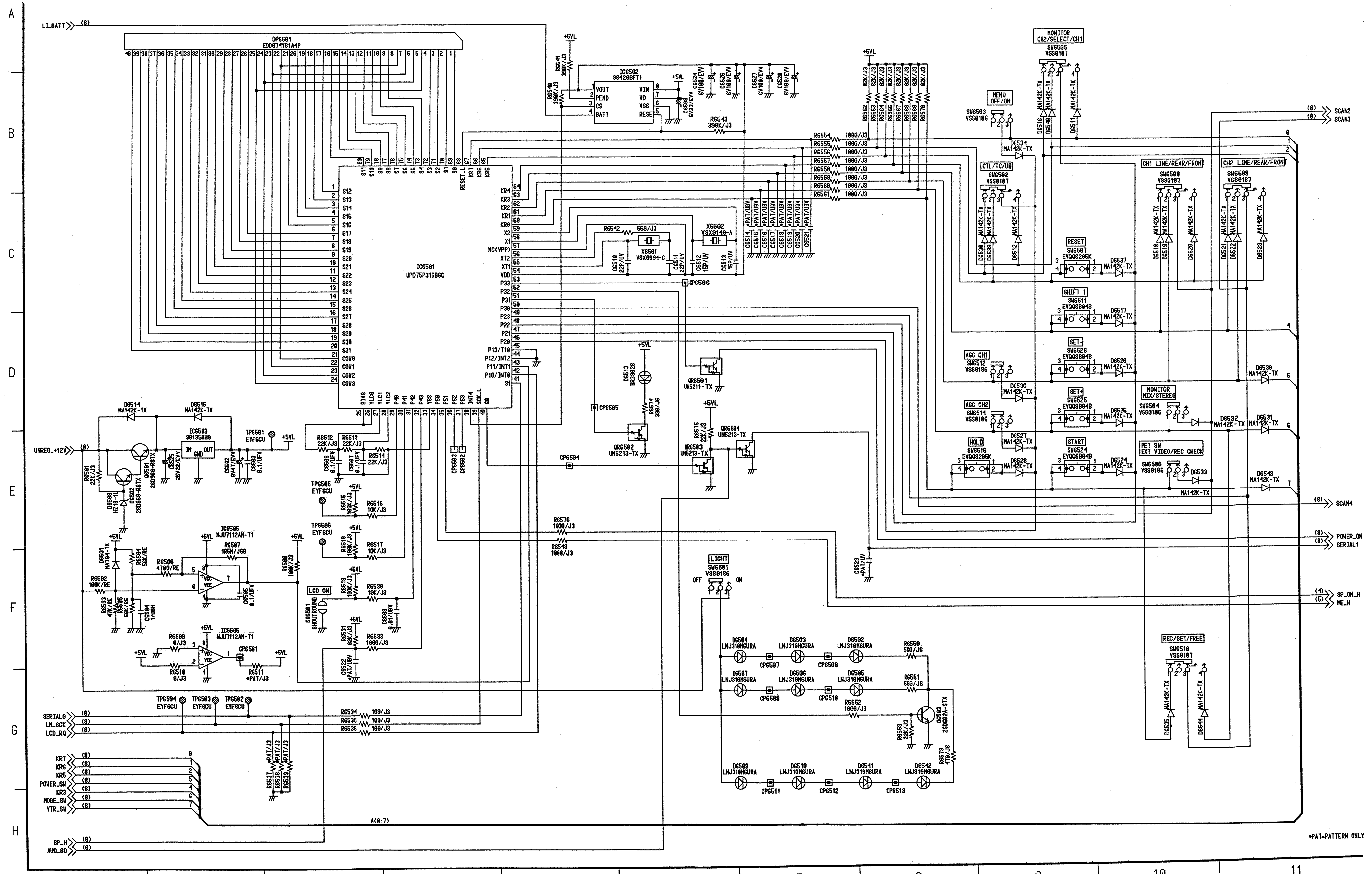
REVERSE SIDE

AUDIO LCD 4/9

AUDIO LCD (6/9) AUDIO CONTROL SCHEMATIC DIAGRAM


*PAT=PATTERN ONLY
CH1_MDC (3)
CH2_MDC (3)
A5R6V [P4001-B13]
D4606 MA142K-TX
C4602 6V47/EVV
C4603 0.1/UFV
+5V
6
D4601 MA142K-TX
R4601 470/J3
IC4602 MN13821-RTX
VSS VDD OUT
C4605 0.01/UBV
C4604 6V33/EVV
R4602 100K/J3
C4606 15P/UV
C4607 15P/UV
X4601 VSX0140-A
R4649 3900/J3
R4603 220/RE
R4604 560/RE
C4608 560P/UV
D4604 MA714-TX
D4605 MA714-TX
C4609 560P/UV
C4610 560P/UV
IC4603
UPD75P328GC
P73 P72 P71 P70 P63 P62 P61 P60 RESET_L X2 X1 VPP XT2 XT1 VDD AVREF AVSS AN5 AN4 AN3
AN2 AN1 AN0 P83 P82 P81 P80 P33 P32 P31 P30 BUZ P22 P21 P20 P13 P12 P11 P10 SI
BP7 BP6 BP5 BP4 BP3 BP2 BP1 BP0 S23 S22 S21 S20 S19 S18 S17 S16 S15 S14 S13 S12
COM0 COM1 COM2 COM3 BIAS VLC0 VLC1 VLC2 P40 P41 P42 P43 VSS P50 P51 P52 P53 INT4 SCK_L SO
AUDIO2(1:16)
+5V
R4605 R4606 R4607 R4608 R4609 R4610 R4611 R4612 R4613 R4614 R4615 R4616 R4617 R4618 R4619 R4620 100K/J3
(1) CH1_GAIN1
(1) CH1_GAIN2
(1) CH2_GAIN1
(1) CH2_GAIN2
(1) PHAN_ON_L
(1) PHAN1_ON_L
(1) PHAN2_ON_L
(3) EMP_ON_H
(3) PD_AD_DA
(9) A_OUT_SEL1
(2) CH2_MODE1
(2) CH2_MODE2
(1) CH1_RY1
(1) CH1_RY2
(1) CH2_RY1
(1) CH2_RY2
TP4601 EYF6CU
R4640 12K/J3
C4611 0.1/UFV
C4612 0.01/UBV
TP4602 EYF6CU
[P4003-1] ALARM_VR_IN
(7) AUD_SD
+5V
R4621 R4622 R4623 R4624 R4625 R4626 R4627 R4628 R4629 R4630 R4631 R4632 R4633 R4634 R4635 R4636 R4637 R4638 R4639 100K/J3
(1) CH1_HPF_ON_L
(1) CH2_HPF_ON_L
(2) CH1_MODE1
(2) CH1_MODE2
(5) CUE_SEL1
(5) CUE_SEL2
(4) MON_SEL1
(4) MON_SEL2
(1) CAM_LEVEL1
(1) CAM_LEVEL2
(1) LINE_MIC1
(1) CH1_CAM
(1) LINE_MIC2
(1) CH2_CAM
(1) STEREO_L
(4) A_MUTE_H
(4) CUE_L
[P4001-A20],(5) EE_L
(9) A_OUT_SEL2
LCD_RQ [P4001-A3]
LM_SCK [P4001-B4]
SERIAL0 [P4001-B5]
R4643 100/J3
R4644 100/J3
R4645 100/J3
R4646 100K/J3
R4647 100K/J3
R4648 100K/J3
CP4020
QR4601 UN5213-TX
AUDIO(1:19)
A
B
C
D
E
F
1 2 3 4 5 6 7 8 9 10

AUDIO LCD (7/9) AUDIO LCD SCHEMATIC DIAGRAM

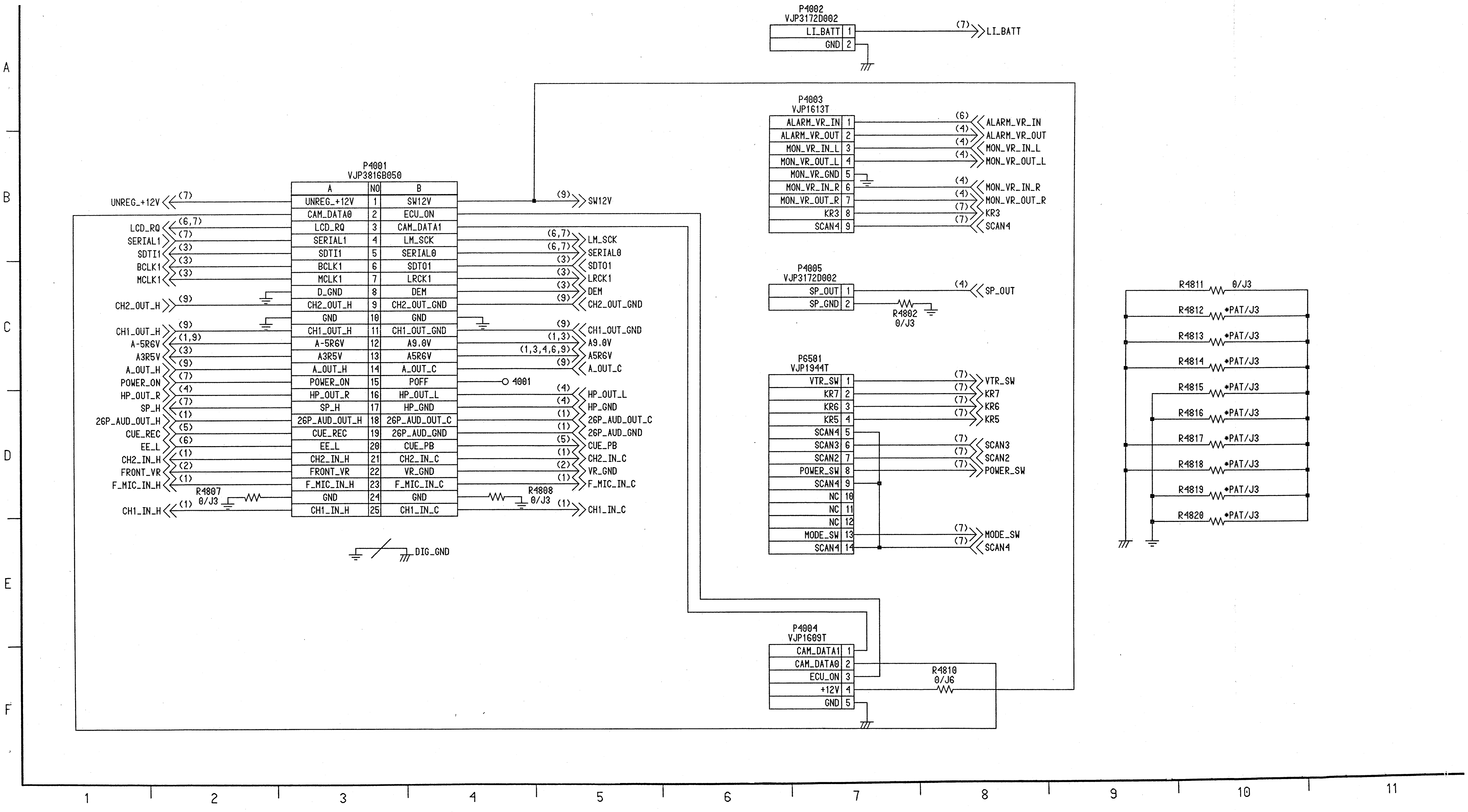


A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11
LI_BATT
DP6501
EDD874YC1A4P
IC6501
UPD75P316BGC
IC6502
S8420BFT1
VOUT
PEND
CS
BATT
VIN
VD
VSS
RESET
+5VL
R6541
390K/J3
R6540
390K/J3
R6543
390K/J3
C6524
C6526
C6527
C6528
C6598
R6542
560/J3
X6501
VSX0094-C
X6502
VSX0140-A
C6510
C6511
C6512
C6513
CP6506
RESET_L
KR4
KR3
KR2
KR1
KR0
X2
X1
NC(VPP)
XT2
XT1
VDD
P33
P32
P31
P30
P23
P22
P21
P20
P13/TI0
P12/INT2
P11/INT1
P10/INT0
S1
BIAS
VLC0
VLC1
VLC2
P40
P41
P42
P43
VSS
P50
P51
P52
P53
INT4
SCK_L
S0
COM0
COM1
COM2
COM3
R6554
R6555
R6556
R6557
R6558
R6559
R6560
R6561
1000/J3
R6562
R6563
R6564
R6565
R6567
R6568
R6569
R6570
82K/J3
*PAT/UBV
C6514
C6515
C6516
C6517
C6518
C6519
C6520
C6521
MONITOR
CH2/SELECT/CH1
SW6505
VSS0187
MENU
OFF/ON
SW6503
VSS0186
CTL/TC/UB
SW6502
VSS0187
D6534
MA142K-TX
D6516
D6540
D6511
D6538
D6539
D6512
RESET
SW6507
EVQQS205K
D6537
SHIFT 1
SW6511
EVQQSB04B
D6517
SET-
SW6526
D6526
SET+
SW6525
D6525
START
SW6524
D6524
AGC CH1
SW6512
VSS0186
D6536
AGC CH2
SW6514
VSS0186
D6527
HOLD
SW6516
EVQQS205K
D6528
CH1 LINE/REAR/FRONT
SW6508
VSS0187
D6518
D6519
D6520
CH2 LINE/REAR/FRONT
SW6509
VSS0187
D6521
D6522
D6523
MONITOR
MIX/STEREO
SW6504
VSS0186
D6532
D6530
D6531
PET SW
EXT VIDEO/REC CHECK
SW6506
VSS0186
D6533
D6543
SCAN2
SCAN3
SCAN4
POWER_ON
SERIAL1
SP_ON_H
ME_H
QR6501
UN5211-TX
QR6502
UN5213-TX
QR6503
UN5213-TX
QR6504
UN5213-TX
R6575
22K/J3
D6513
BR1302S
R6574
330/J6
CP6505
CP6504
R6576
1000/J3
R6548
1000/J3
C6523
*PAT/UV
LIGHT
SW6501
VSS0186
OFF
ON
D6504
D6503
D6502
D6507
D6506
D6505
D6509
D6510
D6541
D6542
LNJ310M6URA
CP6507
CP6508
CP6509
CP6510
CP6511
CP6512
CP6513
R6550
560/J6
R6551
560/J6
R6552
1000/J3
R6553
22K/J3
Q6503
2SD602A-STX
R6573
470/J6
REC/SET/FREE
SW6510
VSS0187
D6535
D6544
D6514
MA142K-TX
D6515
MA142K-TX
IC6503
S81350HG
IN
GND
OUT
TP6501
EYF6CU
UNREG_+12V
R6501
22K/J3
Q6501
2SD968-RSTX
Q6502
2SD968-RSTX
D6500
HZ7C-1L
C6525
25V22/EVY
C6502
6V47/EVY
C6503
0.1/UV
R6512
22K/J3
R6513
22K/J3
R6514
22K/J3
C6506
0.1/UFV
C6507
0.1/UFV
TP6505
EYF6CU
R6515
100K/J3
R6516
10K/J3
TP6506
EYF6CU
R6518
100K/J3
R6517
10K/J3
CP6503
CP6502
IC6505
NJU7112AM-T1
D6501
MA704-TX
R6504
56K/RE
R6506
4700/RE
R6507
1MEG/J66
R6502
100K/RE
R6503
47K/RE
R6505
56K/RE
C6504
1/UBN
C6505
0.1/UFV
R6508
100K/J3
LCD ON
SR6501
SHOUTROUND
R6519
100K/J3
R6530
10K/J3
C6508
0.01/UBV
R6531
82K/J3
R6533
1000/J3
C6522
*PAT/UBV
IC6506
NJU7112AM-T1
R6509
0/J3
R6510
0/J3
CP6501
R6511
*PAT/J3
TP6504
TP6503
TP6502
EYF6CU
SERIAL0
LN_SCK
LCD_RQ
R6534
R6535
R6536
100/J3
KR7
KR6
KR5
POWER_SW
KR3
MODE_SW
VTR_SW
R6537
R6538
R6539
*PAT/J3
A(0:7)
SP_H
AUD_SD
*PAT=PATTERN ONLY

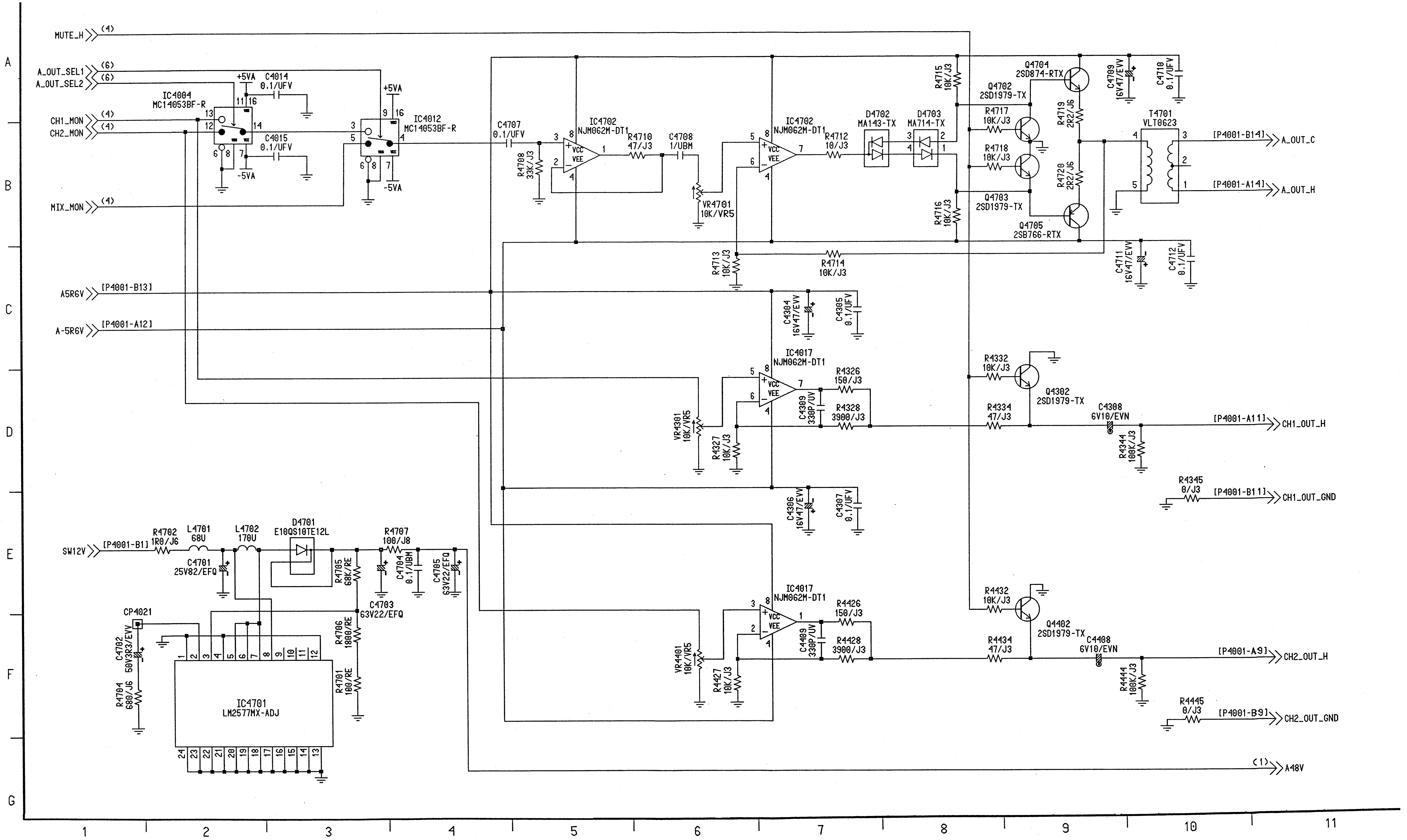
REVERSE SIDE

AUDIO LCD 6/9

AUDIO LCD (8/9) AUDIO LCD I/F SCHEMATIC DIAGRAM

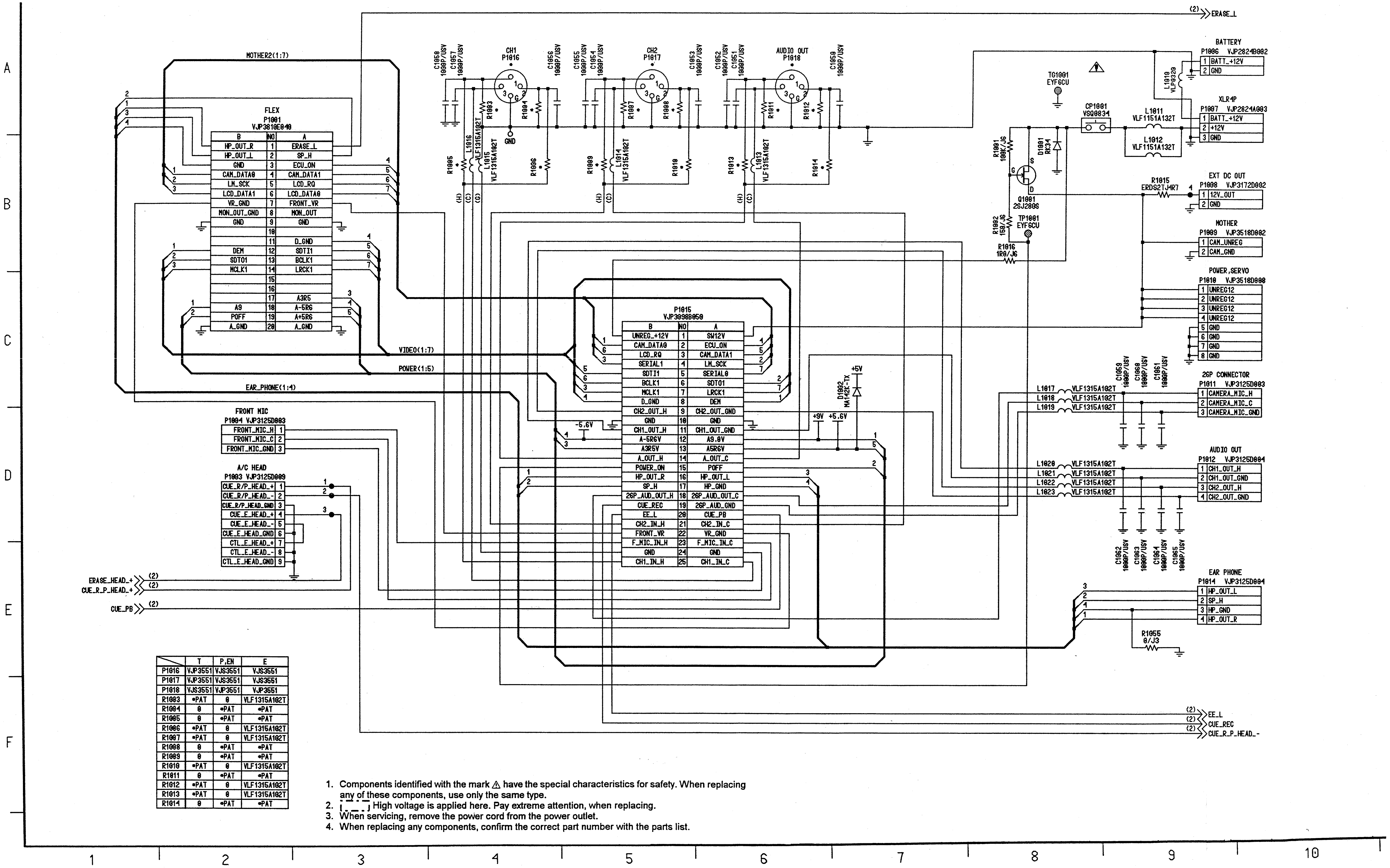

A
B
C
D
E
F
1
2
3
4
5
6
7
8
9
10
11
P4001
VJP3816B050
A
NO
B
UNREG_+12V 1 SW12V
CAM_DATA0 2 ECU_ON
LCD_RQ 3 CAM_DATA1
SERIAL1 4 LM_SCK
SDTI1 5 SERIAL0
BCLK1 6 SDTO1
MCLK1 7 LRCK1
D_GND 8 DEM
CH2_OUT_H 9 CH2_OUT_GND
GND 10 GND
CH1_OUT_H 11 CH1_OUT_GND
A-5R6V 12 A9.0V
A3R5V 13 A5R6V
A_OUT_H 14 A_OUT_C
POWER_ON 15 POFF
HP_OUT_R 16 HP_OUT_L
SP_H 17 HP_GND
26P_AUD_OUT_H 18 26P_AUD_OUT_C
CUE_REC 19 26P_AUD_GND
EE_L 20 CUE_PB
CH2_IN_H 21 CH2_IN_C
FRONT_VR 22 VR_GND
F_MIC_IN_H 23 F_MIC_IN_C
GND 24 GND
CH1_IN_H 25 CH1_IN_C
(7) UNREG_+12V
(6,7) LCD_RQ
(7) SERIAL1
(3) SDTI1
(3) BCLK1
(3) MCLK1
(9) CH2_OUT_H
(9) CH1_OUT_H
(1,9) A-5R6V
(3) A3R5V
(9) A_OUT_H
(7) POWER_ON
(4) HP_OUT_R
(7) SP_H
(1) 26P_AUD_OUT_H
(5) CUE_REC
(6) EE_L
(1) CH2_IN_H
(2) FRONT_VR
(1) F_MIC_IN_H
(1) CH1_IN_H
R4807
0/J3
R4808
0/J3
(9) SW12V
(6,7) LM_SCK
(6,7) SERIAL0
(3) SDTO1
(3) LRCK1
(3) DEM
(9) CH2_OUT_GND
(9) CH1_OUT_GND
(1,3) A9.0V
(1,3,4,6,9) A5R6V
(9) A_OUT_C
4001
(4) HP_OUT_L
(4) HP_GND
(1) 26P_AUD_OUT_C
(1) 26P_AUD_GND
(5) CUE_PB
(1) CH2_IN_C
(2) VR_GND
(1) F_MIC_IN_C
(1) CH1_IN_C
DIG_GND
P4002
VJP3172D002
LI_BATT 1
GND 2
(7) LI_BATT
P4003
VJP1613T
ALARM_VR_IN 1
ALARM_VR_OUT 2
MON_VR_IN_L 3
MON_VR_OUT_L 4
MON_VR_GND 5
MON_VR_IN_R 6
MON_VR_OUT_R 7
KR3 8
SCAN4 9
(6) ALARM_VR_IN
(4) ALARM_VR_OUT
(4) MON_VR_IN_L
(4) MON_VR_OUT_L
(4) MON_VR_IN_R
(4) MON_VR_OUT_R
(7) KR3
(7) SCAN4
P4005
VJP3172D002
SP_OUT 1
SP_GND 2
R4802
0/J3
(4) SP_OUT
P6501
VJP1944T
VTR_SW 1
KR7 2
KR6 3
KR5 4
SCAN4 5
SCAN3 6
SCAN2 7
POWER_SW 8
SCAN4 9
NC 10
NC 11
NC 12
MODE_SW 13
SCAN4 14
(7) VTR_SW
(7) KR7
(7) KR6
(7) KR5
(7) SCAN3
(7) SCAN2
(7) POWER_SW
(7) MODE_SW
(7) SCAN4
P4004
VJP1609T
CAM_DATA1 1
CAM_DATA0 2
ECU_ON 3
+12V 4
GND 5
R4810
0/J6
R4811 0/J3
R4812 *PAT/J3
R4813 *PAT/J3
R4814 *PAT/J3
R4815 *PAT/J3
R4816 *PAT/J3
R4817 *PAT/J3
R4818 *PAT/J3
R4819 *PAT/J3
R4820 *PAT/J3

AUDIO LCD (9/9) AUDIO OUT SCHEMATIC DIAGRAM


MUTE_H (4)
A_OUT_SEL1 (6)
A_OUT_SEL2 (6)
CH1_MON (4)
CH2_MON (4)
MIX_MON (4)
A5RGV [P4001-B13]
A-5RGV [P4001-A12]
SW12V [P4001-B1]
IC4004 MC14053BF-R
+5VA
C4014 0.1/UFV
C4015 0.1/UFV
-5VA
IC4012 MC14053BF-R
C4707 0.1/UFV
R4708 33K/J3
IC4702 NJM062M-DT1
R4710 47/J3
C4708 1/UBM
VR4701 10K/VR5
R4712 10/J3
D4702 MA143-TX
D4703 MA714-TX
R4715 10K/J3
R4716 10K/J3
R4713 10K/J3
R4714 10K/J3
Q4702 2SD1979-TX
Q4703 2SD1979-TX
Q4704 2SD874-RTX
Q4705 2SB766-RTX
R4717 10K/J3
R4718 10K/J3
R4719 2R2/J6
R4720 2R2/J6
C4709 16V47/EVV
C4710 0.1/UFV
C4711 16V47/EVV
C4712 0.1/UFV
T4701 VLT0623
[P4001-B14] A_OUT_C
[P4001-A14] A_OUT_H
C4304 16V47/EVV
C4305 0.1/UFV
IC4017 NJM062M-DT1
R4326 150/J3
R4328 3900/J3
C4309 330P/UV
VR4301 10K/VR5
R4327 10K/J3
R4332 10K/J3
Q4302 2SD1979-TX
R4334 47/J3
C4308 6V10/EVN
R4344 100K/J3
[P4001-A11] CH1_OUT_H
R4345 0/J3
[P4001-B11] CH1_OUT_GND
C4306 16V47/EVV
C4307 0.1/UFV
IC4017 NJM062M-DT1
R4426 150/J3
R4428 3900/J3
C4409 330P/UV
VR4401 10K/VR5
R4427 10K/J3
R4432 10K/J3
Q4402 2SD1979-TX
R4434 47/J3
C4408 6V10/EVN
R4444 100K/J3
[P4001-A9] CH2_OUT_H
R4445 0/J3
[P4001-B9] CH2_OUT_GND
R4702 1R0/J6
L4701 68U
C4701 25V82/EFQ
L4702 170U
D4701 E10QS10TE12L
R4707 100/J8
C4704 0.1/UBM
C4705 63V22/EFQ
R4705 68K/RE
C4703 63V22/EFQ
R4706 1800/RE
R4701 100/RE
CP4021
C4702 50V3R3/EVV
R4704 680/J6
IC4701 LM2577MX-ADJ
(1) A48V
A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9
10
11

REVERSE SIDE
AUDIO LCD 8/9

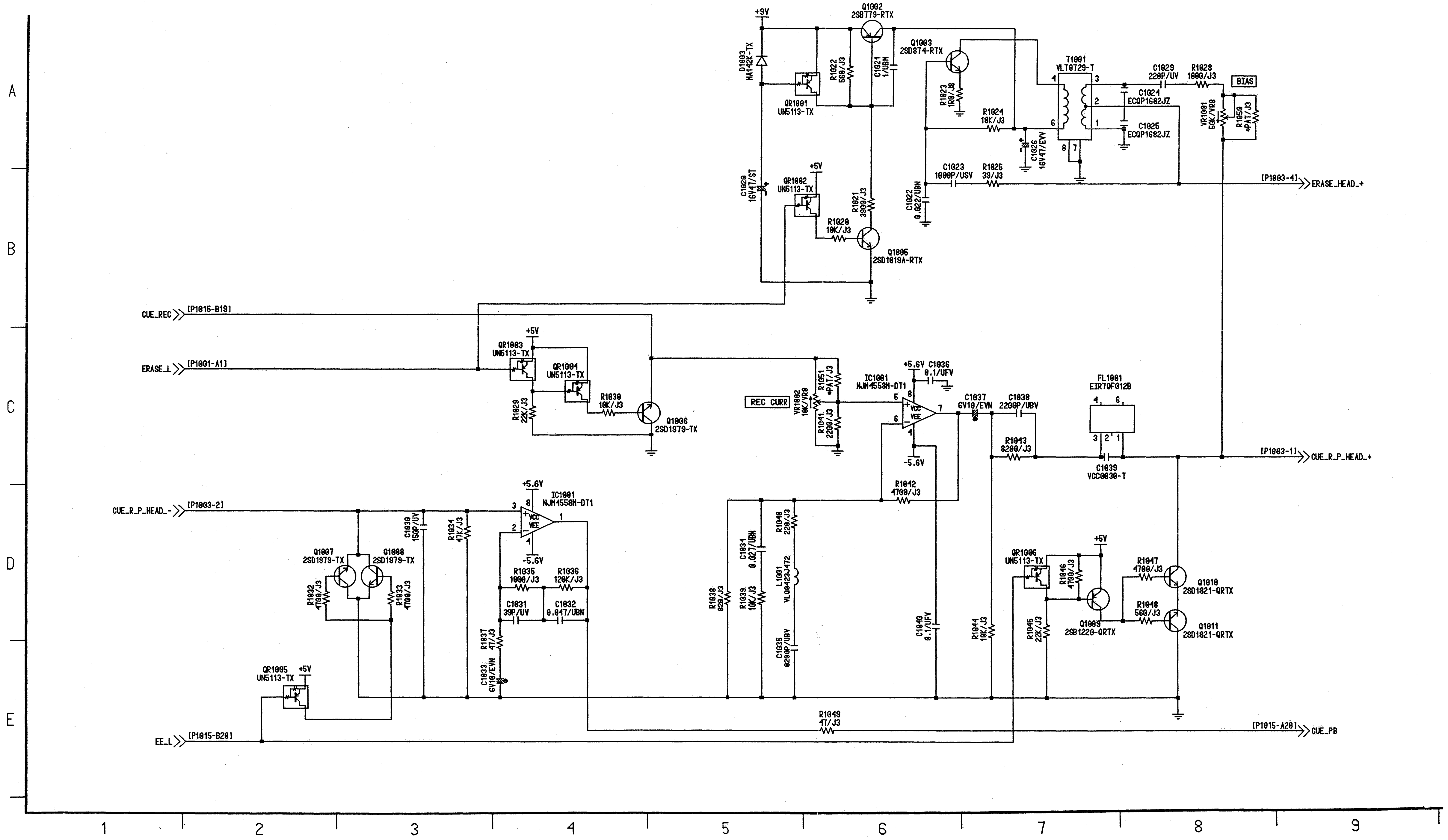
REAR JACK (1/3) SCHEMATIC DIAGRAM


A
B
C
D
E
F
1
2
3
4
5
6
7
8
9
10
MOTHER2(1:7)
FLEX
P1001
VJP3810E040
B
NO
A
HP_OUT_R 1 ERASE_L
HP_OUT_L 2 SP_H
GND 3 ECU_ON
CAM_DATA0 4 CAM_DATA1
LM_SCK 5 LCD_RQ
LCD_DATA1 6 LCD_DATA0
VR_GND 7 FRONT_VR
MON_OUT_GND 8 MON_OUT
GND 9 GND
10
11 D_GND
DEM 12 SDTI1
SDTO1 13 BCLK1
MCLK1 14 LRCK1
15
16
17 A3R5
A9 18 A-5R6
POFF 19 A+5R6
A_GND 20 A_GND
VIDEO(1:7)
POWER(1:5)
EAR_PHONE(1:4)
C1058 1000P/USV
C1057 1000P/USV
CH1
P1016
C1056 1000P/USV
C1055 1000P/USV
C1054 1000P/USV
CH2
P1017
C1053 1000P/USV
C1052 1000P/USV
C1051 1000P/USV
AUDIO OUT
P1018
C1050 1000P/USV
R1003
R1004
R1005
R1006
L1016
VLF1315A102T
L1015
VLF1315A102T
GND
R1007
R1008
R1009
R1010
L1014
VLF1315A102T
R1011
R1012
R1013
R1014
L1013
VLF1315A102T
(H)
(C)
(G)
(2) ERASE_L
TG1001
EYF6CU
CP1001
VSQ0834
R1001
100K/J6
D1001
RK34
Q1001
2SJ280S
S
G
D
R1002
150/J6
TP1001
EYF6CU
R1016
1R0/J6
L1011
VLF1151A132T
L1012
VLF1151A132T
L1010
VLP0320
BATTERY
P1006 VJP2824B002
1 BATT_+12V
2 GND
XLR4P
P1007 VJP2824A003
1 BATT_+12V
2 +12V
3 GND
R1015
ERDS2TJ4R7
EXT DC OUT
P1008 VJP3172D002
1 12V_OUT
2 GND
MOTHER
P1009 VJP3518D002
1 CAM_UNREG
2 CAM_GND
POWER,SERVO
P1010 VJP3518D008
1 UNREG12
2 UNREG12
3 UNREG12
4 UNREG12
5 GND
6 GND
7 GND
8 GND
C1059 1000P/USV
C1060 1000P/USV
C1061 1000P/USV
L1017 VLF1315A102T
L1018 VLF1315A102T
L1019 VLF1315A102T
26P CONNECTOR
P1011 VJP3125D003
1 CAMERA_MIC_H
2 CAMERA_MIC_C
3 CAMERA_MIC_GND
L1020 VLF1315A102T
L1021 VLF1315A102T
L1022 VLF1315A102T
L1023 VLF1315A102T
AUDIO OUT
P1012 VJP3125D004
1 CH1_OUT_H
2 CH1_OUT_GND
3 CH2_OUT_H
4 CH2_OUT_GND
C1062 1000P/USV
C1063 1000P/USV
C1064 1000P/USV
C1065 1000P/USV
EAR PHONE
P1014 VJP3125D004
1 HP_OUT_L
2 SP_H
3 HP_GND
4 HP_OUT_R
R1055
0/J3
P1015
VJP3098B050
B
NO
A
UNREG_+12V 1 SW12V
CAM_DATA0 2 ECU_ON
LCD_RQ 3 CAM_DATA1
SERIAL1 4 LM_SCK
SDTI1 5 SERIAL0
BCLK1 6 SDTO1
MCLK1 7 LRCK1
D_GND 8 DEM
CH2_OUT_H 9 CH2_OUT_GND
GND 10 GND
CH1_OUT_H 11 CH1_OUT_GND
A-5R6V 12 A9.0V
A3R5V 13 A5R6V
A_OUT_H 14 A_OUT_C
POWER_ON 15 POFF
HP_OUT_R 16 HP_OUT_L
SP_H 17 HP_GND
26P_AUD_OUT_H 18 26P_AUD_OUT_C
CUE_REC 19 26P_AUD_GND
EE_L 20 CUE_PB
CH2_IN_H 21 CH2_IN_C
FRONT_VR 22 VR_GND
F_MIC_IN_H 23 F_MIC_IN_C
GND 24 GND
CH1_IN_H 25 CH1_IN_C
-5.6V
+9V
+5.6V
+5V
D1002
MA142K-TX
FRONT MIC
P1004 VJP3125D003
FRONT_MIC_H 1
FRONT_MIC_C 2
FRONT_MIC_GND 3
A/C HEAD
P1003 VJP3125D009
CUE_R/P_HEAD_+ 1
CUE_R/P_HEAD_- 2
CUE_R/P_HEAD_GND 3
CUE_E_HEAD_+ 4
CUE_E_HEAD_- 5
CUE_E_HEAD_GND 6
CTL_E_HEAD_+ 7
CTL_E_HEAD_- 8
CTL_E_HEAD_GND 9
ERASE_HEAD_+ (2)
CUE_R_P_HEAD_+ (2)
CUE_PB (2)
(2) EE_L
(2) CUE_REC
(2) CUE_R_P_HEAD_-

	T	P,EN	E
P1016	VJP3551	VJS3551	VJS3551
P1017	VJP3551	VJS3551	VJS3551
P1018	VJS3551	VJP3551	VJP3551
R1003	•PAT	0	VLF1315A102T
R1004	0	•PAT	•PAT
R1005	0	•PAT	•PAT
R1006	•PAT	0	VLF1315A102T
R1007	•PAT	0	VLF1315A102T
R1008	0	•PAT	•PAT
R1009	0	•PAT	•PAT
R1010	•PAT	0	VLF1315A102T
R1011	0	•PAT	•PAT
R1012	•PAT	0	VLF1315A102T
R1013	•PAT	0	VLF1315A102T
R1014	0	•PAT	•PAT

1. Components identified with the mark ⚠ have the special characteristics for safety. When replacing any of these components, use only the same type.
2. [- - -] High voltage is applied here. Pay extreme attention, when replacing.
3. When servicing, remove the power cord from the power outlet.
4. When replacing any components, confirm the correct part number with the parts list.

REAR JACK (2/3) SCHEMATIC DIAGRAM



A
B
C
D
E
1
2
3
4
5
6
7
8
9
+9V
Q1002
2SB779-RTX
D1003
MA142K-TX
R1022
560/J3
C1021
1/UBN
QR1001
UN5113-TX
Q1003
2SD874-RTX
R1023
1R0/J8
R1024
18K/J3
C1026
16V47/EVV
T1001
VLT0729-T
4
3
2
6
1
8
7
C1029
220P/UV
R1028
1000/J3
BIAS
C1024
ECQP1682JZ
C1025
ECQP1682JZ
VR1001
50K/VR8
R1050
*PAT/J3
C1020
16V47/ST
+5V
QR1002
UN5113-TX
R1021
3900/J3
R1020
10K/J3
Q1005
2SD1819A-RTX
C1022
0.022/UBN
C1023
1000P/USV
R1025
39/J3
[P1003-4]
ERASE_HEAD_+
CUE_REC
[P1015-B19]
ERASE_L
[P1001-A1]
+5V
QR1003
UN5113-TX
QR1004
UN5113-TX
R1029
22K/J3
R1030
10K/J3
Q1006
2SD1979-TX
REC CURR
VR1002
10K/VR8
R1051
*PAT/J3
R1041
2200/J3
IC1001
NJM4558M-DT1
+5.6V C1036
0.1/UFV
5
8
6
4
7
VCC
VEE
-5.6V
C1037
6V10/EVN
C1038
2200P/UBV
FL1001
EIR7QF012B
4
6
3
2
1
R1043
8200/J3
C1039
VCC0030-T
[P1003-1]
CUE_R_P_HEAD_+
R1042
4700/J3
CUE_R_P_HEAD_-
[P1003-2]
Q1007
2SD1979-TX
Q1008
2SD1979-TX
R1032
4700/J3
R1033
4700/J3
C1030
150P/UV
R1034
47K/J3
+5.6V
IC1001
NJM4558M-DT1
3
8
2
4
1
VCC
VEE
-5.6V
R1035
1000/J3
R1036
120K/J3
C1031
39P/UV
C1032
0.047/UBN
R1037
47/J3
C1033
6V10/EVN
R1038
820/J3
C1034
0.027/UBN
R1039
10K/J3
R1040
220/J3
L1001
VL08423J472
C1035
8200P/UBV
C1040
0.1/UFV
R1044
10K/J3
QR1006
UN5113-TX
+5V
R1046
4700/J3
R1045
22K/J3
Q1009
2SB1220-QRTX
R1047
4700/J3
Q1010
2SD1821-QRTX
R1048
560/J3
Q1011
2SD1821-QRTX
QR1005
UN5113-TX
+5V
EE_L
[P1015-B20]
R1049
47/J3
[P1015-A20]
CUE_PB

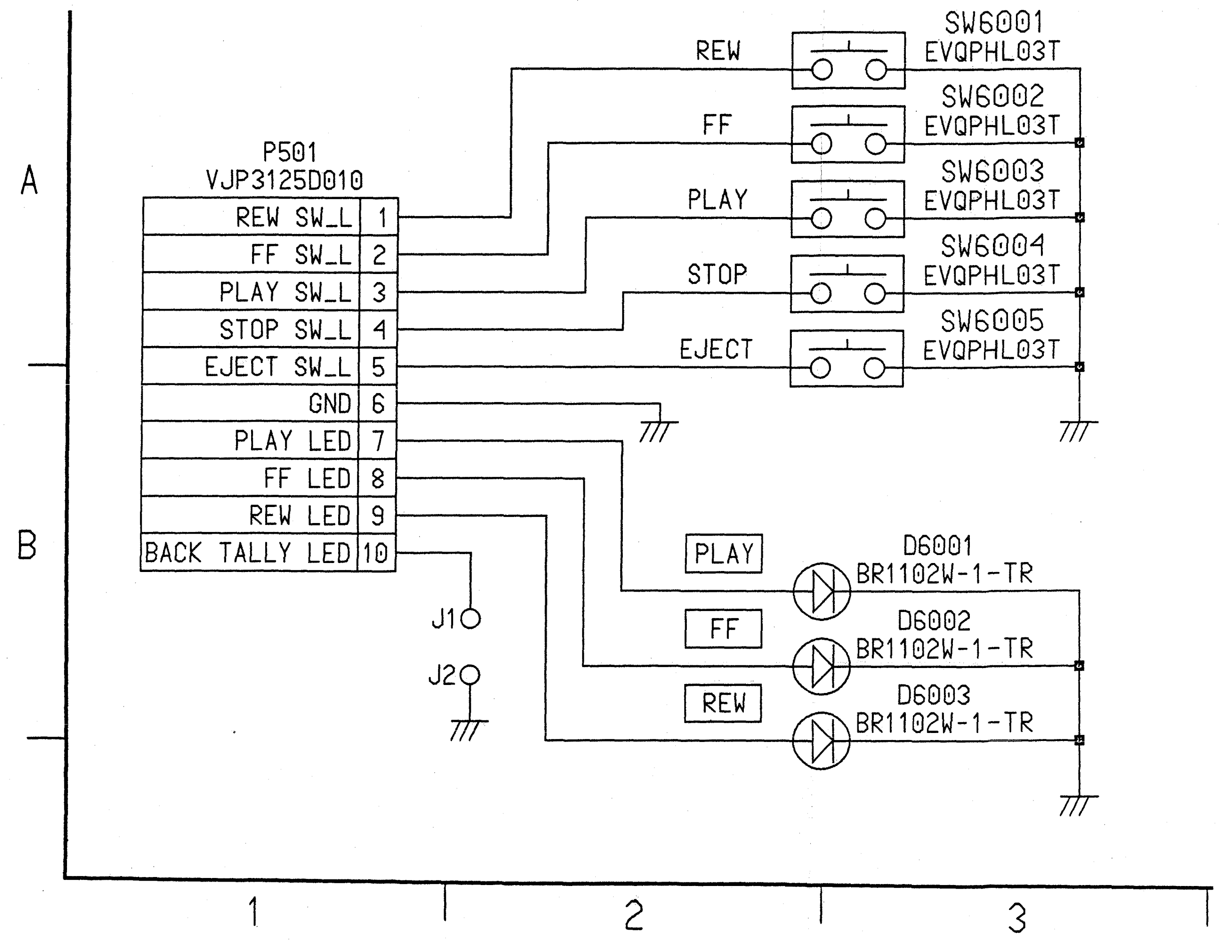
REVERSE SIDE

REAR JACK 1/3

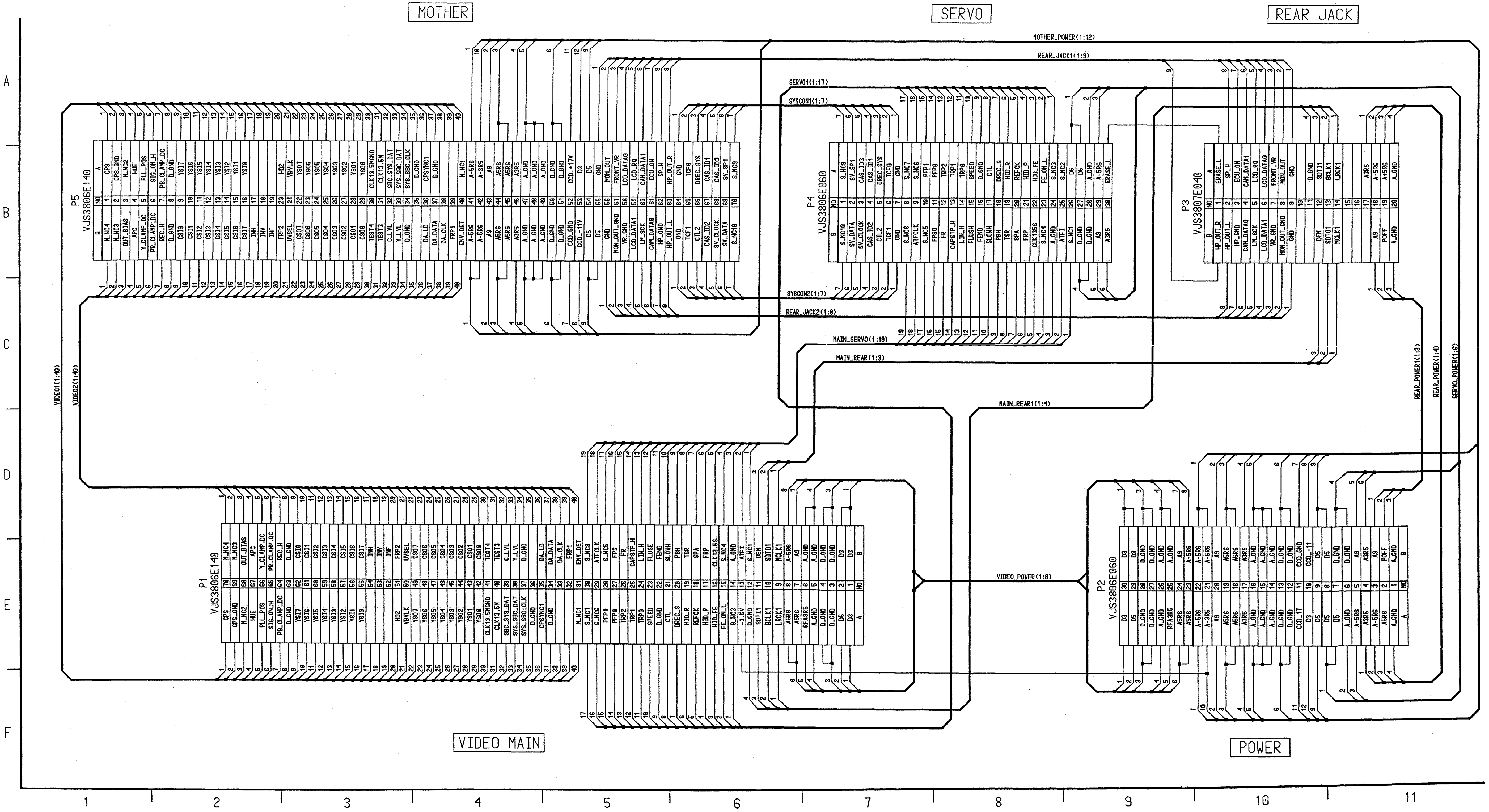
REAR JACK (3/3) COMPARISON CHART BETWEEN MODELS

REF	T	P. EN	E	ON
P1016	VJP3551	VJS3551	VJS3551	VJP3551
P1017	VJP3551	VJS3551	VJS3551	VJP3551
P1018	VJS3551	VJP3551	VJP3551	VJS3551
R1003	*PAT/J3	0/J3	VLF1315A102T	0/J3
R1004	0/J3	*PAT/J3	*PAT/J3	0/J3
R1005	0/J3	*PAT/J3	*PAT/J3	0/J3
R1006	*PAT/J3	0/J3	VLF1315A102T	0/J3
R1007	*PAT/J3	0/J3	VLF1315A102T	0/J3
R1008	0/J3	*PAT/J3	*PAT/J3	0/J3
R1009	0/J3	*PAT/J3	*PAT/J3	0/J3
R1010	*PAT/J3	0/J3	VLF1315A102T	0/J3
R1011	0/J3	*PAT/J3	*PAT/J3	0/J3
R1012	*PAT/J3	0/J3	VLF1315A102T	0/J3
R1013	*PAT/J3	0/J3	VLF1315A102T	0/J3
R1014	0/J3	*PAT/J3	*PAT/J3	0/J3
R1041	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R1050	*PAT/J3	*PAT/J3	*PAT/J3	0/J3
R1051	*PAT/J3	*PAT/J3	*PAT/J3	0/J3

OPERATE SCHEMATIC DIAGRAM


A
B
P501
VJP3125D010
REW SW_L 1
FF SW_L 2
PLAY SW_L 3
STOP SW_L 4
EJECT SW_L 5
GND 6
PLAY LED 7
FF LED 8
REW LED 9
BACK TALLY LED 10
J1
J2
REW
FF
PLAY
STOP
EJECT
SW6001
EVQPHL03T
SW6002
EVQPHL03T
SW6003
EVQPHL03T
SW6004
EVQPHL03T
SW6005
EVQPHL03T
PLAY
FF
REW
D6001
BR1102W-1-TR
D6002
BR1102W-1-TR
D6003
BR1102W-1-TR
1
2
3

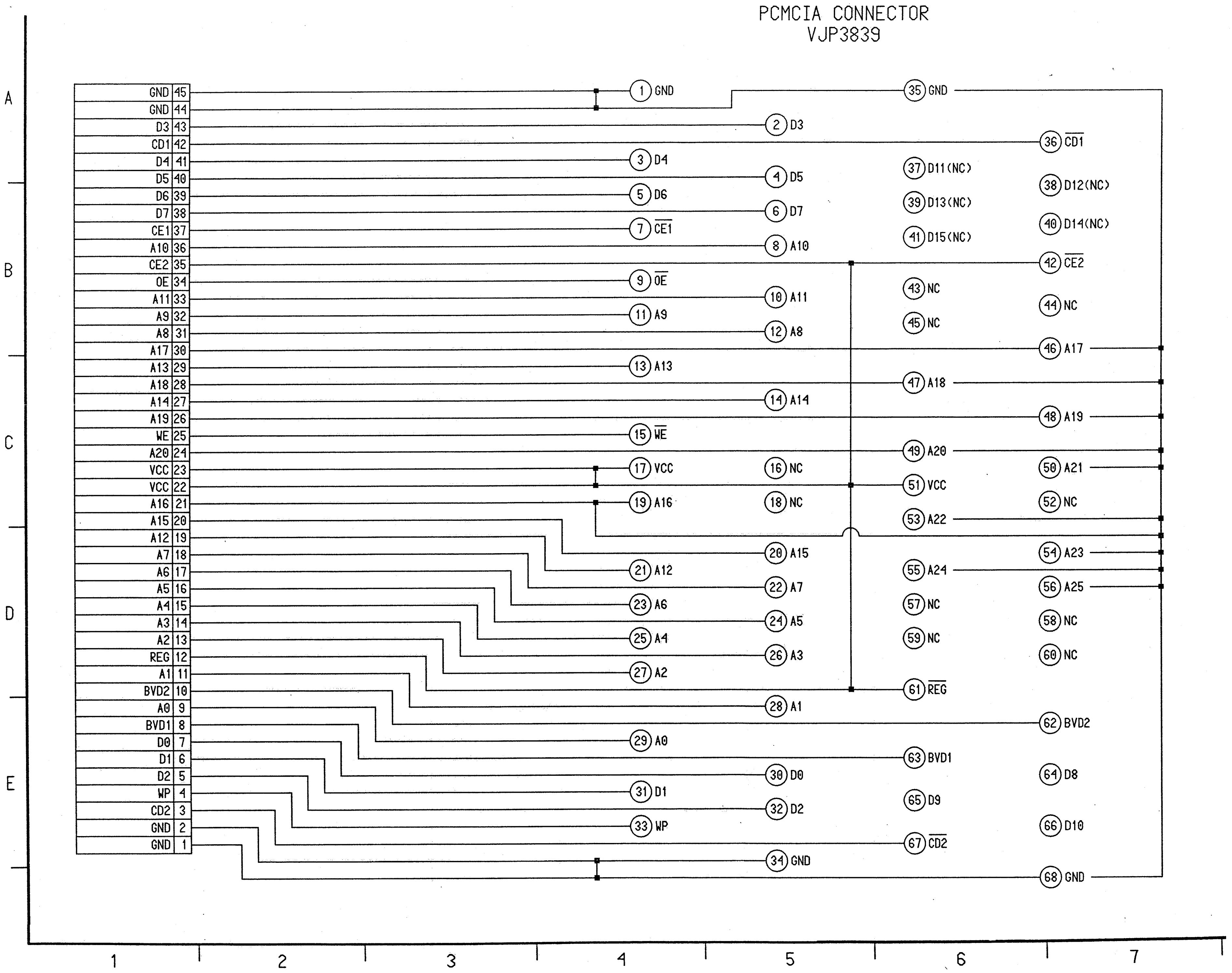
VTR FLEX SCHEMATIC DIAGRAM


MOTHER
SERVO
REAR JACK
VIDEO MAIN
POWER
P5
VJS3806E140
P4
VJS3806E060
P3
VJS3807E040
P1
VJS3806E140
P2
VJS3806E060
MOTHER_POWER(1:12)
REAR_JACK1(1:9)
SERVO1(1:17)
SYSCON1(1:7)
SYSCON2(1:7)
REAR_JACK2(1:8)
MAIN_SERVO(1:19)
MAIN_REAR(1:3)
MAIN_REAR1(1:4)
VIDEO1(1:40)
VIDEO2(1:40)
VIDEO_POWER(1:8)
REAR_POWER1(1:3)
REAR_POWER(1:4)
SERVO_POWER(1:6)
A
B
C
D
E
F
1
2
3
4
5
6
7
8
9
10
11

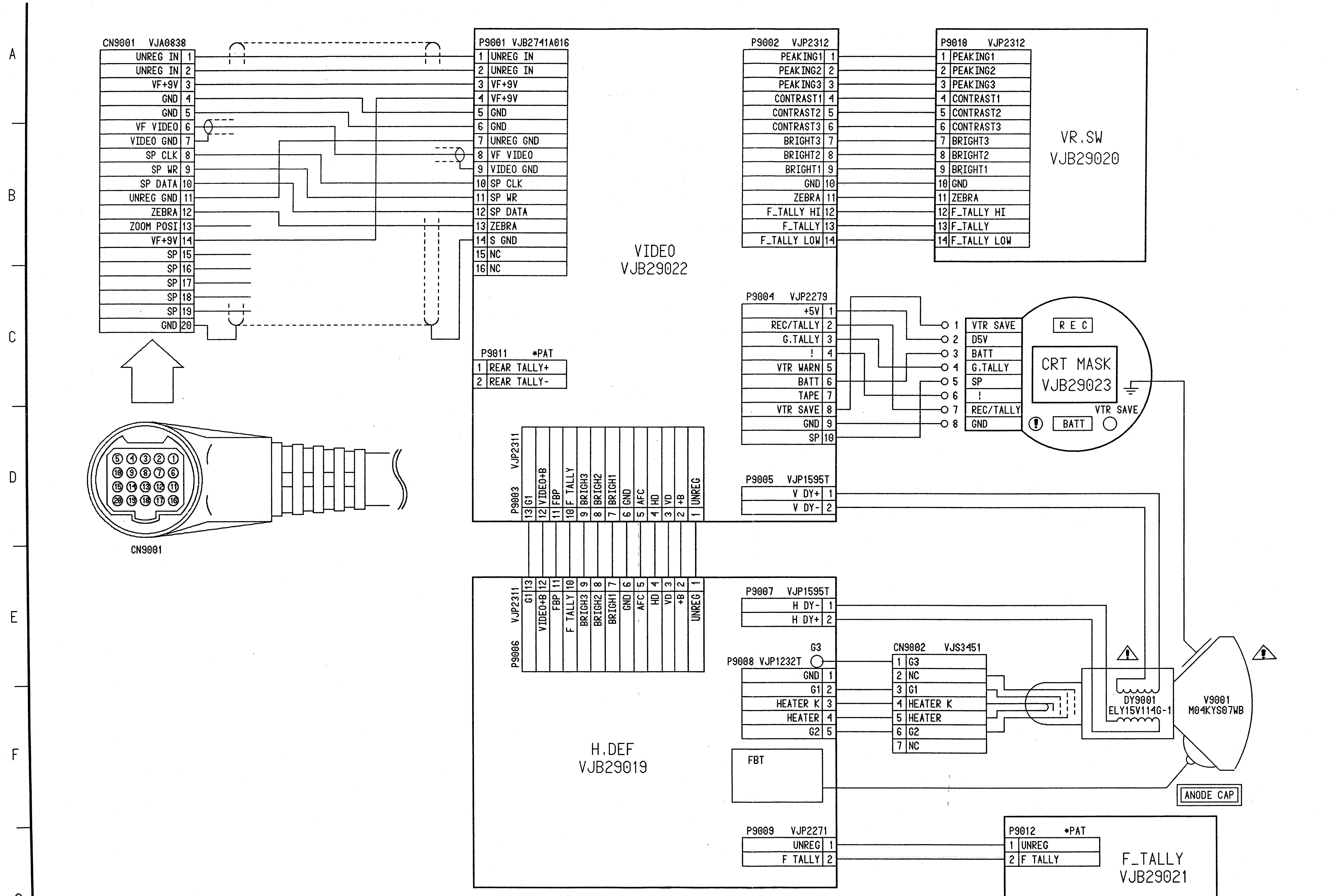
REVERSE SIDE

REAR JACK 3/3, OPERATE

MEMORY CARD FLEX SCHEMATIC DIAGRAM


PCMCIA CONNECTOR
VJP3839
GND 45
GND 44
D3 43
CD1 42
D4 41
D5 40
D6 39
D7 38
CE1 37
A10 36
CE2 35
OE 34
A11 33
A9 32
A8 31
A17 30
A13 29
A18 28
A14 27
A19 26
WE 25
A20 24
VCC 23
VCC 22
A16 21
A15 20
A12 19
A7 18
A6 17
A5 16
A4 15
A3 14
A2 13
REG 12
A1 11
BVD2 10
A0 9
BVD1 8
D0 7
D1 6
D2 5
WP 4
CD2 3
GND 2
GND 1
① GND
② D3
③ D4
④ D5
⑤ D6
⑥ D7
⑦ CE1
⑧ A10
⑨ OE
⑩ A11
⑪ A9
⑫ A8
⑬ A13
⑭ A14
⑮ WE
⑯ NC
⑰ VCC
⑱ NC
⑲ A16
⑳ A15
㉑ A12
㉒ A7
㉓ A6
㉔ A5
㉕ A4
㉖ A3
㉗ A2
㉘ A1
㉙ A0
㉚ D0
㉛ D1
㉜ D2
㉝ WP
㉞ GND
㉟ GND
㊱ CD1
㊲ D11(NC)
㊳ D12(NC)
㊴ D13(NC)
㊵ D14(NC)
㊶ D15(NC)
㊷ CE2
㊸ NC
㊹ NC
㊺ NC
㊻ A17
㊼ A18
㊽ A19
㊾ A20
㊿ A21
(51) VCC
(52) NC
(53) A22
(54) A23
(55) A24
(56) A25
(57) NC
(58) NC
(59) NC
(60) NC
(61) REG
(62) BVD2
(63) BVD1
(64) D8
(65) D9
(66) D10
(67) CD2
(68) GND
A
B
C
D
E
1
2
3
4
5
6
7

EVF INTERCONNECTION

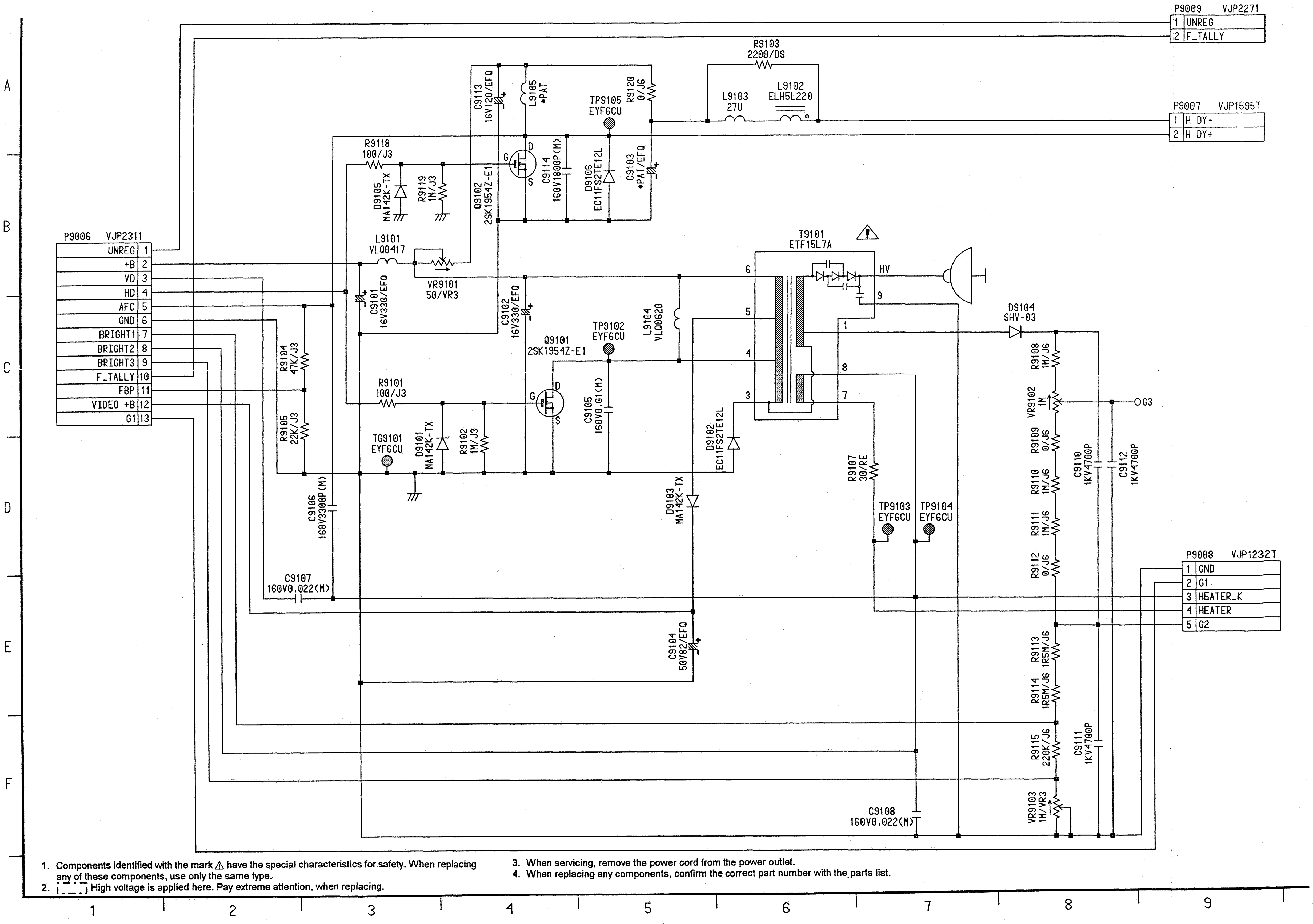

A
B
C
D
E
F
G
CN9001 VJA0838
UNREG IN 1
UNREG IN 2
VF+9V 3
GND 4
GND 5
VF VIDEO 6
VIDEO GND 7
SP CLK 8
SP WR 9
SP DATA 10
UNREG GND 11
ZEBRA 12
ZOOM POSI 13
VF+9V 14
SP 15
SP 16
SP 17
SP 18
SP 19
GND 20
CN9001
P9001 VJB2741A016
1 UNREG IN
2 UNREG IN
3 VF+9V
4 VF+9V
5 GND
6 GND
7 UNREG GND
8 VF VIDEO
9 VIDEO GND
10 SP CLK
11 SP WR
12 SP DATA
13 ZEBRA
14 S GND
15 NC
16 NC
VIDEO
VJB29022
P9011 *PAT
1 REAR TALLY+
2 REAR TALLY-
P9002 VJP2312
PEAKING1 1
PEAKING2 2
PEAKING3 3
CONTRAST1 4
CONTRAST2 5
CONTRAST3 6
BRIGHT3 7
BRIGHT2 8
BRIGHT1 9
GND 10
ZEBRA 11
F_TALLY HI 12
F_TALLY 13
F_TALLY LOW 14
P9010 VJP2312
1 PEAKING1
2 PEAKING2
3 PEAKING3
4 CONTRAST1
5 CONTRAST2
6 CONTRAST3
7 BRIGHT3
8 BRIGHT2
9 BRIGHT1
10 GND
11 ZEBRA
12 F_TALLY HI
13 F_TALLY
14 F_TALLY LOW
VR.SW
VJB29020
P9004 VJP2279
+5V 1
REC/TALLY 2
G.TALLY 3
! 4
VTR WARN 5
BATT 6
TAPE 7
VTR SAVE 8
GND 9
SP 10
1 VTR SAVE
2 D5V
3 BATT
4 G.TALLY
5 SP
6 !
7 REC/TALLY
8 GND
R E C
CRT MASK
VJB29023
VTR SAVE
BATT
P9003 VJP2311
13 G1
12 VIDEO+B
11 FBP
10 F TALLY
9 BRIGH3
8 BRIGH2
7 BRIGH1
6 GND
5 AFC
4 HD
3 VD
2 +B
1 UNREG
P9005 VJP1595T
V DY+ 1
V DY- 2
P9006 VJP2311
G1 13
VIDEO+B 12
FBP 11
F TALLY 10
BRIGH3 9
BRIGH2 8
BRIGH1 7
GND 6
AFC 5
HD 4
VD 3
+B 2
UNREG 1
P9007 VJP1595T
H DY- 1
H DY+ 2
G3
P9008 VJP1232T
GND 1
G1 2
HEATER K 3
HEATER 4
G2 5
CN9002 VJS3451
1 G3
2 NC
3 G1
4 HEATER K
5 HEATER
6 G2
7 NC
DY9001
ELY15V114G-1
V9001
M04KYS07WB
ANODE CAP
H.DEF
VJB29019
FBT
P9009 VJP2271
UNREG 1
F TALLY 2
P9012 *PAT
1 UNREG
2 F TALLY
F_TALLY
VJB29021

1. Components identified with the mark ⚠ have the special characteristics for safety. When replacing any of these components, use only the same type.
2. [- - -] High voltage is applied here. Pay extreme attention, when replacing.
3. When servicing, remove the power cord from the power outlet.
4. When replacing any components, confirm the correct part number with the parts list.

1 2 3 4 5 6 7 8 9

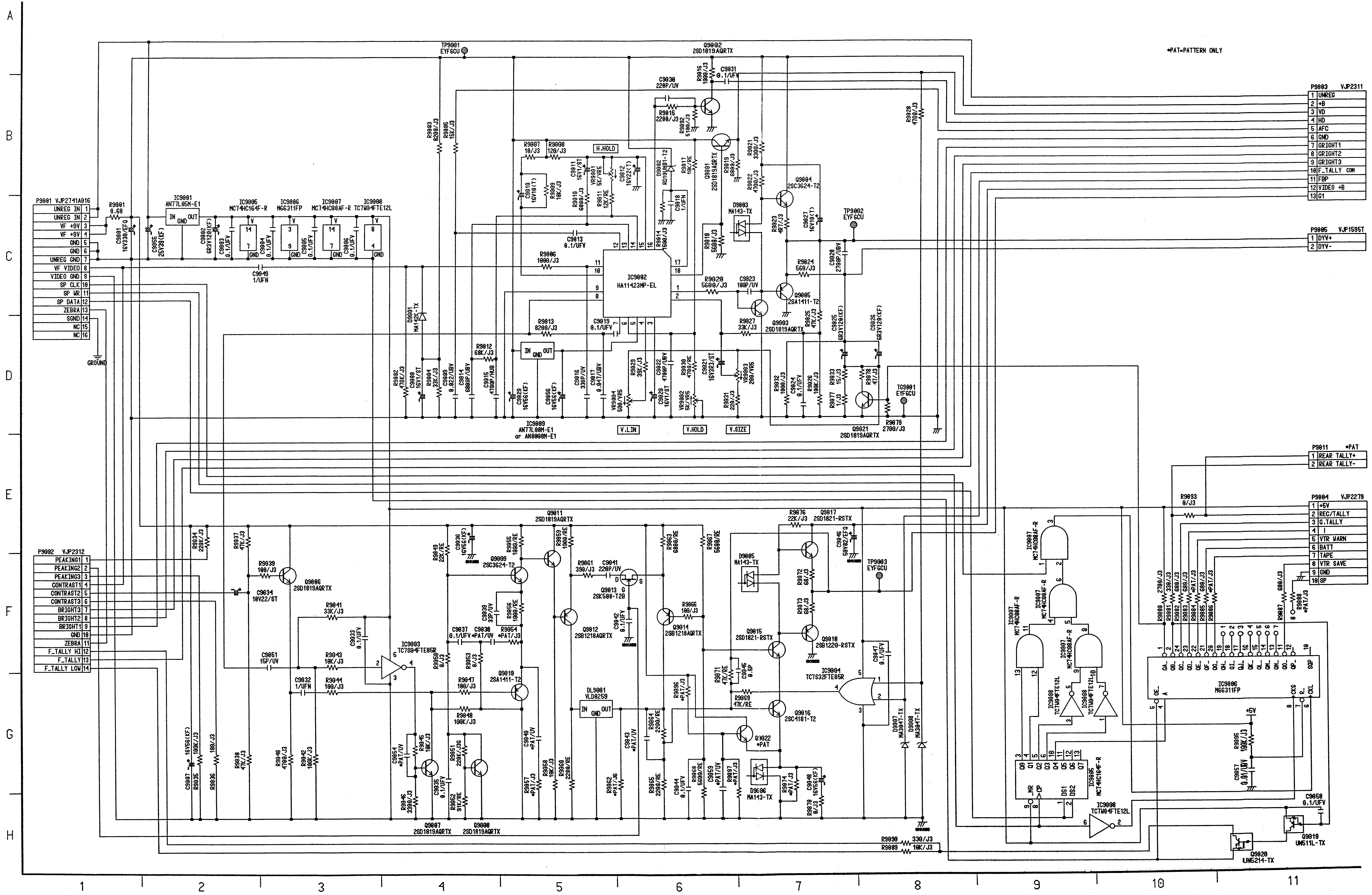
REVERSE SIDE
MEMORY CARD FLEX

H. DEF SCHEMATIC DIAGRAM


P9009 VJP2271
1 UNREG
2 F_TALLY
R9103 2200/DS
L9103 27U
L9102 ELH5L220
P9007 VJP1595T
1 H DY-
2 H DY+
C9113 16V120/EFQ
L9105 *PAT
TP9105 EYF6CU
R9120 0/J6
R9118 100/J3
D9105 MA142K-TX
R9119 1M/J3
Q9102 2SK1954Z-E1
C9114 160V1800P(M)
D9106 EC11FS2TE12L
C9103 *PAT/EFQ
P9006 VJP2311
UNREG 1
+B 2
VD 3
HD 4
AFC 5
GND 6
BRIGHT1 7
BRIGHT2 8
BRIGHT3 9
F_TALLY 10
FBP 11
VIDEO +B 12
G1 13
L9101 VLQ0417
VR9101 50/VR3
C9101 16V330/EFQ
C9102 16V330/EFQ
Q9101 2SK1954Z-E1
TP9102 EYF6CU
L9104 VLQ0620
T9101 ETF15L7A
HV
D9104 SHV-03
R9104 47K/J3
R9105 22K/J3
R9101 100/J3
TG9101 EYF6CU
D9101 MA142K-TX
R9102 1M/J3
C9105 160V0.01(M)
D9102 EC11FS2TE12L
D9103 MA142K-TX
R9107 30/RE
TP9103 EYF6CU
TP9104 EYF6CU
R9108 1M/J6
VR9102 1M
G3
R9109 0/J6
R9110 1M/J6
R9111 1M/J6
R9112 0/J6
C9110 1KV4700P
C9112 1KV4700P
C9106 160V3300P(M)
C9107 160V0.022(M)
P9008 VJP1232T
1 GND
2 G1
3 HEATER_K
4 HEATER
5 G2
C9104 50V82/EFQ
R9113 1R5M/J6
R9114 1R5M/J6
R9115 220K/J6
C9111 1KV4700P
VR9103 1M/VR3
C9108 160V0.022(M)
A
B
C
D
E
F
1
2
3
4
5
6
7
8
9

1. Components identified with the mark ⚠ have the special characteristics for safety. When replacing any of these components, use only the same type.
2. ⌐- - -¬ High voltage is applied here. Pay extreme attention, when replacing.
3. When servicing, remove the power cord from the power outlet.
4. When replacing any components, confirm the correct part number with the parts list.

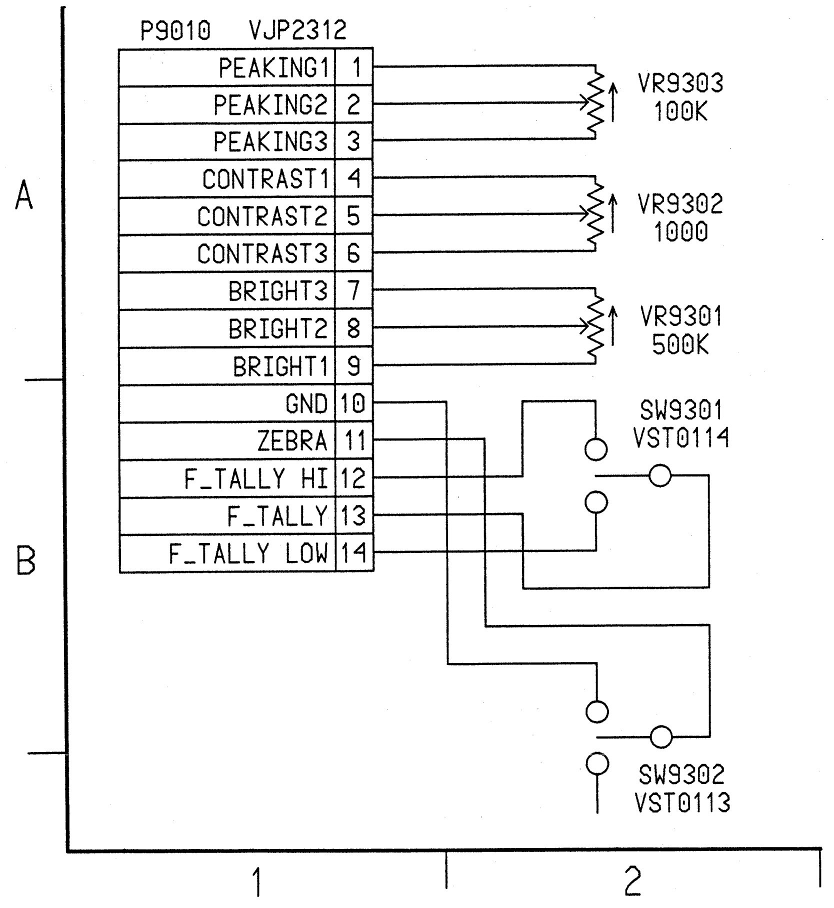
EVF CRT MASK SCHEMATIC DIAGRAM


*PAT=PATTERN ONLY
P9001 VJP2741A016
UNREG IN 1
UNREG IN 2
VF +9V 3
VF +9V 4
GND 5
GND 6
UNREG GND 7
VF VIDEO 8
VIDEO GND 9
SP CLK 10
SP WR 11
SP DATA 12
ZEBRA 13
SGND 14
NC 15
NC 16
GROUND
R9001 0.68
C9001 16V330/EFQ
C9055 25V39(KF)
IC9001 AN77L05M-E1
C9002 6R3V120(KF)
C9003 0.1/UFV
IC9005 MC74HC164F-R
IC9006 M66311FP
IC9007 MC74HC08AF-R
IC9008 TC7W04FTE12L
C9049 1/UFN
TP9001 EYF6CU
Q9002 2SD1819AQRTX
IC9002 HA11423MP-EL
IC9009 AN77L08M-E1 or AN8008M-E1
H.HOLD
V.LIN
V.HOLD
V.SIZE
Q9001 2SD1819AQRTX
Q9004 2SC3624-T2
Q9005 2SA1411-T2
Q9003 2SD1819AQRTX
D9003 MA143-TX
D9001 MA142K-TX
TP9002 EYF6CU
TG9001 EYF6CU
Q9021 2SD1819AQRTX
P9003 VJP2311
1 UNREG
2 +B
3 VD
4 HD
5 AFC
6 GND
7 GRIGHT1
8 GRIGHT2
9 GRIGHT3
10 F_TALLY COM
11 FBP
12 VIDEO +B
13 G1
P9005 VJP1595T
1 DYV+
2 DYV-
P9011 *PAT
1 REAR TALLY+
2 REAR TALLY-
P9004 VJP2279
1 +5V
2 REC/TALLY
3 G.TALLY
4 I
5 VTR WARN
6 BATT
7 TAPE
8 VTR SAVE
9 GND
10 SP
P9002 VJP2312
PEAKING1 1
PEAKING2 2
PEAKING3 3
CONTRAST1 4
CONTRAST2 5
CONTRAST3 6
BRIGHT3 7
BRIGHT2 8
BRIGHT1 9
GND 10
ZEBRA 11
F_TALLY HI 12
F_TALLY 13
F_TALLY LOW 14
Q9006 2SD1819AQRTX
IC9003 TC7S04FTE85R
Q9009 2SC3624-T2
Q9011 2SD1819AQRTX
Q9010 2SA1411-T2
Q9012 2SB1218AQRTX
Q9013 2SK508-T2B
Q9014 2SB1218AQRTX
DL9001 VLD0259
Q9007 2SD1819AQRTX
Q9008 2SD1819AQRTX
Q9017 2SD1821-RSTX
Q9015 2SD1821-RSTX
Q9018 2SB1220-RSTX
Q9016 2SC4181-T2
Q9022 *PAT
D9005 MA143-TX
D9006 MA143-TX
D9007 MA3047-TX
D9008 MA3047-TX
IC9004 TC7S32FTE85R
TP9003 EYF6CU
IC9006 M66311FP
IC9005 MC74HC164F-R
Q9019 UN511L-TX
Q9020 UN5214-TX
R9090 330/J3
R9089 10K/J3
A
B
C
D
E
F
G
H
1
2
3
4
5
6
7
8
9
10
11

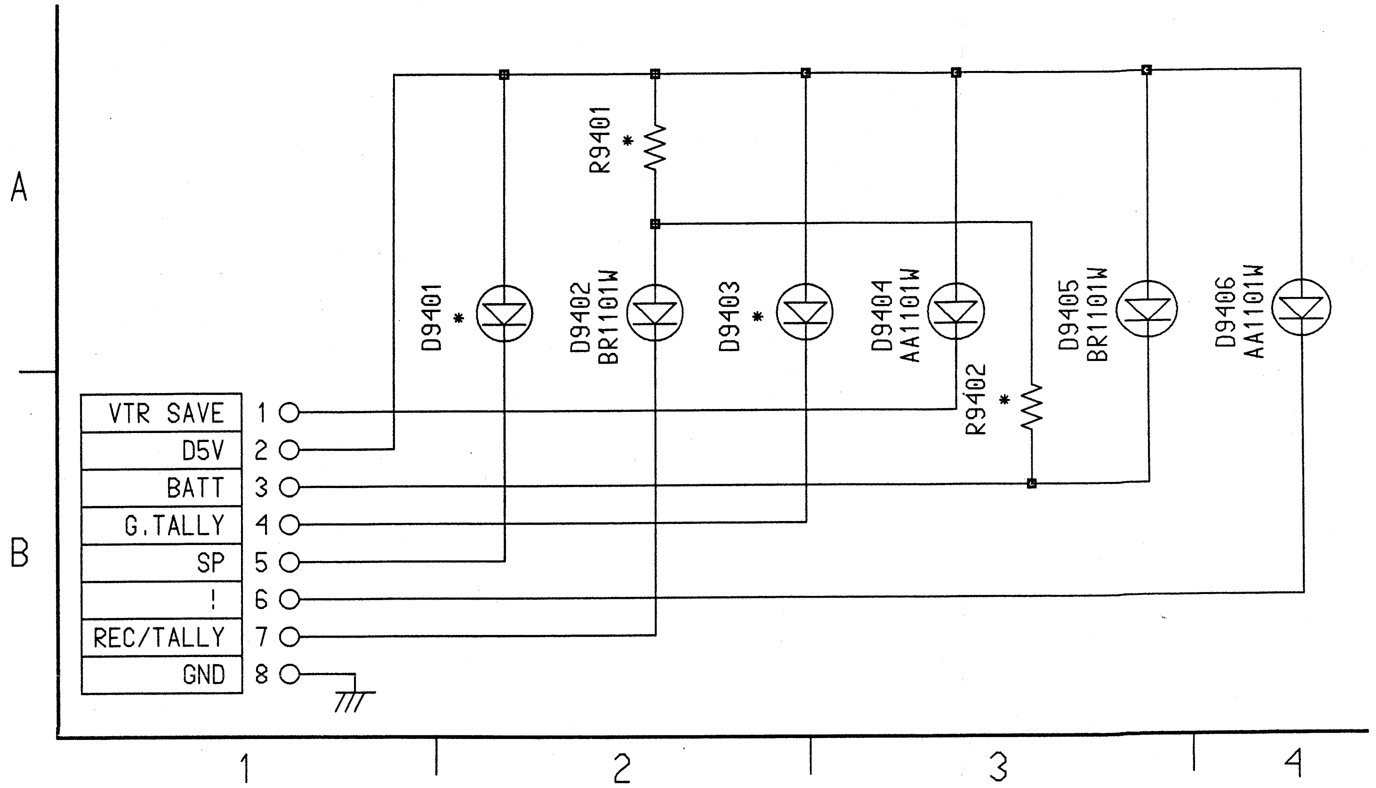
REVERSE SIDE

H DEF

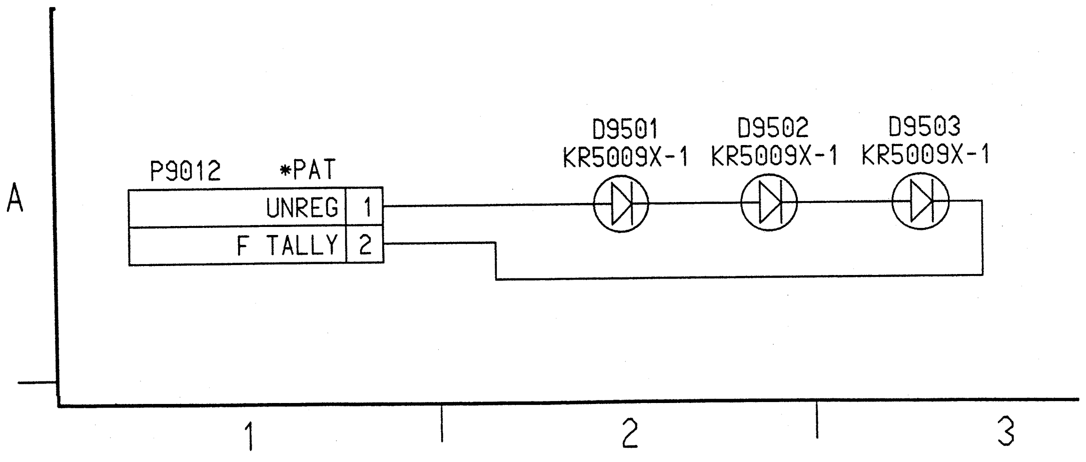
EVF VIDEO SCHEMATIC DIAGRAM


P9010 VJP2312
PEAKING1 1
PEAKING2 2
PEAKING3 3
CONTRAST1 4
CONTRAST2 5
CONTRAST3 6
BRIGHT3 7
BRIGHT2 8
BRIGHT1 9
GND 10
ZEBRA 11
F_TALLY HI 12
F_TALLY 13
F_TALLY LOW 14
VR9303
100K
VR9302
1000
VR9301
500K
SW9301
VST0114
SW9302
VST0113
A
B
1
2

EVF SWVR SCHEMATIC DIAGRAM


R9401
*
D9401
*
D9402
BR1101W
D9403
*
D9404
AA1101W
R9402
*
D9405
BR1101W
D9406
AA1101W
VTR SAVE 1
D5V 2
BATT 3
G.TALLY 4
SP 5
! 6
REC/TALLY 7
GND 8
A
B
1
2
3
4

F TALLY SCHEMATIC DIAGRAM


P9012 *PAT
UNREG 1
F TALLY 2
D9501
KR5009X-1
D9502
KR5009X-1
D9503
KR5009X-1
A
1
2
3

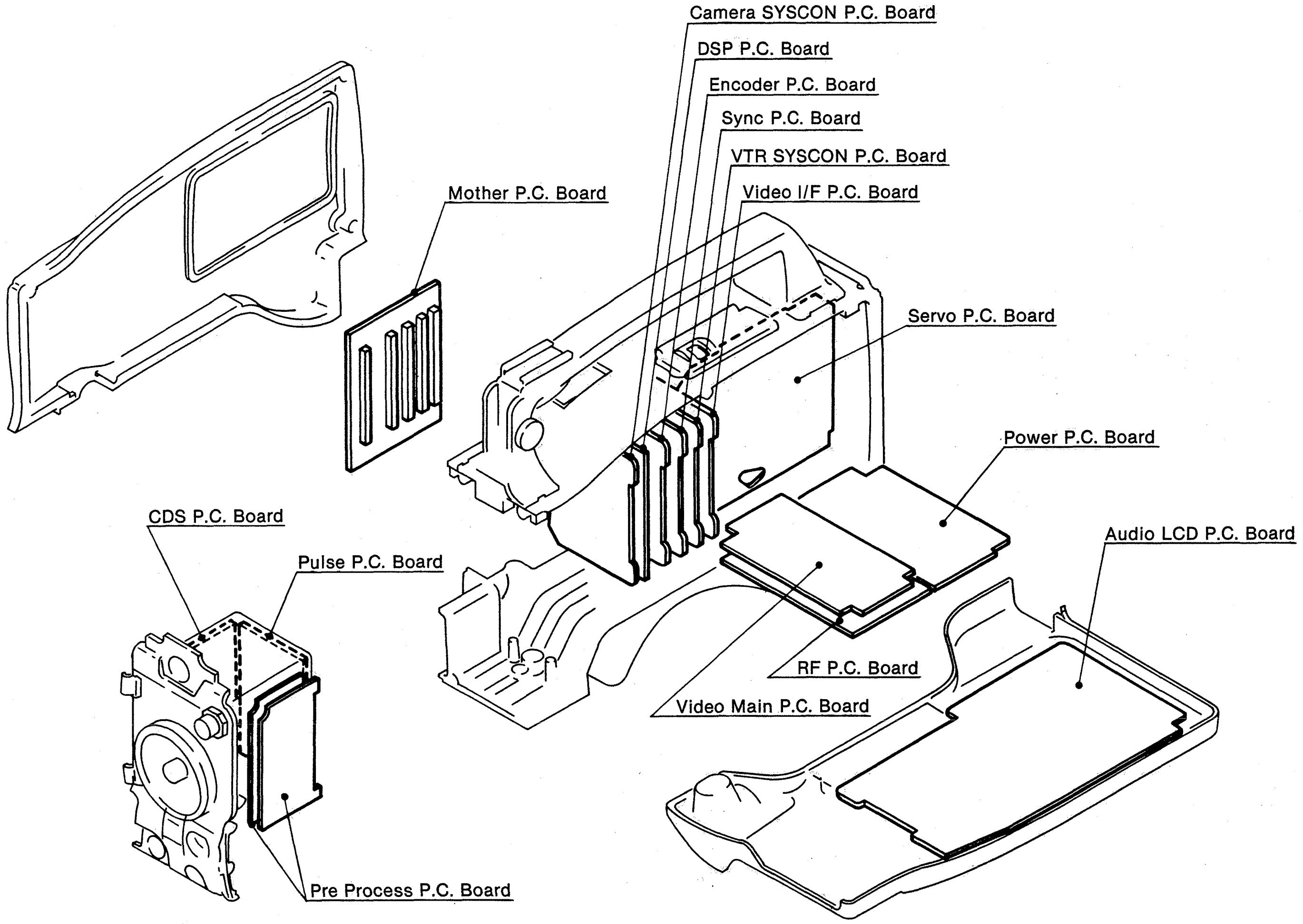
SECTION 3

CIRCUIT BOARDS

Circuit Board Diagrams

Circuit Board Location ························· 3-1
CDS ························· 3-1
PULSE ························· 3-2
PRE PROCESS ························· 3-3
MOTHER ························· 3-4
CAMERA SYSCON ························· 3-5
CAMERA DSP ························· 3-6
CAMERA ENCODER ························· 3-7
CAMERA SYNC ························· 3-8
VIDEO IF ························· 3-9
VTR SYSCON ························· 3-10
SERVO ························· 3-11
VIDEO MAIN ························· 3-12
RF ························· 3-13
POWER ························· 3-14
AUDIO LCD ························· 3-16
REAR JACK/BNC/FRONT MIC ························· 3-17

P.C. BOARD LOCATION


Camera SYSCON P.C. Board
DSP P.C. Board
Encoder P.C. Board
Sync P.C. Board
VTR SYSCON P.C. Board
Video I/F P.C. Board
Mother P.C. Board
Servo P.C. Board
Power P.C. Board
CDS P.C. Board
Pulse P.C. Board
Audio LCD P.C. Board
RF P.C. Board
Video Main P.C. Board
Pre Process P.C. Board

CDS

Transistors		
Q3001	B-3	©
Q3101	B-2	Ⓕ
Q3102	B-2	Ⓕ
Q3103	B-2	Ⓕ
Q3104	B-2	Ⓕ
Q3105	B-2	Ⓕ
Q3106	B-2	Ⓕ
Q3107	B-3	©
Q3108	B-2	©
Q3109	B-2	©
Q3110	B-2	©
Q3111	B-2	©
Q3112	B-2	©
Q3113	B-1	©
Q3114	B-2	©
Q3115	B-1	©
Q3116	B-1	Ⓕ
Q3117	B-1	Ⓕ
Q3118	B-1	Ⓕ
Q3119	B-1	Ⓕ
Q3120	B-1	Ⓕ
Q3121	B-1	Ⓕ
Q3122	B-1	Ⓕ
Q3123	B-2	Ⓕ
Q3201	B-3	Ⓕ
Q3202	A-2	Ⓕ
Q3203	A-2	Ⓕ
Q3204	A-2	Ⓕ
Q3205	A-2	Ⓕ
Q3206	A-2	Ⓕ
Q3207	A-3	©
Q3208	A-2	©
Q3209	A-2	©
Q3210	A-2	©
Q3211	A-2	©
Q3212	A-2	©
Q3213	A-2	©
Q3214	A-2	©
Q3215	A-1	©
Q3216	A-2	Ⓕ
Q3217	A-2	Ⓕ
Q3218	A-1	Ⓕ
Q3219	A-1	Ⓕ
Q3220	A-1	Ⓕ
Q3221	A-1	Ⓕ
Q3222	A-1	Ⓕ
Q3301	A-3	Ⓕ
Q3302	A-2	Ⓕ
Q3303	A-2	Ⓕ
Q3304	A-2	Ⓕ
Q3305	A-2	Ⓕ
Q3306	A-2	Ⓕ
Q3307	A-3	©
Q3308	A-2	©
Q3309	A-2	©
Q3310	A-2	©
Q3311	A-2	©
Q3312	A-2	©
Q3313	A-2	©
Q3314	A-2	©
Q3315	A-1	©
Q3316	A-2	Ⓕ
Q3317	A-2	Ⓕ
Q3318	A-1	Ⓕ
Q3319	A-1	Ⓕ
Q3321	A-1	Ⓕ
Q3322	A-1	Ⓕ
Q3323	A-1	Ⓕ

Transistor-Resistors		
QR3101	B-3	Ⓕ
QR3102	B-3	©
QR3201	A-3	Ⓕ
QR3202	A-3	©
QR3301	A-3	Ⓕ
QR3302	A-3	©

Integrated Circuit		
IC3001	B-3	Ⓕ
IC3002	B-3	©

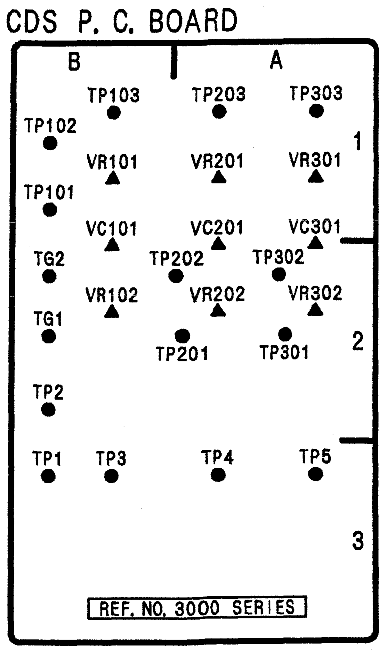
Test Points		
TP3001	B-3	Ⓕ
TP3002	B-2	Ⓕ
TP3003	B-3	Ⓕ
TP3004	A-3	Ⓕ
TP3005	A-3	Ⓕ
TP3101	B-1	Ⓕ
TP3102	B-1	Ⓕ
TP3103	B-1	Ⓕ
TP3201	A-2	Ⓕ
TP3202	A-2	Ⓕ
TP3203	A-1	Ⓕ
TP3301	A-2	Ⓕ
TP3302	A-2	Ⓕ
TP3303	A-1	Ⓕ
TG3001	B-2	Ⓕ
TG3002	B-2	Ⓕ

Adjustments		
VC3101	B-2	Ⓕ
VC3201	A-2	Ⓕ
VC3301	A-2	Ⓕ
VR3101	B-1	Ⓕ
VR3102	B-2	Ⓕ
VR3201	B-1	Ⓕ
VR3202	A-2	Ⓕ
VR3301	A-1	Ⓕ
VR3302	A-2	Ⓕ

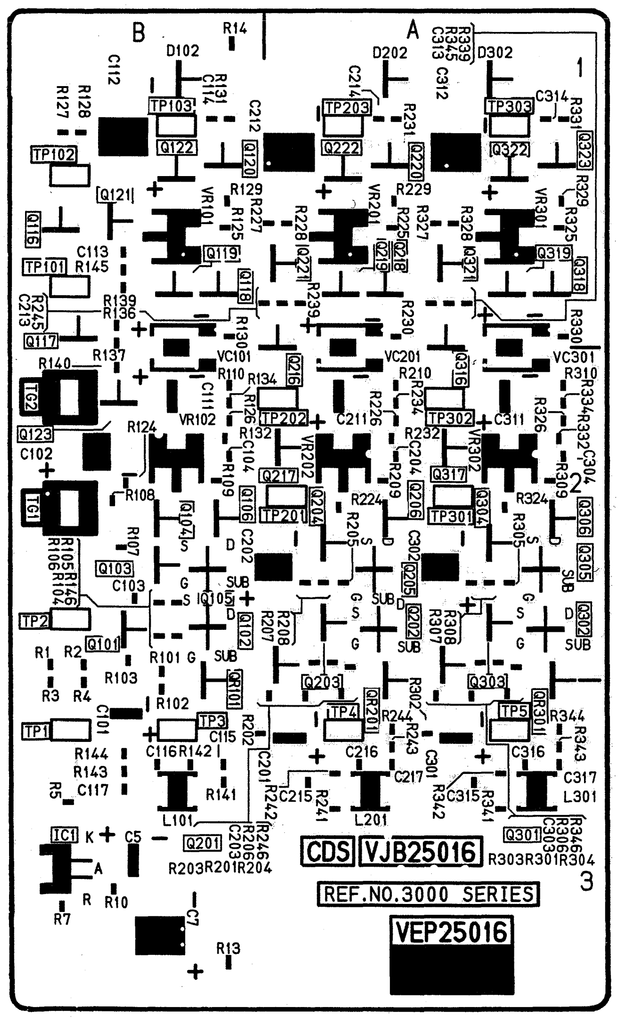
Connectors		
P3001	A-3	©
P3002	B-2	©
P3003	A-1	©

ADDRESS INFORMATION
©... COMPONENT SIDE
Ⓕ... FOIL SIDE

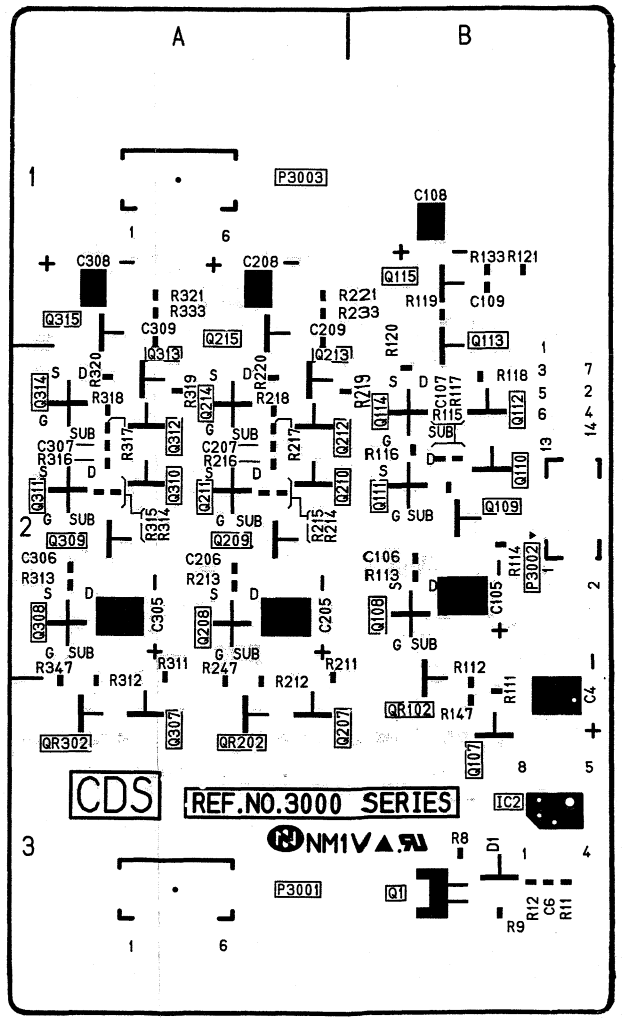
CDS P.C. BOARD (VEP25016B)


CDS P. C. BOARD
B
A
TP103
TP203
TP303
TP102
1
VR101
VR201
VR301
TP101
VC101
VC201
VC301
TG2
TP202
TP302
VR102
VR202
VR302
TG1
TP201
TP301
2
TP2
TP1
TP3
TP4
TP5
3
REF. NO. 3000 SERIES

(FOIL SIDE)


B
A
1
2
3
CDS
VJB25016
REF.NO.3000 SERIES
VEP25016
TP101
TP102
TP103
TP201
TP202
TP203
TP301
TP302
TP303
TP1
TP2
TP3
TP4
TP5
TG1
TG2
VR101
VR102
VR201
VR202
VR301
VR302
VC101
VC201
VC301
IC1

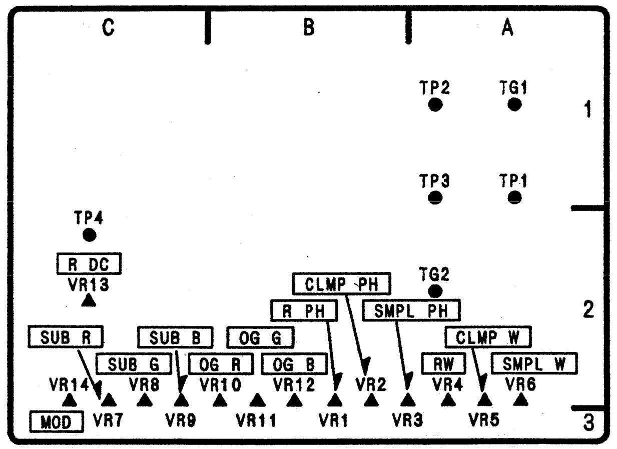
(FIOL SIDE)


A
B
1
2
3
P3003
P3001
P3002
CDS
REF.NO.3000 SERIES
NM1V
IC2
Q1
C108
C208
C308

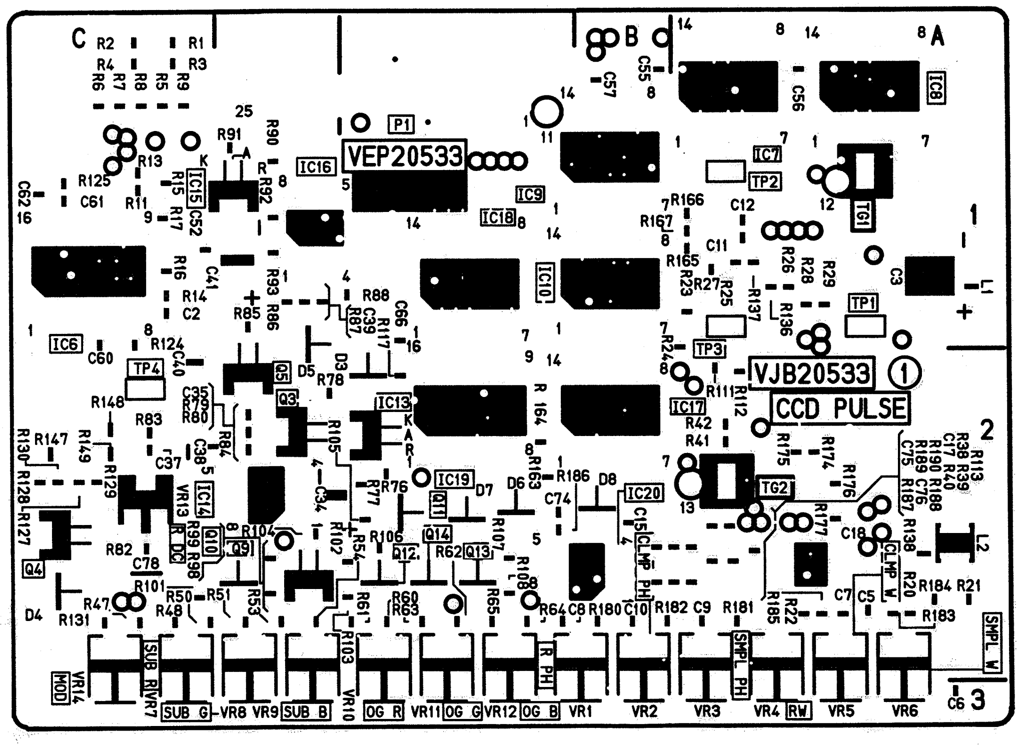
(COMPONENT SIDE)

PULSE P.C. BOARD (VEP20533B)

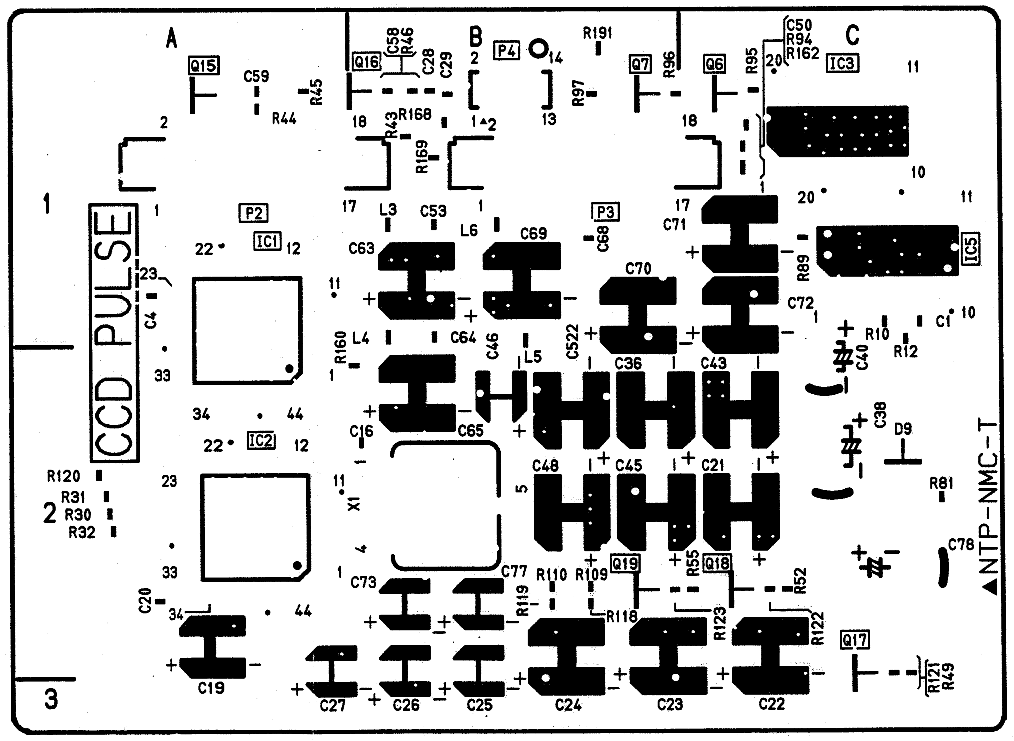
PULSE P. C. BOARD


C
B
A
TP2
TG1
1
TP3
TP1
TP4
R DC
VR13
CLMP PH
TG2
R PH
SMPL PH
2
SUB R
SUB B
OG G
CLMP W
SUB G
OG R
OG B
RW
SMPL W
VR14
VR8
VR10
VR12
VR2
VR4
VR6
MOD
VR7
VR9
VR11
VR1
VR3
VR5
3

(FOIL SIDE)


C
B
A
1
2
3
VEP20533
VJB20533
①
CCD PULSE
P1
IC6
IC7
IC8
IC9
IC10
IC13
IC14
IC15
IC16
IC17
IC18
IC19
IC20
Q3
Q4
Q5
Q9
Q10
Q11
Q12
Q13
Q14
TP1
TP2
TP3
TP4
TG1
TG2
R DC
MOD
SUB R
SUB G
SUB B
OG R
OG G
OG B
R PH
CLMP PH
SMPL PH
CLMP W
SMPL W
RW
VR1
VR2
VR3
VR4
VR5
VR6
VR7
VR8
VR9
VR10
VR11
VR12
VR13
VR14
L1
L2
D3
D4
D5
D6
D7
D8

(FIOL SIDE)

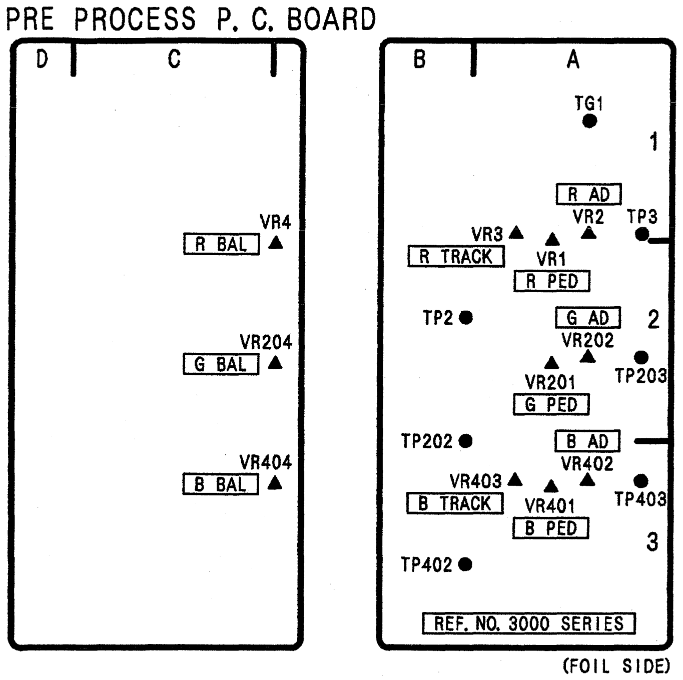

A
B
C
1
2
3
CCD PULSE
NTP-NMC-T
Q6
Q7
Q15
Q16
Q17
Q18
Q19
IC1
IC2
IC3
IC5
P2
P3
P4
X1
L3
L4
L5
L6
D9
C19
C22
C23
C24
C25
C26
C27
C36
C43
C45
C48
C21
C69
C70
C73
C77
C78
R120
R31
R30
R32

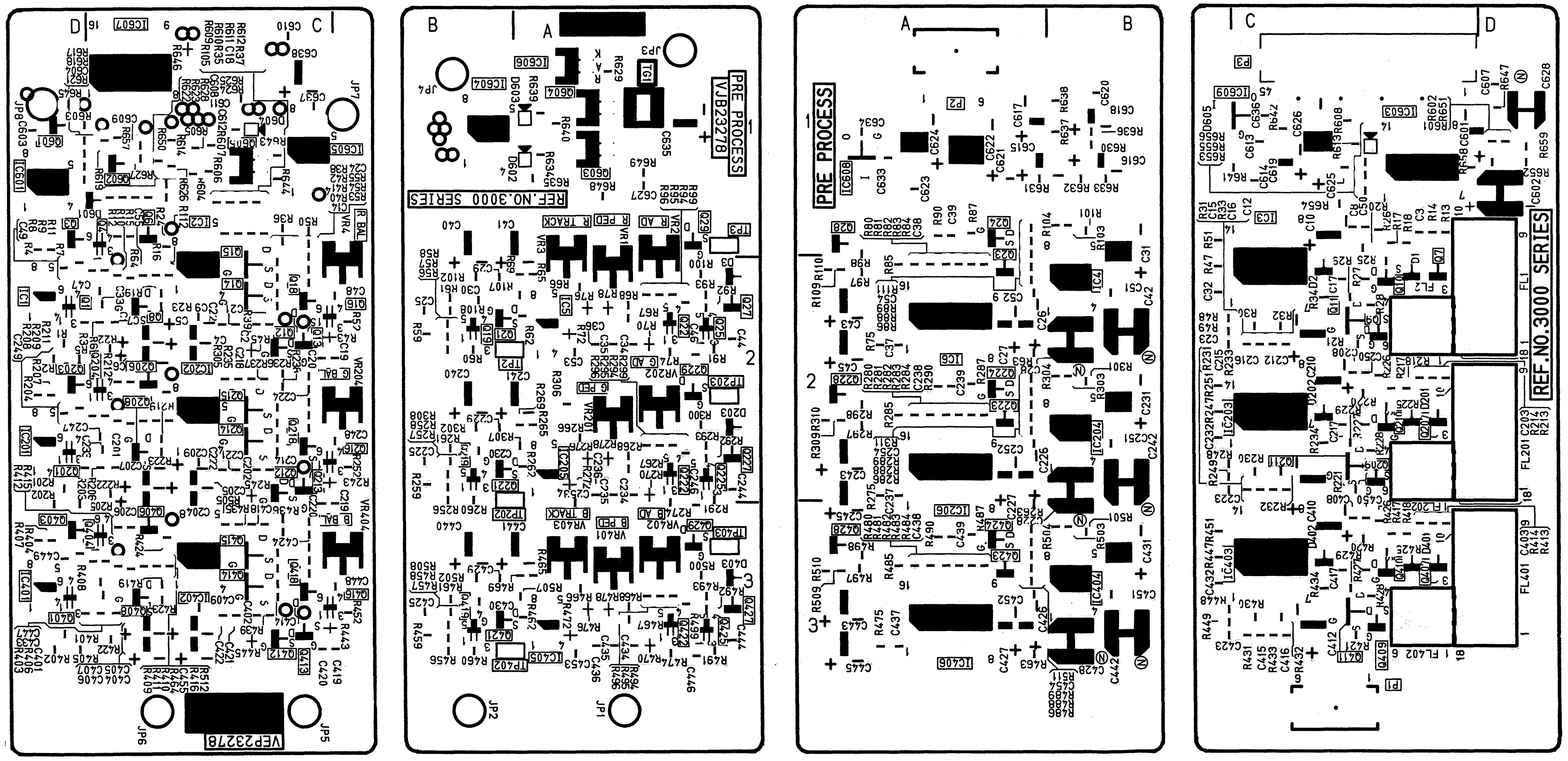
(COMPONENT SIDE)

PULSE		
Transistors		
Q3	C-2	Ⓕ
Q4	C-2	Ⓕ
Q5	C-2	Ⓕ
Q6	C-1	Ⓒ
Q7	B-1	Ⓒ
Q9	C-2	Ⓕ
Q10	C-2	Ⓕ
Q11	B-2	Ⓕ
Q12	B-2	Ⓕ
Q13	B-2	Ⓕ
Q14	B-2	Ⓕ
Q15	A-1	Ⓒ
Q16	B-1	Ⓒ
Q17	C-2	Ⓒ
Q18	C-2	Ⓒ
Q19	B-2	Ⓒ
Integrated Circuit		
IC1	A-1	Ⓒ
IC2	A-2	Ⓒ
IC3	C-1	Ⓒ
IC5	C-1	Ⓒ
IC6	C-1	Ⓕ
IC7	A-1	Ⓕ
IC8	A-1	Ⓕ
IC9	B-1	Ⓕ
IC10	B-1	Ⓕ
IC13	B-2	Ⓕ
IC14	C-2	Ⓕ
IC15	C-1	Ⓕ
IC16	C-1	Ⓕ
IC17	A-2	Ⓕ
IC18	B-1	Ⓕ
IC19	B-2	Ⓕ
IC20	B-2	Ⓕ
Test Points		
TP1	A-1	Ⓕ
TP2	A-1	Ⓕ
TP3	A-1	Ⓕ
TP4	C-2	Ⓕ
TG1	A-2	Ⓕ
TG2	A-2	Ⓕ
Adjustment		
VR1	B-3	Ⓕ
VR2	B-3	Ⓕ
VR3	A-3	Ⓕ
VR4	A-3	Ⓕ
VR5	A-3	Ⓕ
VR6	A-3	Ⓕ
VR7	C-3	Ⓕ
VR8	C-3	Ⓕ
VR9	C-3	Ⓕ
VR10	B-3	Ⓕ
VR11	B-3	Ⓕ
VR12	B-3	Ⓕ
VR13	C-2	Ⓕ
VR14	C-3	Ⓕ
Connectors		
P1	B-1	Ⓕ
P2	A-1	Ⓒ
P3	B-1	Ⓒ
P4	B-1	Ⓒ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

PRE PROCESS P.C. BOARD (VEP23278A)


PRE PROCESS P. C. BOARD
D
C
B
A
VR4
R BAL
VR204
G BAL
VR404
B BAL
TG1
1
R AD
VR2
TP3
VR3
R TRACK
VR1
R PED
TP2
G AD
2
VR202
TP203
VR201
G PED
TP202
B AD
VR402
VR403
B TRACK
VR401
TP403
B PED
3
TP402
REF. NO. 3000 SERIES
(FOIL SIDE)


D
C
B
A
VEP23278
PRE PROCESS
VJB23278
REF. NO. 3000 SERIES
PRE PROCESS
REF. NO. 3000 SERIES
JP1
JP2
JP3
JP4
JP5
JP6
JP7
JP8
1
2
3

(FOIL SIDE) (COMPONENT SIDE)

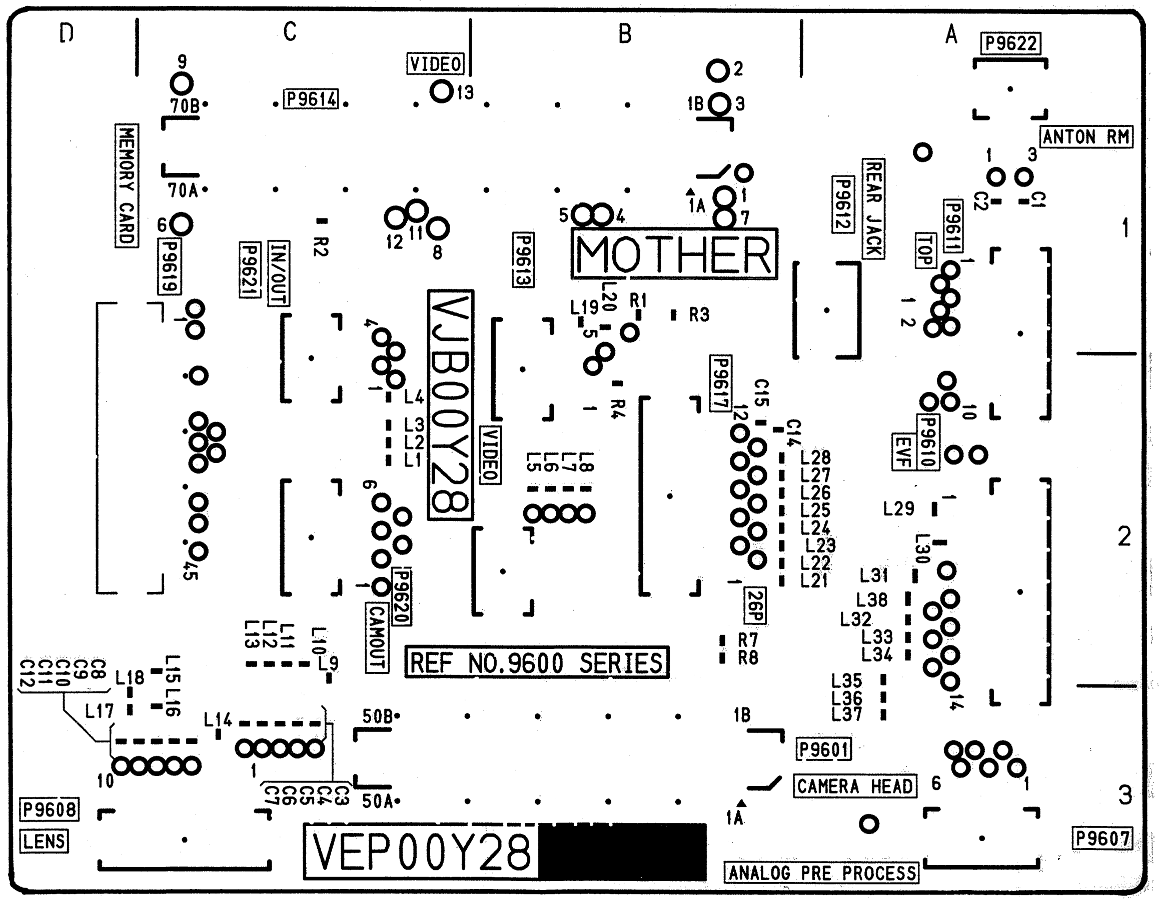
PRE PROCESS	
Transistors	
Q3001	
Q3003	D-1 Ⓕ
Q3004	C-1 Ⓕ
Q3006	C-1 Ⓕ
Q3007	C-2 Ⓒ
Q3008	C-2 Ⓕ
Q3009	C-2 Ⓒ
Q3010	C-2 Ⓒ
Q3011	C-2 Ⓒ
Q3012	C-2 Ⓕ
Q3013	C-2 Ⓕ
Q3014	C-2 Ⓕ
Q3015	C-1 Ⓕ
Q3016	B-2 Ⓕ
Q3018	C-2 Ⓕ
Q3019	B-2 Ⓕ
Q3021	B-2 Ⓕ
Q3022	A-2 Ⓕ
Q3023	A-2 Ⓕ
Q3024	A-1 Ⓒ
Q3025	A-2 Ⓕ
Q3027	A-2 Ⓕ
Q3028	A-1 Ⓒ
Q3029	A-1 Ⓕ
Q3201	D-2 Ⓕ
Q3203	D-2 Ⓕ
Q3204	C-2 Ⓕ
Q3206	C-2 Ⓕ
Q3207	C-2 Ⓒ
Q3208	C-2 Ⓕ
Q3209	C-2 Ⓒ
Q3210	C-2 Ⓒ
Q3211	C-2 Ⓒ
Q3212	C-2 Ⓕ
Q3213	C-2 Ⓕ
Q3214	C-2 Ⓕ
Q3215	C-2 Ⓕ
Q3216	B-2 Ⓕ
Q3218	C-2 Ⓕ
Q3219	B-2 Ⓕ
Q3221	B-2 Ⓕ
Q3222	A-2 Ⓕ
Q3223	A-2 Ⓒ
Q3224	A-2 Ⓒ
Q3225	A-2 Ⓕ
Q3227	A-2 Ⓕ
Q3228	A-2 Ⓒ
Q3229	A-2 Ⓕ
Q3401	D-3 Ⓕ
Q3403	D-3 Ⓕ
Q3404	C-3 Ⓕ
Q3406	C-3 Ⓕ
Q3407	C-3 Ⓒ
Q3408	C-3 Ⓕ
Q3409	C-3 Ⓒ
Q3410	C-3 Ⓒ
Q3411	C-3 Ⓒ
Q3412	C-3 Ⓕ
Q3413	C-3 Ⓕ
Q3414	C-3 Ⓕ
Q3415	C-3 Ⓕ
Q3416	B-3 Ⓕ
Q3418	C-3 Ⓕ
Q3419	B-3 Ⓕ
Q3421	B-3 Ⓕ
Q3422	A-3 Ⓕ
Q3423	A-3 Ⓒ
Q3424	A-3 Ⓒ
Q3425	A-3 Ⓕ
Q3427	A-3 Ⓕ
Q3428	A-3 Ⓒ
Q3429	A-3 Ⓕ
Q3601	D-1 Ⓕ
Q3602	C-1 Ⓕ
Q3603	A-1 Ⓕ
Q3604	A-1 Ⓕ
Q3605	C-1 Ⓕ
Integrated Circuit	
IC3001	D-2 Ⓕ
IC3002	C-1 Ⓕ
IC3003	C-1 Ⓒ
IC3004	B-2 Ⓒ
IC3005	A-2 Ⓕ
IC3006	A-2 Ⓒ
IC3201	D-2 Ⓕ
IC3202	C-2 Ⓕ
IC3203	C-2 Ⓒ
IC3204	B-2 Ⓒ
IC3205	A-2
IC3206	A-3 Ⓒ
IC3401	D-3 Ⓕ
IC3402	C-3 Ⓕ
IC3403	C-3 Ⓒ
IC3404	B-3 Ⓒ
IC3405	A-3 Ⓕ
IC3406	A-3 Ⓒ
IC3601	D-1 Ⓕ
IC3603	C-1 Ⓒ
IC3604	B-1 Ⓕ
IC3605	B-1 Ⓕ
IC3606	A-1 Ⓕ
IC3607	C-1 Ⓕ
IC3608	A-1 Ⓒ
IC3609	C-1 Ⓒ
Test Points	
TP3002	B-2 Ⓕ
TP3003	A-1 Ⓕ
TP3202	B-3 Ⓕ
TP3203	A-2 Ⓕ
TP3402	B-3 Ⓕ
TP3403	A-2 Ⓕ
TG3001	A-1 Ⓕ
Adjustments	
VR3001	A-1 Ⓕ
VR3002	A-1 Ⓕ
VR3003	A-1 Ⓕ
VR3004	B-1 Ⓕ
VR3201	A-2 Ⓕ
VR3202	A-2 Ⓕ
VR3204	B-2 Ⓕ
VR3401	A-3 Ⓕ
VR3402	A-3 Ⓕ
VR3403	A-3 Ⓕ
VR3404	B-3 Ⓕ
Connectors	
P1	C-3 Ⓒ
P2	A-1 Ⓒ
P3	C-1 Ⓒ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

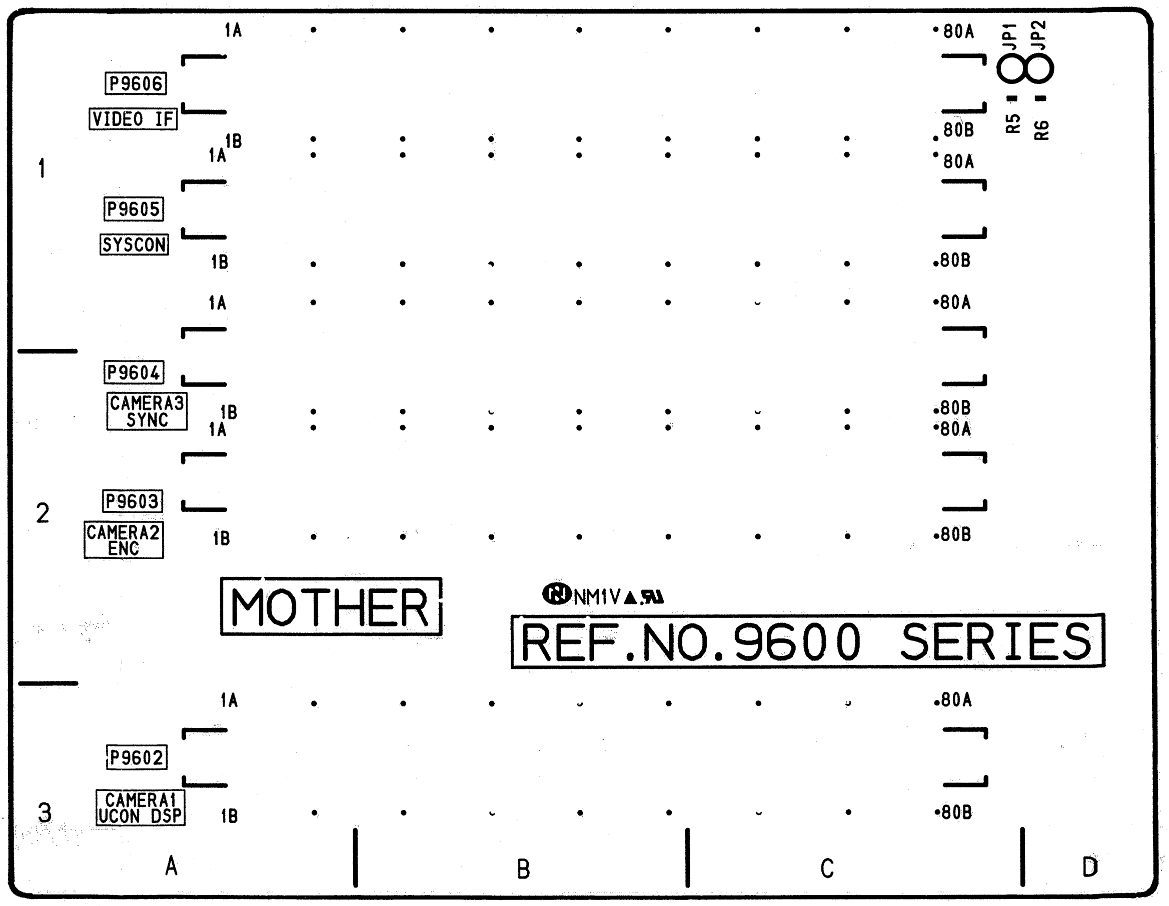
MOTHER P.C. BOARD (VEP00V89B)

MOTHER	
Connectors	
P9601	A-3 Ⓕ
P9602	A-3 Ⓒ
P9603	A-2 Ⓒ
P9604	A-2 Ⓒ
P9605	A-1 Ⓒ
P9606	A-1 Ⓒ
P9607	A-3 Ⓕ
P9608	D-3 Ⓕ
P9610	A-2 Ⓕ
P9611	A-1 Ⓕ
P9612	A-1 Ⓕ
P9613	B-1 Ⓕ
P9614	C-1 Ⓕ
P9617	B-2 Ⓕ
P9619	C-1 Ⓕ
P9620	C-2 Ⓕ
P9621	C-1 Ⓕ
P9622	A-1 Ⓕ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

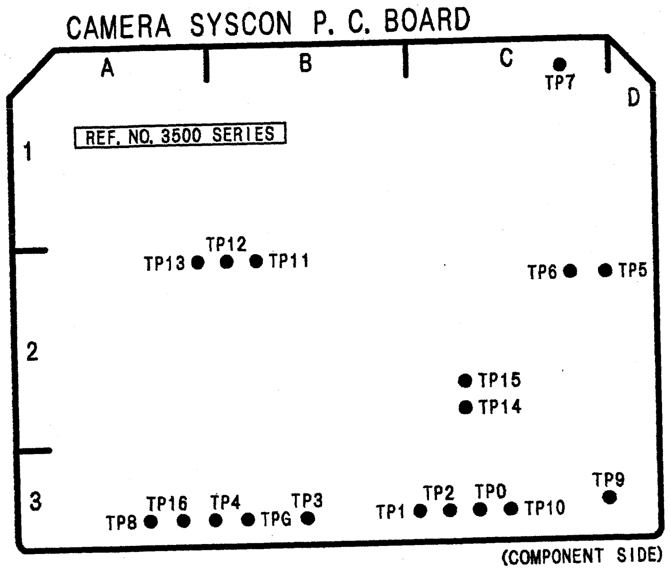

D
C
B
A
1
2
3
P9622
ANTON RM
VIDEO
P9614
MEMORY CARD
P9619
P9621
IN/OUT
P9613
MOTHER
VJB00Y28
P9612
REAR JACK
P9611
TOP
P9617
VIDEO
P9610
EVF
P9620
CAMOUT
REF NO.9600 SERIES
26P
P9601
CAMERA HEAD
P9608
LENS
VEP00Y28
ANALOG PRE PROCESS
P9607
70B
70A
50B
50A
1A
1B
R1
R2
R3
R4
R7
R8
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C14
C15
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
L20
L21
L22
L23
L24
L25
L26
L27
L28
L29
L30
L31
L32
L33
L34
L35
L36
L37
L38

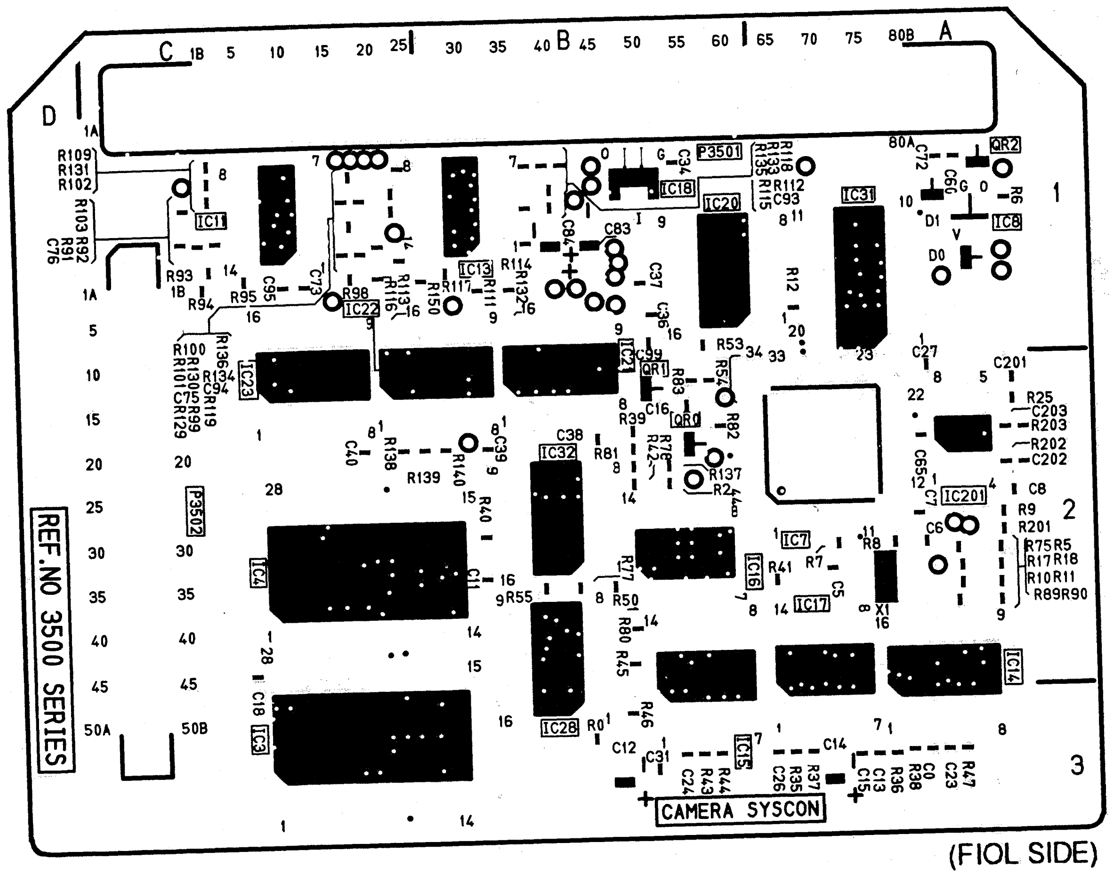
(FIOL SIDE)


1A
1B
80A
80B
JP1
JP2
R5
R6
P9606
VIDEO IF
P9605
SYSCON
P9604
CAMERA3 SYNC
P9603
CAMERA2 ENC
P9602
CAMERA1 UCON DSP
MOTHER
NM1V
REF.NO.9600 SERIES
1
2
3
A
B
C
D

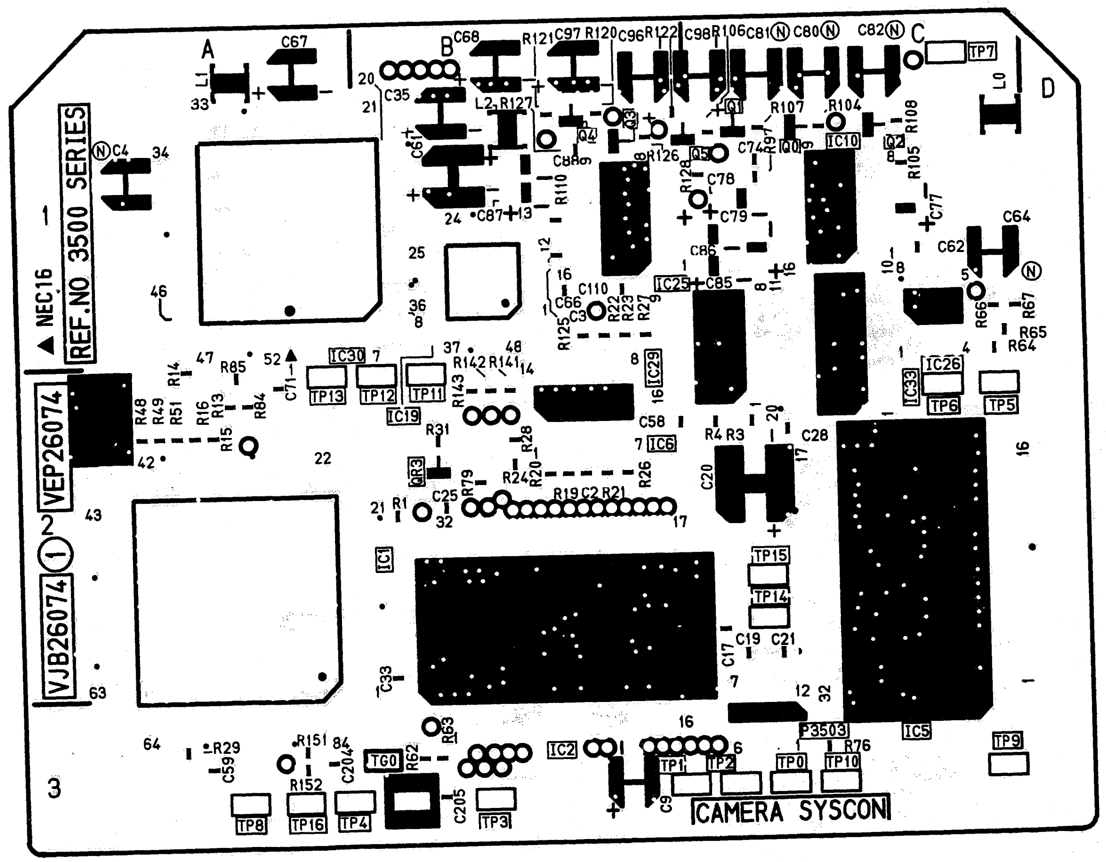
(COMPONENT SIDE)

CAMERA SYSCON P.C. BOARD (VEP26074C)


CAMERA SYSCON P. C. BOARD
A
B
C
D
1
2
3
REF. NO. 3500 SERIES
TP12
TP13
TP11
TP7
TP6
TP5
TP15
TP14
TP16
TP4
TP3
TP8
TPG
TP2
TP0
TP1
TP10
TP9
(COMPONENT SIDE)


REF.NO 3500 SERIES
CAMERA SYSCON
A
B
C
D
1
2
3
P3501
P3502
IC1
IC3
IC4
IC8
IC13
IC14
IC15
IC16
IC17
IC18
IC20
IC22
IC23
IC28
IC31
IC32
IC201
QR1
QR2

(FIOL SIDE)


VJB26074
①
VEP26074
▲ NEC16
REF.NO 3500 SERIES
CAMERA SYSCON
A
B
C
D
1
2
3
P3503
IC1
IC2
IC5
IC6
IC10
IC19
IC25
IC26
IC29
IC30
IC33
QR3
TP0
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TG0
L0
L1
L2

(COMPONENT SIDE)

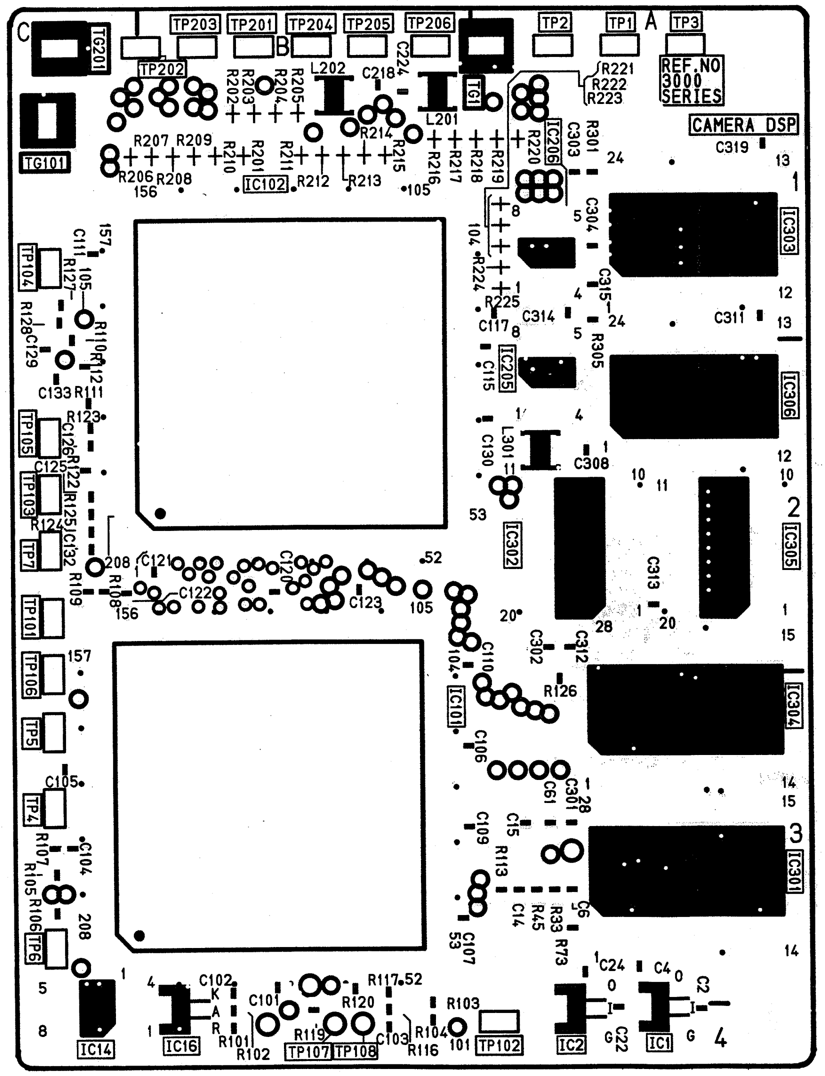
CAMERA SYSCON		
Transistors		
Q3500	C-1	ⓒ
Q3501	C-1	ⓒ
Q3502	C-1	ⓒ
Q3503	B-1	ⓒ
Q3504	B-1	ⓒ
Q3505	C-1	ⓒ
Transistor-Resistors		
QR3500	B-2	Ⓕ
QR3501	B-2	Ⓕ
QR3502	A-1	Ⓕ
QR3503	B-2	ⓒ
Integrated Circuits		
IC3201	A-2	Ⓕ
IC3501	B-2	ⓒ
IC3502	B-3	ⓒ
IC3503	C-3	Ⓕ
IC3504	C-2	Ⓕ
IC3505	C-3	ⓒ
IC3506	B-2	ⓒ
IC3507	A-2	Ⓕ
IC3508	A-1	Ⓕ
IC3510	C-1	ⓒ
IC3511	C-1	Ⓕ
IC3513	B-1	Ⓕ
IC3514	A-2	Ⓕ
IC3515	B-3	Ⓕ
IC3516	B-2	Ⓕ
IC3517	A-2	Ⓕ
IC3518	B-1	Ⓕ
IC3519	B-2	ⓒ
IC3520	B-1	Ⓕ
IC3521	B-2	Ⓕ
IC3522	B-1	Ⓕ
IC3523	C-2	Ⓕ
IC3525	B-1	ⓒ
IC3526	C-2	ⓒ
IC3528	B-3	Ⓕ
IC3529	B-2	ⓒ
IC3530	A-1	ⓒ
IC3531	A-1	Ⓕ
IC3532	B-2	Ⓕ
IC3533	C-2	ⓒ
Test Points		
TP3500	C-3	ⓒ
TP3501	B-3	ⓒ
TP3502		
TP3503	B-3	ⓒ
TP3504	A-3	ⓒ
TP3505	C-2	ⓒ
TP3506	C-2	ⓒ
TP3507	C-1	ⓒ
TP3508	A-3	ⓒ
TP3509	C-3	ⓒ
TP3510	C-3	ⓒ
TP3511	B-2	ⓒ
TP3512	B-2	ⓒ
TP3513	A-2	ⓒ
TP3514	C-2	ⓒ
TP3515	C-2	ⓒ
TP3516	A-3	ⓒ
TG3500	B-3	ⓒ
Connectors		
P3501	B-1	Ⓕ
P3502	C-2	Ⓕ
P3503	C-3	ⓒ

ADDRESS INFORMATION
ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

CAMERA DSP P.C. BOARD (VEP23275A)

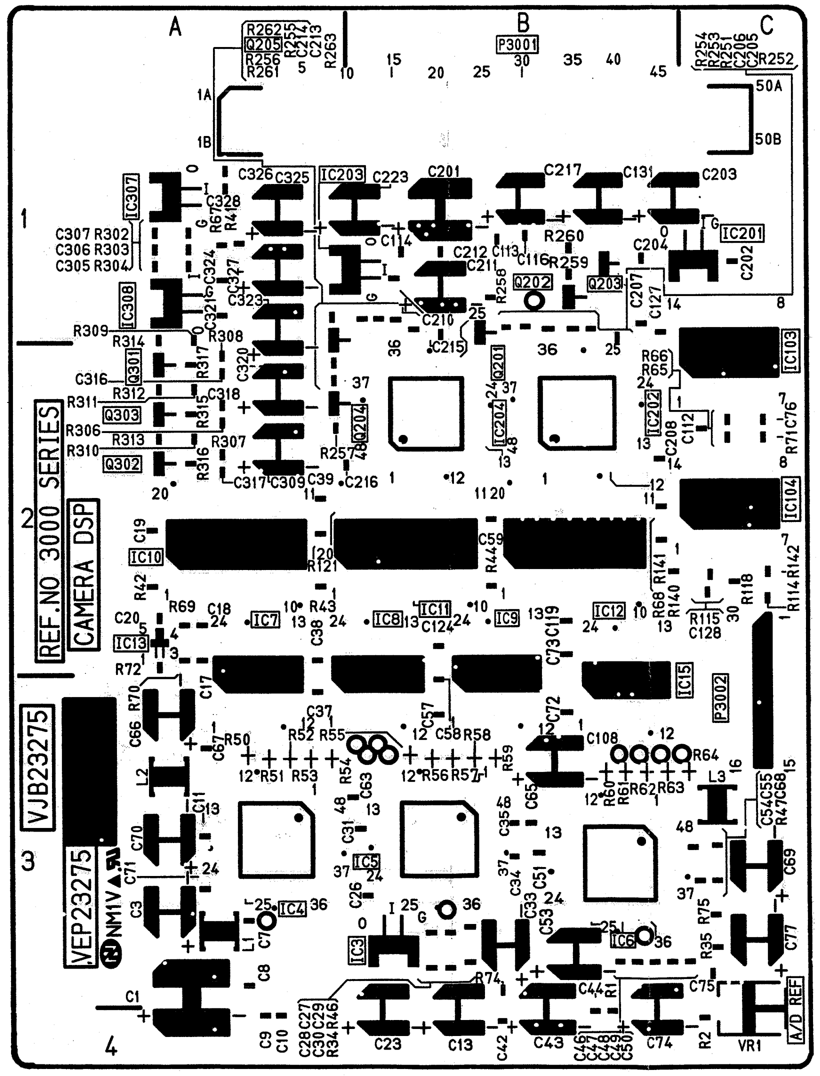
CAMERA DSP		
Transistors		
Q3201	B-2	Ⓒ
Q3202	B-1	Ⓒ
Q3203	B-1	Ⓒ
Q3204	B-2	Ⓒ
Q3205	A-1	Ⓒ
Integrated Circuits		
IC3001	A-4	Ⓕ
IC3002	A-4	Ⓕ
IC3003	B-3	Ⓒ
IC3004	A-3	Ⓒ
IC3005	B-3	Ⓒ
IC3006	B-3	Ⓒ
IC3007	A-2	Ⓒ
IC3008	B-2	Ⓒ
IC3009	B-2	Ⓒ
IC3010	A-2	Ⓒ
IC3011	B-2	Ⓒ
IC3012	B-2	Ⓒ
IC3013	A-2	Ⓒ
IC3014	C-4	Ⓕ
IC3015	C-2	Ⓒ
IC3016	B-4	Ⓕ
IC3101	B-3	Ⓕ
IC3102	B-1	Ⓕ
IC3103	C-2	Ⓒ
IC3104	C-2	Ⓒ
IC3201	C-1	Ⓒ
IC3202	B-2	Ⓒ
IC3203	B-1	Ⓒ
IC3204	B-2	Ⓒ
IC3205	A-2	Ⓕ
IC3206	A-1	Ⓕ
IC3301	A-3	Ⓕ
IC3302	A-2	Ⓕ
IC3303	A-1	Ⓕ
IC3304	A-3	Ⓕ
IC3305	A-2	Ⓕ
IC3306	A-2	Ⓕ
IC3307	A-1	Ⓒ
IC3308	A-1	Ⓒ
Test Points		
TP3001	A-1	Ⓕ
TP3002	A-1	Ⓕ
TP3003	A-1	Ⓕ
TP3004	C-3	Ⓕ
TP3005	C-3	Ⓕ
TP3006	C-3	Ⓕ
TP3007	C-2	Ⓕ
TP3101	C-2	Ⓕ
TP3102	A-4	Ⓕ
TP3103	C-3	Ⓕ
TP3104	C-1	Ⓕ
TP3105	C-2	Ⓕ
TP3106	B-4	Ⓕ
TP3107	C-3	Ⓕ
TP3108	B-4	Ⓕ
TP3201	B-1	Ⓕ
TP3202	B-1	Ⓕ
TP3203	B-1	Ⓕ
TP3204	B-1	Ⓕ
TP3205	B-1	Ⓕ
TP3206	B-1	Ⓕ
TG3001	A-1	Ⓕ
TG3101	C-1	Ⓕ
TG3201	C-1	Ⓕ
Adjustments		
VR3001	C-4	Ⓒ
Connectors		
P3001	B-1	Ⓒ
P3002	C-3	Ⓒ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE



A
B
C
TP203
TP201
TP204
TP205
TP206
TP2
TP1
TP3
TP202
TG201
TG1
TG101
REF. NO 3000 SERIES
CAMERA DSP
IC303
IC306
IC305
IC304
IC301
IC302
IC205
IC206
IC101
IC102
IC1
IC2
IC14
IC16
TP104
TP105
TP103
TP7
TP101
TP106
TP5
TP4
TP6
TP107
TP108
TP102
1
2
3

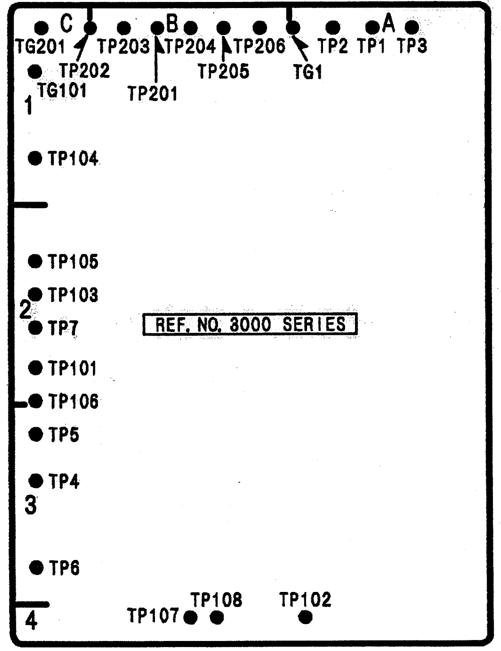
(FIOL SIDE)



A
B
C
P3001
REF. NO 3000 SERIES
CAMERA DSP
VJB23275
VEP23275
IC307
IC308
IC301
IC303
IC302
IC203
IC201
IC202
IC204
IC103
IC104
IC10
IC13
IC7
IC8
IC11
IC9
IC12
IC15
IC4
IC5
IC3
IC6
P3002
A/D REF
VR1
Q201
Q202
Q203
Q204
Q205
1
2
3
4

(COMPONENT SIDE)

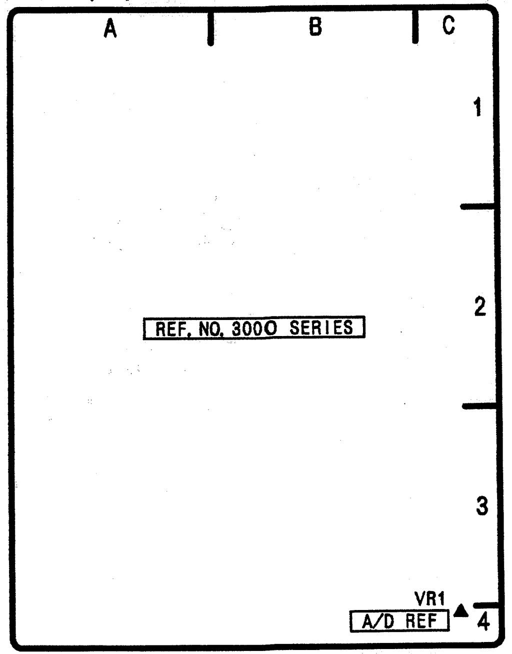
DSP P. C. BOARD



C
B
A
TG201
TP203
TP204
TP206
TP2
TP1
TP3
TP202
TP205
TG1
TG101
TP201
TP104
TP105
TP103
TP7
TP101
TP106
TP5
TP4
TP6
TP107
TP108
TP102
REF. NO. 3000 SERIES
1
2
3
4

(FOIL SIDE)

DSP P. C. BOARD

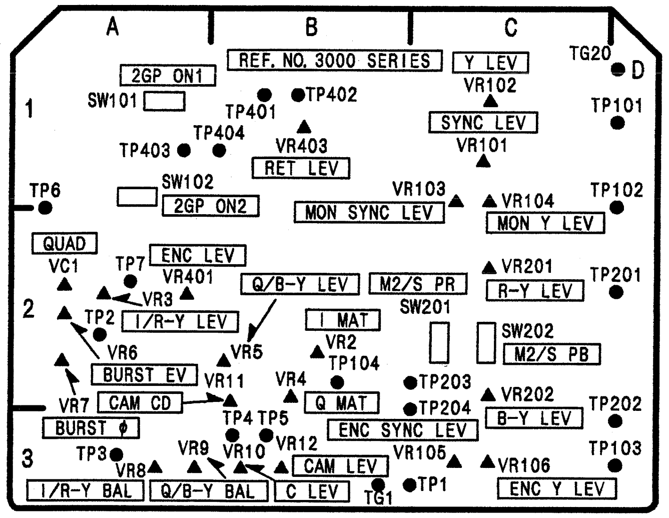


A
B
C
REF. NO. 3000 SERIES
VR1
A/D REF
1
2
3
4

(COMPONENT SIDE)

CAMERA ENCODER P.C. BOARD (VEP23276B)

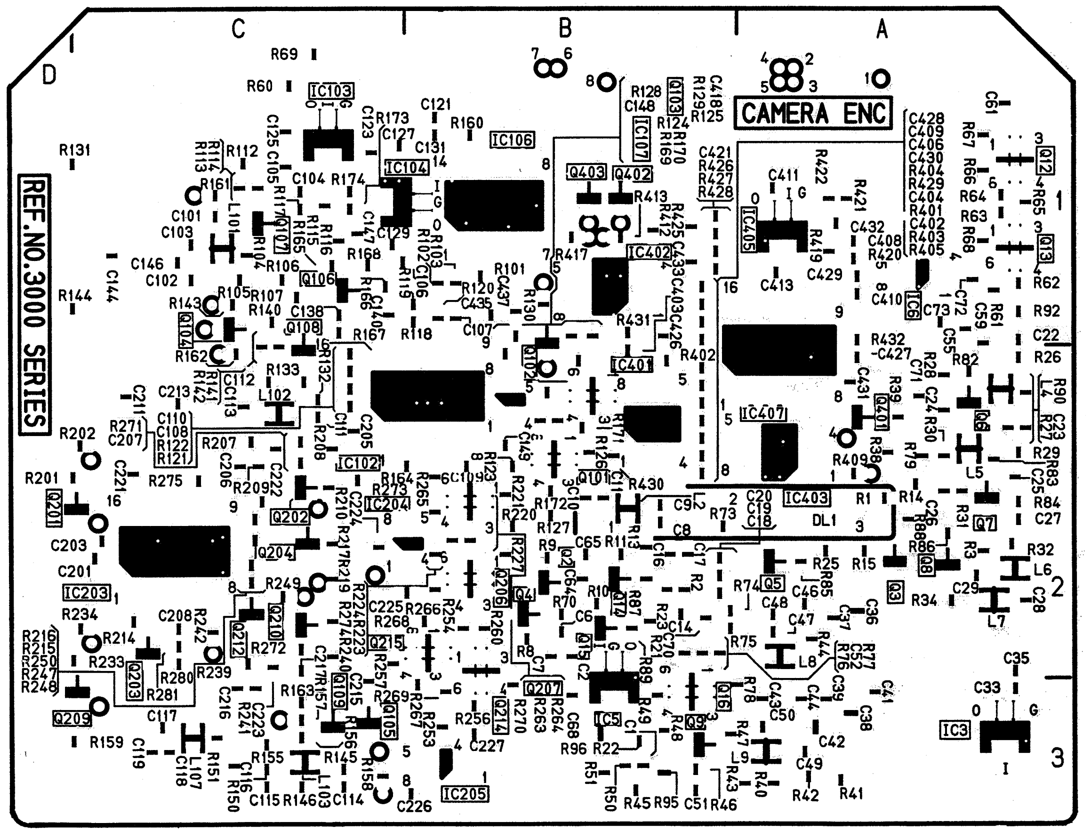
CAMERA ENCODER P. C. BOARD


A
B
C
D
1
2
3
2GP ON1
SW101
REF. NO. 3000 SERIES
Y LEV
TG201
VR102
TP101
TP401
TP402
TP404
SYNC LEV
VR101
TP403
VR403
RET LEV
TP6
SW102
2GP ON2
VR103
MON SYNC LEV
VR104
MON Y LEV
TP102
QUAD
VC1
TP7
ENC LEV
VR401
VR3
Q/B-Y LEV
M2/S PR
VR201
R-Y LEV
TP201
SW201
TP2
I/R-Y LEV
I MAT
VR2
SW202
M2/S PB
VR6
VR5
TP104
BURST EV
VR11
VR4
TP203
VR202
VR7
CAM CD
Q MAT
TP204
B-Y LEV
TP202
BURST ϕ
TP4
TP5
ENC SYNC LEV
TP3
VR8
VR9
VR10
VR12
VR105
TP103
CAM LEV
VR106
I/R-Y BAL
Q/B-Y BAL
C LEV
TG1
TP1
ENC Y LEV

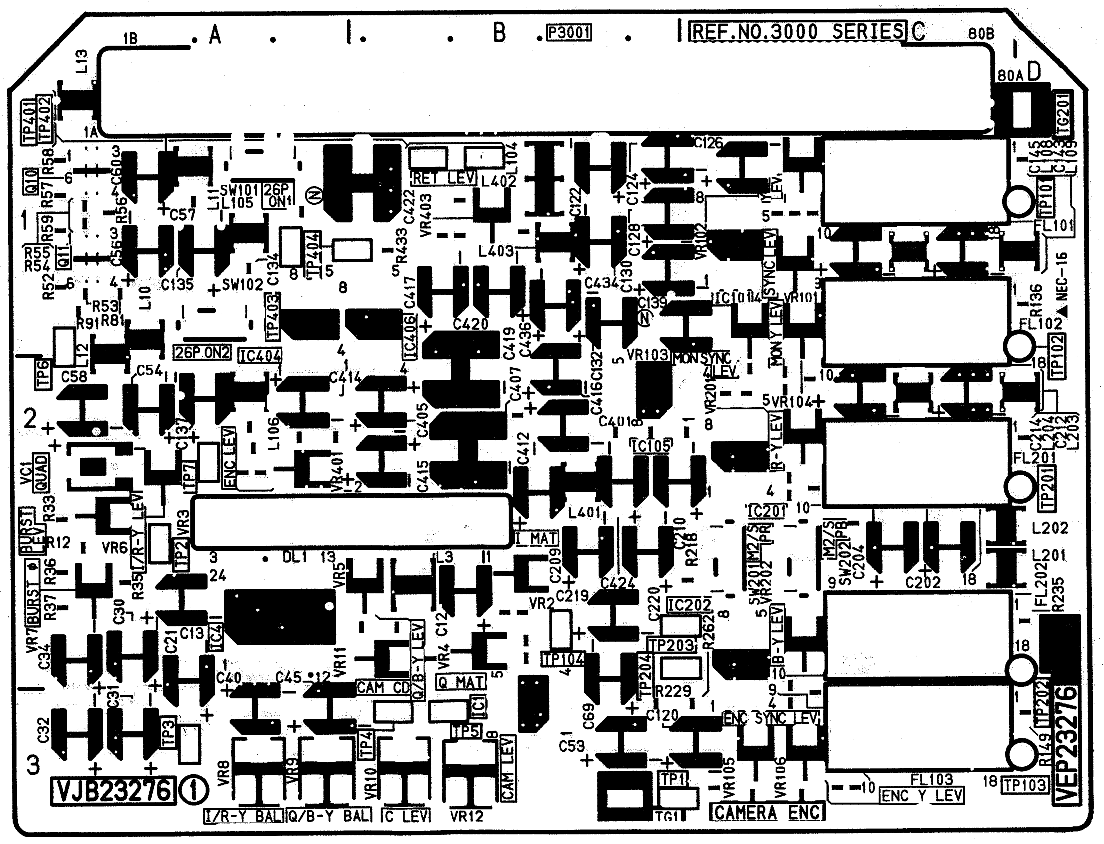
(COMPONENT SIDE)

CAMERA ENCODER		
Transistors		
Q3003	A-2	Ⓕ
Q3005	A-2	Ⓕ
Q3006	A-2	Ⓕ
Q3008	A-2	Ⓕ
Q3009	B-3	Ⓕ
Q3010	A-1	©
Q3011	A-1	©
Q3012	A-1	Ⓕ
Q3013	A-1	Ⓕ
Q3014	B-2	Ⓕ
Q3015	B-2	Ⓕ
Q3016	B-3	Ⓕ
Q3101	B-2	Ⓕ
Q3102	B-2	Ⓕ
Q3103	B-1	Ⓕ
Q3104	C-1	Ⓕ
Q3105	C-3	Ⓕ
Q3106	C-1	Ⓕ
Q3107	C-1	Ⓕ
Q3108	C-1	Ⓕ
Q3109	C-3	Ⓕ
Q3201	D-2	Ⓕ
Q3202	C-2	Ⓕ
Q3203	C-3	©
Q3204	C-2	Ⓕ
Q3206	B-2	Ⓕ
Q3207	B-3	Ⓕ
Q3209	D-3	Ⓕ
Q3210	C-2	Ⓕ
Q3212	C-2	Ⓕ
Q3214	B-3	Ⓕ
Q3215	C-2	Ⓕ
Q3401	A-2	Ⓕ
Q3402	B-1	Ⓕ
Q3403	B-1	Ⓕ
Integrated Circuits		
IC3001	B-3	©
IC3003	A-3	Ⓕ
IC3004	A-2	©
IC3005	B-3	Ⓕ
IC3006	A-1	Ⓕ
IC3101	C-1	©
IC3102	C-2	Ⓕ
IC3103	C-1	Ⓕ
IC3104	C-1	Ⓕ
IC3105	B-2	©
IC3106	B-1	Ⓕ
IC3107	B-1	Ⓕ
IC3201	C-2	©
IC3202	B-2	©
IC3203	C-2	Ⓕ
IC3204	C-2	Ⓕ
IC3205	B-3	Ⓕ
IC3401	B-2	Ⓕ
IC3402	B-1	Ⓕ
IC3403	A-2	Ⓕ
IC3404	A-1	©
IC3405	A-1	Ⓕ
IC3406	B-1	©
Test Points		
TP3001	B-3	©
TP3002	A-2	©
TP3003	A-3	©
TP3004	B-3	©
TP3005	B-3	©
TP3006	A-2	©
TP3007	A-2	©
TP3101	A-2	©
TP3102	A-3	©
TP3103	D-3	©
TP3104	B-2	©
TP3105	D-1	©
TP3106	A-2	©
TP3201	D-2	©
TP3202	D-3	©
TP3203	B-2	©
TP3401	A-1	©
TP3402	A-1	©
TP3403	A-1	©
TP3404	A-1	©
TG3001	B-3	©
TG3201	D-1	©
Adjustments		
VC3001	A-2	©
VR3003	A-2	©
VR3005	A-2	©
VR3006	A-2	©
VR3008	A-3	©
VR3009	A-3	©
VR3010	B-3	©
VR3011	A-2	©
VR3012	B-3	©
VR3101	C-1	©
VR3102	A-2	©
VR3103	B-1	©
VR3104	B-2	©
VR3105	C-3	©
VR3106	C-3	©
VR3201	C-2	©
VR3202	C-2	©
VR3401	A-2	©
VR3403	B-1	©
Switches		
SW3101	A-1	©
SW3102	A-1	©
SW3201	C-2	©
SW3202	C-2	©
Connectors		
P3001	B-1	©

ADDRESS INFORMATION
©... COMPONENT SIDE
Ⓕ... FOIL SIDE


D
C
B
A
1
2
3
REF.NO.3000 SERIES
CAMERA ENC

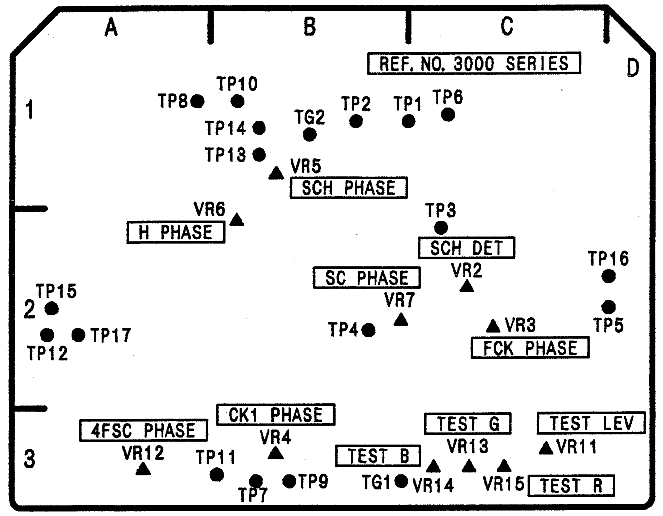
(FOIL SIDE)


A
B
C
D
1
2
3
REF.NO.3000 SERIES
P3001
VJB23276①
VEP23276
CAMERA ENC

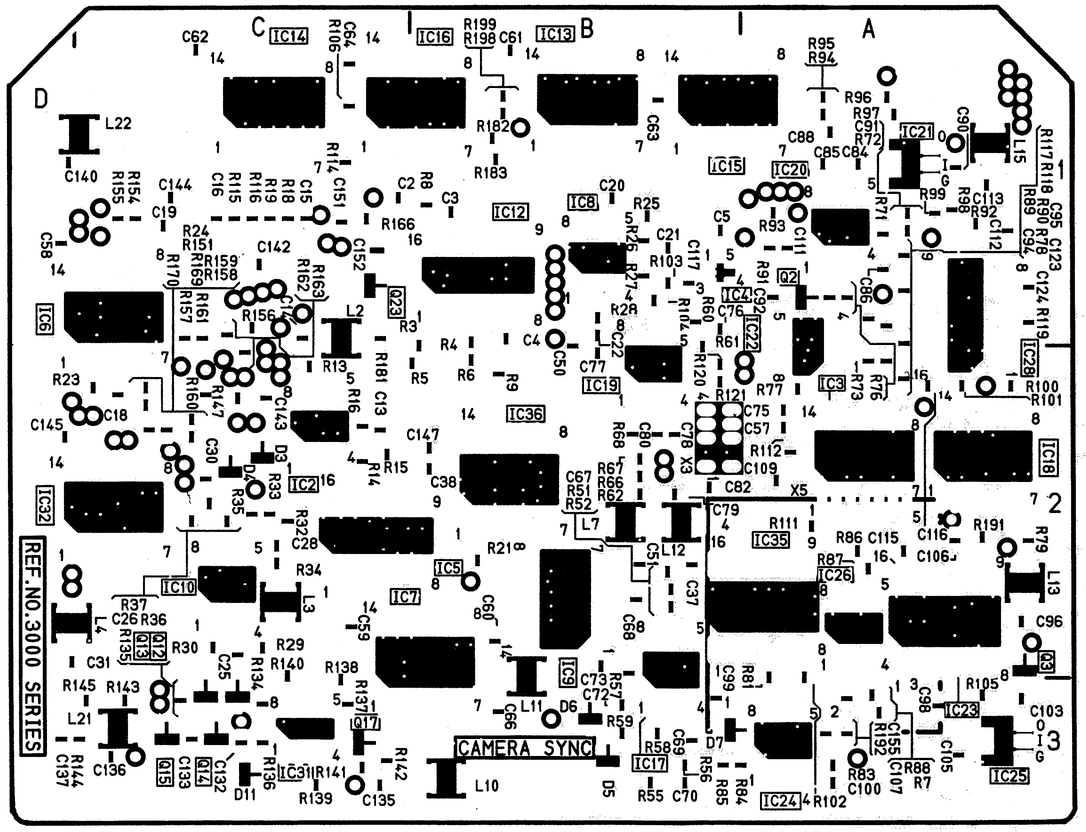
(COMPONENT SIDE)

CAMERA SYNC P.C. BOARD (VEP23277B) FOR EN MODEL
(VEP23277C) FOR E MODEL

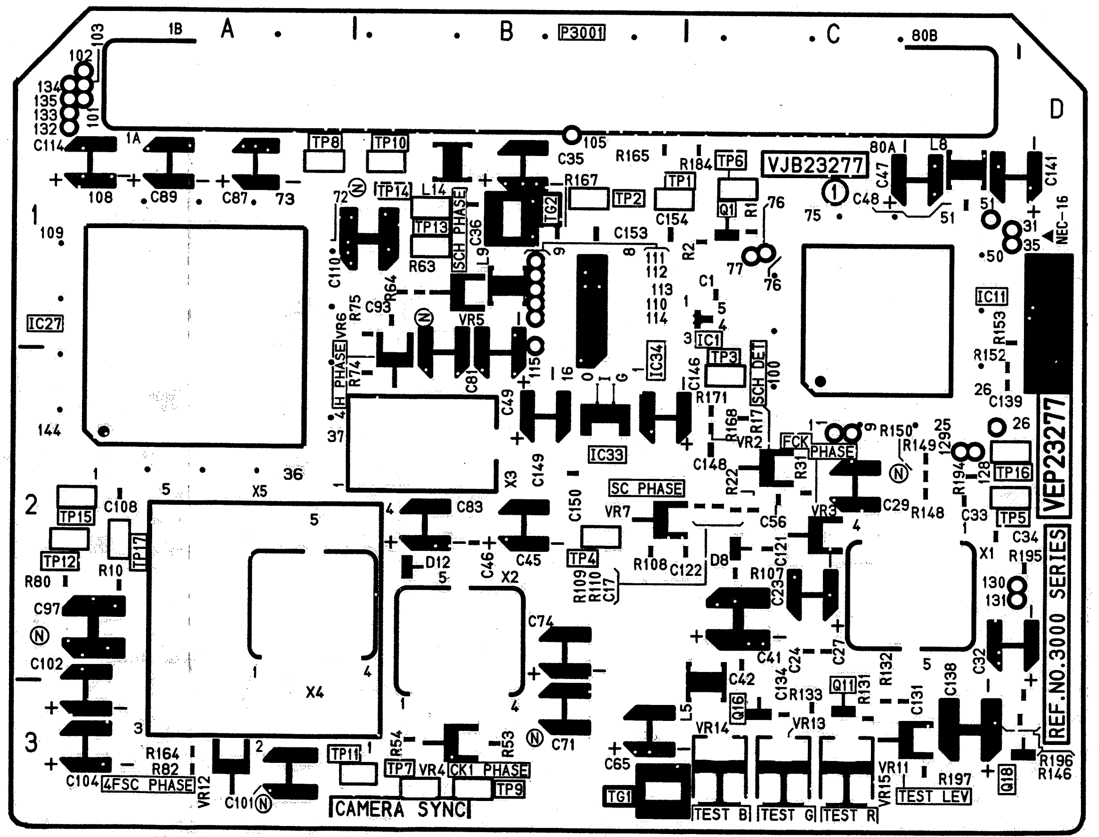
CAMERA SYNC P. C. BOARD


A
B
C
D
1
2
3
REF. NO. 3000 SERIES
TP10
TP8
TP14
TP13
TG2
TP2
TP1
TP6
VR5
SCH PHASE
VR6
H PHASE
TP3
SCH DET
SC PHASE
VR2
TP16
VR7
TP15
TP17
TP12
TP4
VR3
TP5
FCK PHASE
4FSC PHASE
CK1 PHASE
VR4
TEST G
TEST LEV
VR12
TP11
TP7
TP9
TEST B
TG1
VR14
VR13
VR15
VR11
TEST R

(COMPONENT SIDE)



(FIOL SIDE)

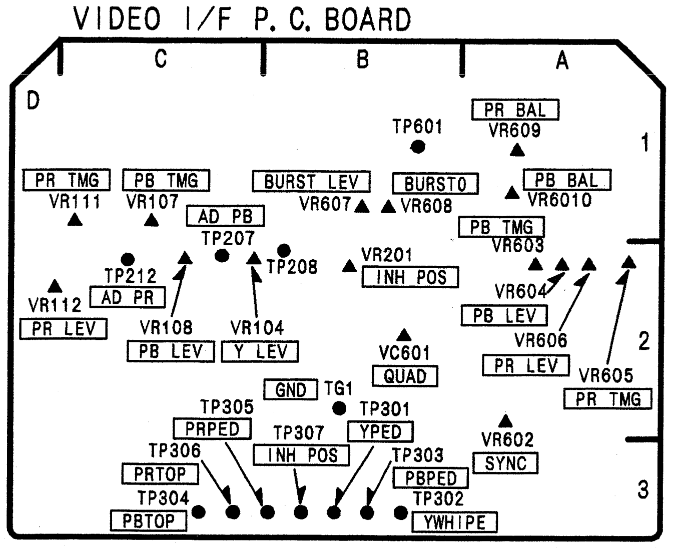


(COMPONENT SIDE)

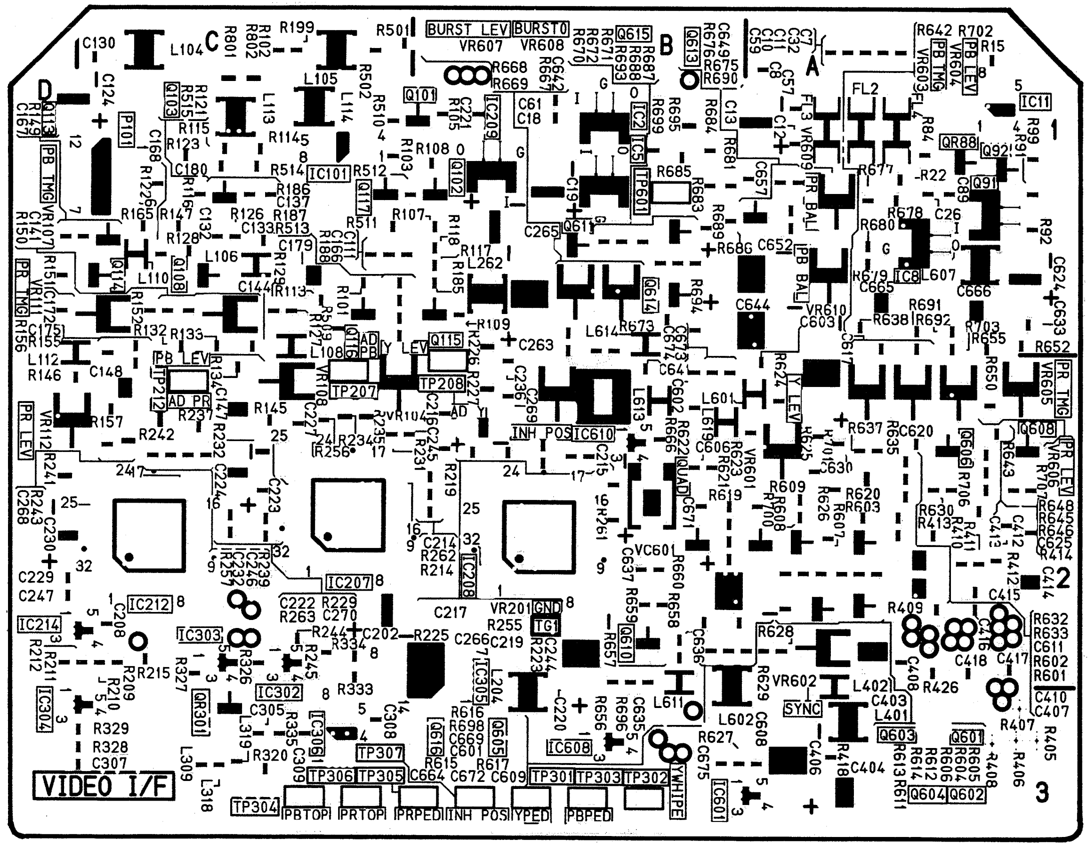
CAMERA SYNC		
Transistors		
Q3001	C-1	Ⓒ
Q3002	A-1	Ⓕ
Q3003	A-2	Ⓕ
Q3011	C-1	Ⓒ
Q3012	C-2	Ⓕ
Q3013	C-2	Ⓕ
Q3014	C-3	Ⓕ
Q3015	C-3	Ⓕ
Q3016	C-3	Ⓒ
Q3017	C-3	Ⓕ
Q3018	C-3	Ⓒ
Q3023	C-1	Ⓕ
Integrated Circuits		
IC3002	C-2	Ⓕ
IC3003	A-2	Ⓕ
IC3005	B-2	Ⓕ
IC3006	D-1	Ⓕ
IC3007	C-2	Ⓕ
IC3008	B-1	Ⓕ
IC3009	B-3	Ⓕ
IC3010	C-2	Ⓕ
IC3011	C-2	Ⓒ
IC3013	B-1	Ⓕ
IC3014	C-1	Ⓕ
IC3015	B-1	Ⓕ
IC3016	B-1	Ⓕ
IC3017	B-3	Ⓕ
IC3018	A-2	Ⓕ
IC3019	B-2	Ⓕ
IC3020	A-1	Ⓕ
IC3021	A-1	Ⓕ
IC3022	A-1	Ⓕ
IC3023	A-3	Ⓕ
IC3024	A-3	Ⓕ
IC3025	A-3	Ⓕ
IC3027	A-1	Ⓒ
IC3028	A-2	Ⓕ
IC3031	C-3	Ⓕ
IC3032	D-2	Ⓕ
IC3033	B-2	Ⓒ
IC3034	B-1	Ⓒ
IC3035	A-2	Ⓕ
IC3036	B-2	Ⓕ
Test Points		
TP3001	B-1	Ⓒ
TP3002	B-1	Ⓒ
TP3003	C-1	Ⓒ
TP3004	B-2	Ⓒ
TP3005	C-2	Ⓒ
TP3006	C-1	Ⓒ
TP3007	B-3	Ⓒ
TP3008	A-1	Ⓒ
TP3009	B-3	Ⓒ
TP3010	B-2	Ⓒ
TP3011	A-3	Ⓒ
TP3012	A-2	Ⓒ
TP3013	B-2	Ⓒ
TP3014	B-2	Ⓒ
TP3015	A-2	Ⓒ
TP3016	C-2	Ⓒ
TP3017	A-2	Ⓒ
TG3001	B-3	Ⓒ
TG3002	B-2	Ⓒ
Adjustments		
VR3002	C-2	Ⓒ
VR3005	B-1	Ⓒ
VR3006	A-1	Ⓒ
VR3007	B-2	Ⓒ
VR3011	C-3	Ⓒ
VR3012	A-3	Ⓒ
VR3013	C-3	Ⓒ
VR3014	C-3	Ⓒ
VR3015	C-3	Ⓒ
Connectors		
P3001	B-1	Ⓒ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

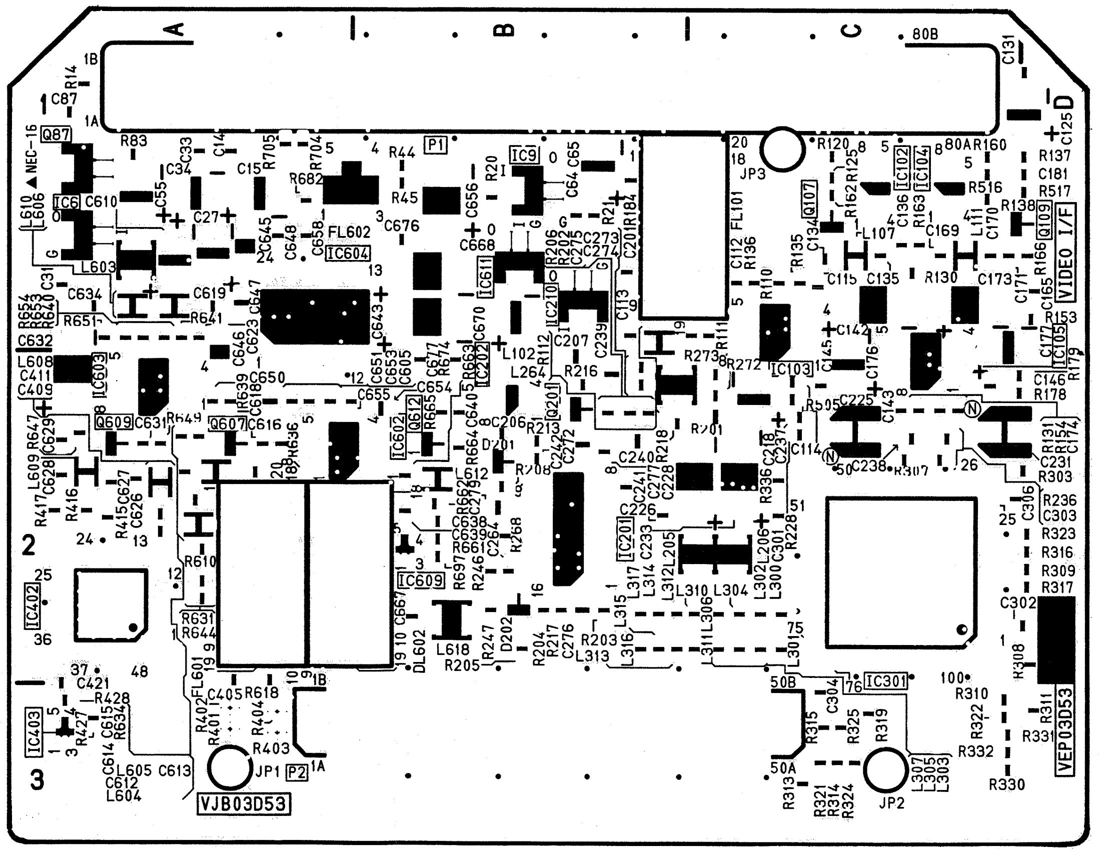
VIDEO I/F P.C. BOARD (VEP03D53A)


VIDEO I/F P. C. BOARD
C
B
A
D
1
2
3
TP601
PR BAL
VR609
PR TMG
VR111
PB TMG
VR107
BURST LEV
VR607
BURSTO
VR608
PB BAL
VR6010
AD PB
TP207
TP208
PB TMG
VR603
TP212
AD PR
VR112
PR LEV
VR108
PB LEV
VR104
Y LEV
VR201
INH POS
VR604
PB LEV
VR606
PR LEV
VR605
PR TMG
VC601
QUAD
GND
TG1
TP305
PRPED
TP301
TP307
YPED
VR602
SYNC
TP306
PRTOP
INH POS
TP303
PBPED
TP304
PBTOP
TP302
YWHIPE

(FOIL SIDE)


VIDEO I/F
BURST LEV
BURSTO
PB TMG
PR TMG
PR LEV
PB LEV
PR BAL
PB BAL
AD PR
AD PB
Y LEV
INH POS
QUAD
SYNC
YWHIPE
PBTOP
PRTOP
PRPED
YPED
PBPED
A
B
C
D
1
2
3

(FOIL SIDE)

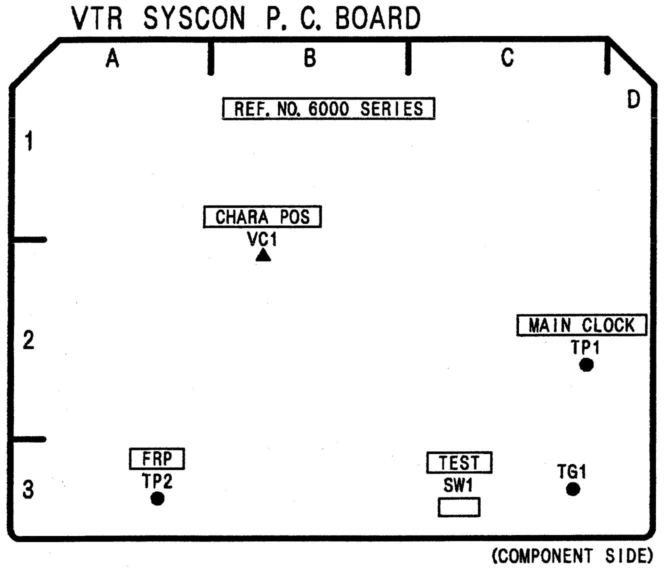

VIDEO I/F
VEP03D53
VJB03D53
A
B
C
D
1
2
3
JP1
JP2
JP3

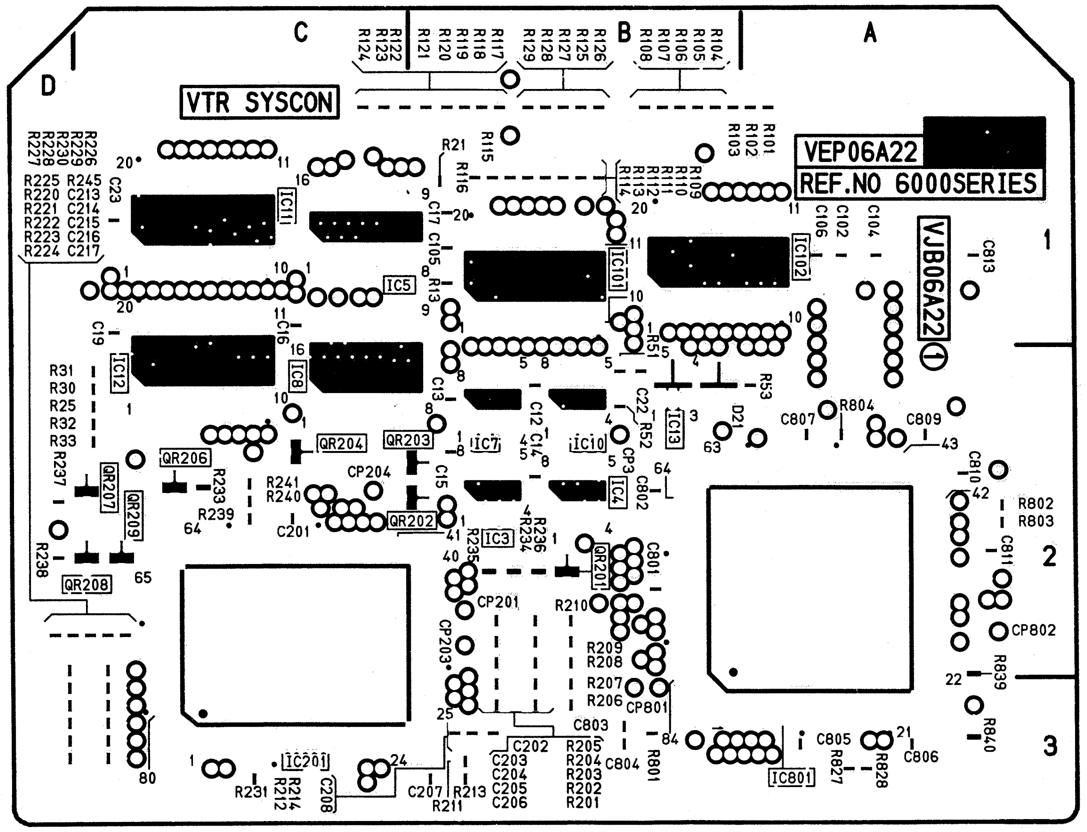
(COMPONENT SIDE)

VIDEO I/F		
Transistors		
Q1	D-1	Ⓕ
Q3	C-1	Ⓕ
Q4	C-1	Ⓕ
Q5	C-2	Ⓕ
Q6	C-2	Ⓕ
Q87	A-1	Ⓒ
Q88	A-1	Ⓒ
Q89	A-1	Ⓒ
Q90	A-1	Ⓒ
Q91	A-1	Ⓕ
Q92	A-1	Ⓕ
Q93	A-1	Ⓒ
Q101	B-1	Ⓕ
Q102	B-1	Ⓕ
Q103	C-1	Ⓕ
Q104	B-2	Ⓒ
Q105	B-3	Ⓕ
Q106	B-2	Ⓕ
Q107	C-1	Ⓒ
Q108	C-1	Ⓕ
Q109	D-1	Ⓒ
Q110	C-3	Ⓕ
Q111	B-3	Ⓕ
Q112	B-3	Ⓕ
Q113	B-3	Ⓕ
Q114	B-2	Ⓕ
Q115	B-2	Ⓕ
Q116	C-1	Ⓕ
Q117	C-1	Ⓕ
Q201	B-2	Ⓒ
Q601	A-3	Ⓕ
Q603	A-3	Ⓕ
Q604	B-1	Ⓒ
Q605	B-3	Ⓕ
Q607	A-2	Ⓒ
Q608	A-2	Ⓕ
Q609	A-2	Ⓒ
Q610	B-2	Ⓕ
Q612	B-2	Ⓒ
Q613	B-1	Ⓕ
Q614	B-1	Ⓕ
Q615	B-1	Ⓕ
Q616	B-3	Ⓕ
Transistor-Resistors		
QR88	A-1	Ⓕ
QR89	A-1	Ⓕ
QR90	A-1	Ⓒ
QR301	C-3	Ⓕ
Integrated Circuits		
IC1	C-2	Ⓒ
IC2	B-1	Ⓕ
IC4	C-2	Ⓕ
IC5	B-1	Ⓕ
IC6	A-1	Ⓒ
IC7	B-1	Ⓕ
IC8	A-1	Ⓕ
IC9	B-1	Ⓒ
IC10	B-2	Ⓕ
IC11	A-1	Ⓕ
IC101	C-1	Ⓕ
IC102	C-1	Ⓒ
IC103	C-2	Ⓒ
IC104	C-1	Ⓒ
IC105	D-1	Ⓒ
IC106	B-3	Ⓒ
IC201	B-2	Ⓒ
IC202	B-2	Ⓒ
IC203	B-1	Ⓕ
IC204	A-1	Ⓕ
IC205	B-1	Ⓕ
IC207	C-2	Ⓕ
IC208	B-2	Ⓕ
IC209	B-1	Ⓕ
IC210	B-1	Ⓒ
IC211	B-1	Ⓕ
IC212	C-2	Ⓕ
IC214	D-2	Ⓕ
IC301	C-3	Ⓒ
IC302	C-3	Ⓕ
IC303	C-3	Ⓕ
IC304	D-3	Ⓕ
IC306	C-3	Ⓕ
IC402	A-2	Ⓒ
IC403	A-3	Ⓒ
IC601	B-3	Ⓕ
IC602	B-2	Ⓒ
IC608	B-3	Ⓕ
IC609	B-2	Ⓒ
IC610	B-2	Ⓕ
IC611	B-1	Ⓒ
Test Points		
TP207	C-2	Ⓕ
TP208	B-2	Ⓕ
TP212	C-2	Ⓕ
TP301	B-3	Ⓕ
TP302	B-3	Ⓕ
TP303	B-3	Ⓕ
TP304	C-3	Ⓕ
TP305	C-3	Ⓕ
TP306	C-3	Ⓕ
TP307	C-3	Ⓕ
TP601	B-1	Ⓕ
TG1	B-2	Ⓕ
Adjustments		
VR1	C-1	Ⓒ
VR2	C-1	Ⓒ
VR104	B-2	Ⓒ
VR105	C-3	Ⓒ
VR107	D-1	Ⓕ
VR108	C-2	Ⓕ
VR111	D-1	Ⓕ
VR112	D-2	Ⓕ
VR201	B-2	Ⓕ
VR601	A-2	Ⓕ
VR602	A-3	Ⓕ
VR603	A-1	Ⓕ
VR604	A-1	Ⓕ
VR605	A-2	Ⓕ
VR606	A-2	Ⓕ
VR607	B-1	Ⓕ
VR608	B-1	Ⓕ
VR609	A-1	Ⓕ
VR610	A-1	Ⓕ
VR611	B-1	Ⓕ
VC601	B-2	Ⓕ
Connectors		
P1	B-1	Ⓒ
P2	A-3	Ⓒ
P101	C-1	Ⓕ

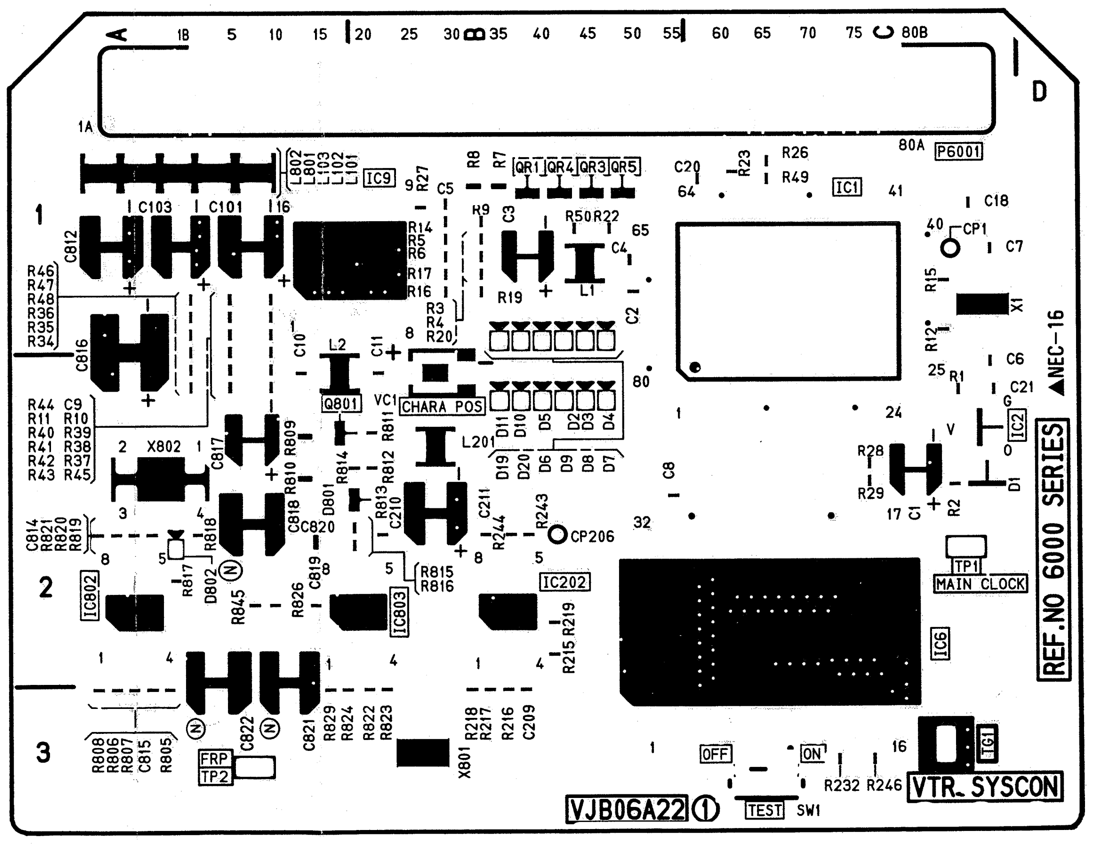
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

VTR SYSCON P.C. BOARD (VEP06A22B)


VTR SYSCON P. C. BOARD
A
B
C
D
1
2
3
REF. NO. 6000 SERIES
CHARA POS
VC1
MAIN CLOCK
TP1
FRP
TP2
TEST
SW1
TG1
(COMPONENT SIDE)


VTR SYSCON
VEP06A22
REF.NO 6000SERIES
VJB06A22①
C
B
A
D
1
2
3

(FOIL SIDE)

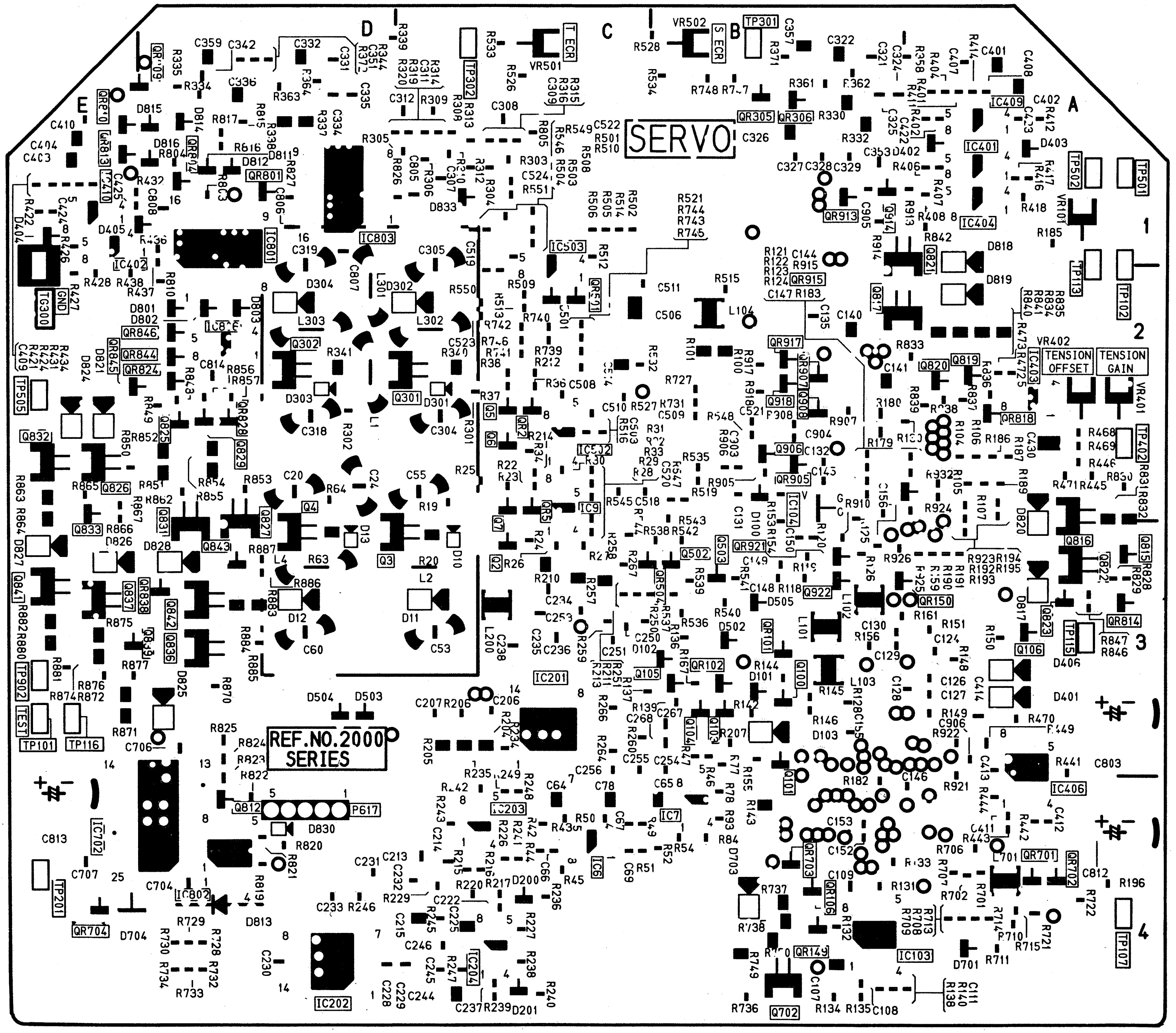

A
B
C
D
1
2
3
CHARA POS
MAIN CLOCK
TP1
FRP
TP2
TEST
SW1
OFF
ON
▲NEC-16
REF.NO 6000 SERIES
VJB06A22①
VTR. SYSCON
P6001

(COMPONENT SIDE)

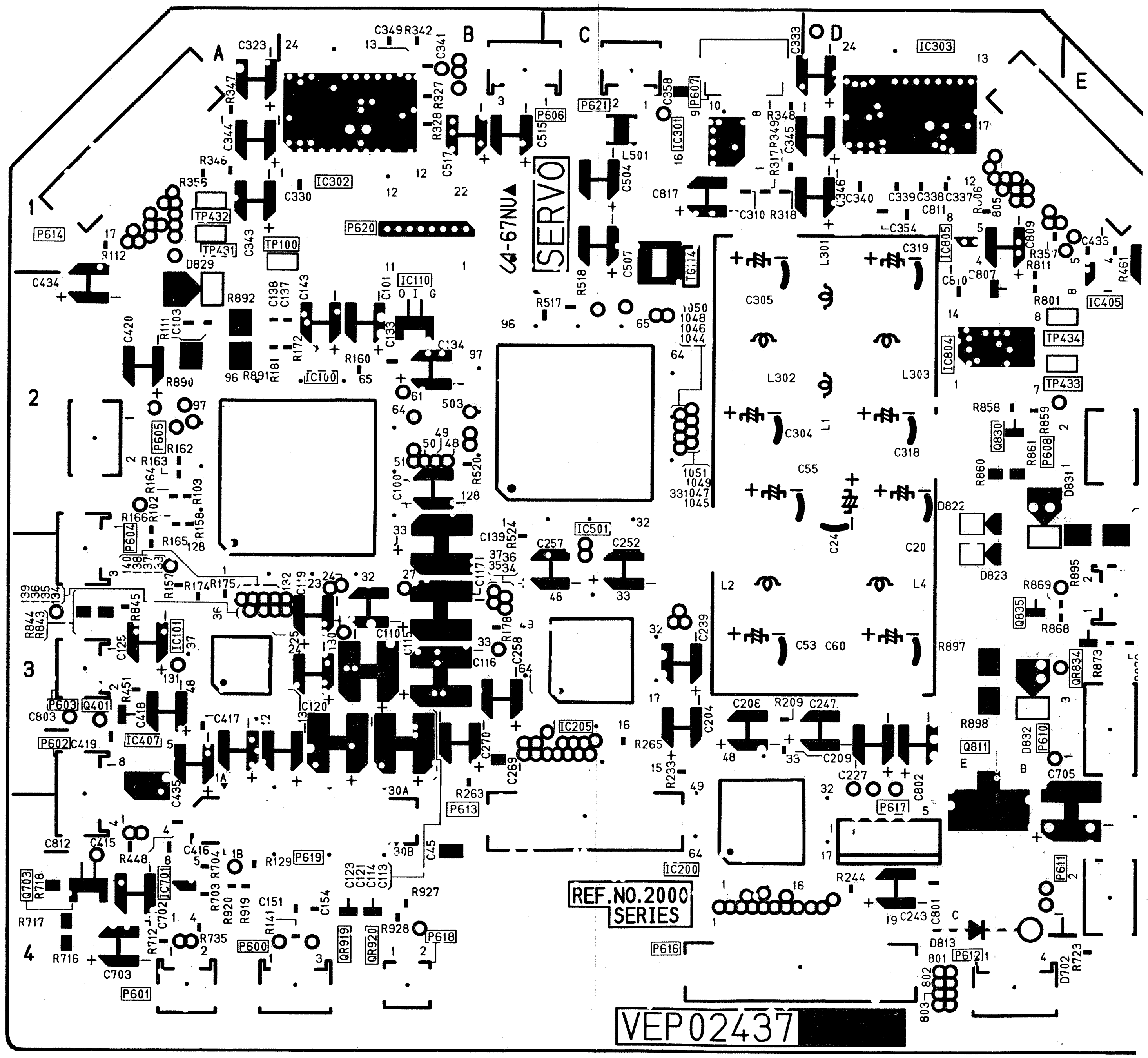
VTR SYSCON		
Transistors		
Q6801	A-2	Ⓒ
Transistor-Resistors		
QR6001	B-1	Ⓒ
QR6003	B-1	Ⓒ
QR6004	B-1	Ⓒ
QR6005	B-1	Ⓒ
QR6201	B-2	Ⓕ
QR6202	B-2	Ⓕ
QR6203	B-2	Ⓕ
QR6204	C-2	Ⓕ
QR6206	C-2	Ⓕ
QR6207	C-2	Ⓕ
QR6208	C-2	Ⓕ
QR6209	C-2	Ⓕ
Integrated Circuits		
IC6001	C-1	Ⓒ
IC6002	D-2	Ⓒ
IC6003	B-2	Ⓕ
IC6004	B-2	Ⓕ
IC6005	C-1	Ⓕ
IC6006	C-2	Ⓒ
IC6007	B-2	Ⓕ
IC6008	C-2	Ⓕ
IC6009	B-1	Ⓒ
IC6010	B-2	Ⓕ
IC6011	C-1	Ⓕ
IC6012	C-2	Ⓕ
IC6013	B-2	Ⓕ
IC6101	B-1	Ⓕ
IC6102	A-1	Ⓕ
IC6201	C-3	Ⓕ
IC6202	B-2	Ⓒ
IC6801	A-3	Ⓕ
IC6802	B-2	Ⓒ
IC6803	B-2	Ⓒ
Test Points		
TP6001	C-2	Ⓒ
TP6002	A-3	Ⓒ
TG6001	C-3	Ⓒ
Adjustments		
VC6001	B-2	Ⓒ
Switches		
SW6001	C-3	Ⓒ
Connectors		
P6001	C-1	Ⓒ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

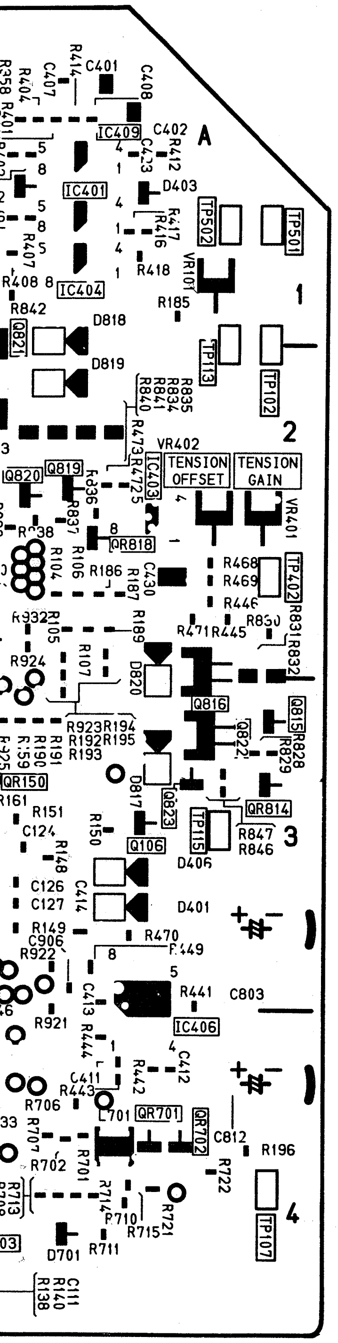
SERVO P.C. BOARD (VEP02437B)


SERVO
REF.NO.2000
SERIES
TENSION OFFSET
TENSION GAIN
A
B
C
D
E
1
2
3
4

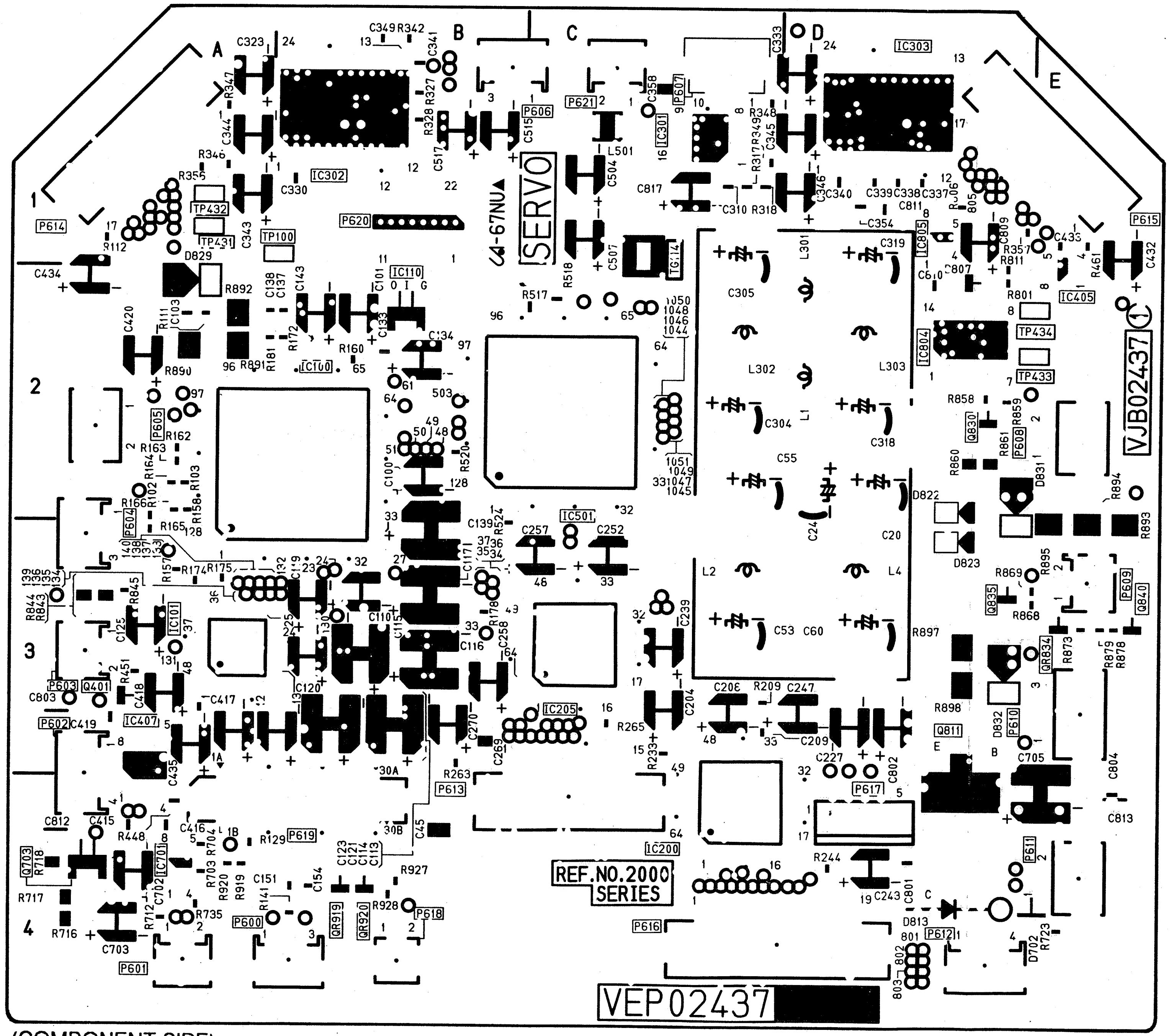
(FIOL SIDE)


SERVO
C4-67NU
REF.NO.2000
SERIES
VEP02437
A
B
C
D
E
1
2
3
4

(COMPONENT SIDE)

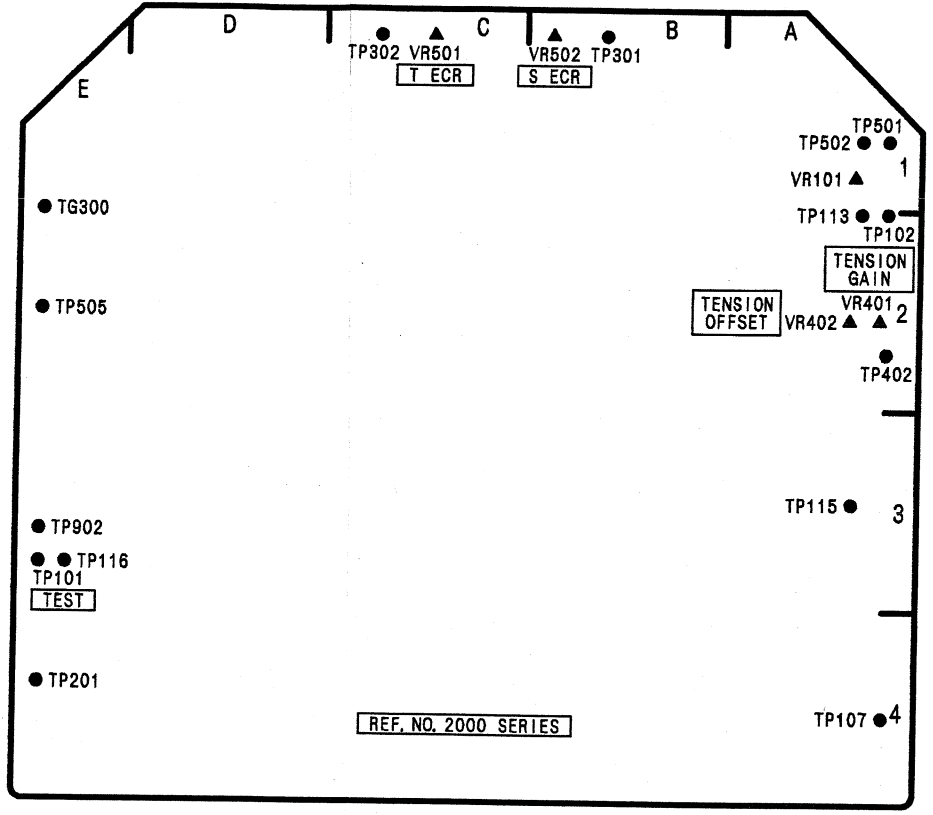

A
1
2
3
4
TP502
TP501
TP113
TP102
VR402
TENSION OFFSET
TENSION GAIN
VR401
IC409
IC401
IC404
IC406
IC407
TP115
TP107
QR150
QR701
QR702
D701

(FIOL SIDE)


A
B
C
D
E
1
2
3
4
SERVO
VJB02437
REF.NO.2000 SERIES
VEP02437
IC110
IC302
IC303
IC501
IC205
IC200
IC401
IC405
IC407
IC703
IC406
IC804
P614
P615
P620
P606
P621
P607
P605
P604
P603
P602
P613
P616
P617
P601
P600
P619
P618
P612
P611
P610
P608
P609
TP100
TP431
TP432
TP433
TP434
TG114
L301
L302
L303
L501
C305
C304
C318
C55
C53
C60
C20

(COMPONENT SIDE)

SERVO P. C. BOARD


D
C
B
A
E
TP302
VR501
T ECR
VR502
TP301
S ECR
TP501
TP502
1
VR101
TP113
TP102
TENSION GAIN
TENSION OFFSET
VR401
VR402
2
TP402
TG300
TP505
TP902
TP116
TP101
TEST
TP115
3
TP201
TP107
4
REF. NO. 2000 SERIES

(FOIL SIDE)

SERVO

Transistors		
Q2	C-3	Ⓕ
Q3	D-3	Ⓕ
Q4	D-2	Ⓕ
Q5	C-2	Ⓕ
Q6	C-2	Ⓕ
Q7	C-2	Ⓕ
Q100	B-3	Ⓕ
Q101	B-3	Ⓕ
Q103	B-3	Ⓕ
Q104	B-3	Ⓕ
Q105	C-3	Ⓕ
Q106	A-3	Ⓕ
Q301	D-2	Ⓕ
Q302	D-2	Ⓕ
Q401	A-3	Ⓒ
Q702	B-4	Ⓕ
Q703	A-4	Ⓒ
Q811	D-3	Ⓒ
Q812	D-4	Ⓕ
Q815	A-3	Ⓕ
Q816	A-3	Ⓕ
Q817	B-2	Ⓕ
Q819	A-2	Ⓕ
Q820	A-2	Ⓕ
Q821	A-1	Ⓕ
Q822	A-3	Ⓕ
Q823	A-3	Ⓕ
Q825	D-2	Ⓕ
Q826	E-2	Ⓕ
Q827	D-3	Ⓕ
Q829	D-2	Ⓕ
Q830	D-2	Ⓒ
Q831	D-3	Ⓕ
Q832	E-2	Ⓕ
Q833	E-3	Ⓕ
Q835	D-3	Ⓒ
Q836	D-3	Ⓕ
Q837	E-3	Ⓕ
Q839	E-3	Ⓕ
Q840	E-3	Ⓒ
Q841	E-3	Ⓕ
Q842	D-3	Ⓕ
Q843	D-3	Ⓕ
Q906	B-2	Ⓕ
Q908	B-2	Ⓕ
Q914	B-1	Ⓕ
Q918	B-2	Ⓕ
Q922	B-3	Ⓕ

Transistor-Resistors		
QR2	C-2	Ⓕ
QR5	C-2	Ⓕ
QR101	B-3	Ⓕ
QR102	B-3	Ⓕ
QR106	B-4	Ⓕ
QR149	B-4	Ⓕ
QR150	A-3	Ⓕ
QR501	C-2	Ⓕ
QR701	A-4	Ⓕ
QR702	A-4	Ⓕ
QR703	B-4	Ⓕ
QR801	D-1	Ⓕ
QR804	D-1	Ⓕ
QR809	D-1	Ⓕ
QR810	E-1	Ⓕ
QR813	E-1	Ⓕ
QR814	A-3	Ⓕ
QR818	A-2	Ⓕ
QR824	E-2	Ⓕ
QR828	D-2	Ⓕ
QR834	E-3	Ⓒ
QR838	E-3	Ⓕ
QR844	E-2	Ⓕ
QR845	E-2	Ⓕ
QR846	E-2	Ⓕ
QR905	B-2	Ⓕ
QR907	B-2	Ⓕ
QR913	B-1	Ⓕ
QR915	B-2	Ⓕ
QR917	B-2	Ⓕ
QR919	B-4	Ⓒ
QR920	B-4	Ⓒ
QR921	B-3	Ⓕ

Integrated Circuit		
IC6	C-4	Ⓕ
IC7	B-4	Ⓕ
IC9	C-2	Ⓕ
IC101	A-3	Ⓒ
IC103	A-4	Ⓕ
IC104	B-2	Ⓕ
IC110	B-2	Ⓒ
IC200	C-4	Ⓒ
IC201	C-3	Ⓕ
IC202	D-4	Ⓕ
IC203	C-4	Ⓕ
IC204	C-4	Ⓕ
IC205	C-3	Ⓒ
IC301	C-1	Ⓒ
IC302	B-1	Ⓒ
IC303	D-1	Ⓕ
IC401	A-1	Ⓕ
IC402		
IC403	A-2	Ⓕ
IC404	A-1	Ⓕ
IC405	E-2	Ⓕ
IC406	A-4	Ⓕ
IC407	A-3	Ⓒ
IC409	A-1	Ⓕ
IC410	E-1	Ⓕ
IC502	C-2	Ⓕ
IC503	C-1	Ⓕ
IC701	A-4	Ⓒ
IC702	E-4	Ⓕ
IC801	D-1	Ⓕ
IC802	D-4	Ⓕ
IC803	D-1	Ⓕ
IC804	D-2	Ⓒ
IC805	D-1	Ⓒ
IC806	D-2	Ⓕ

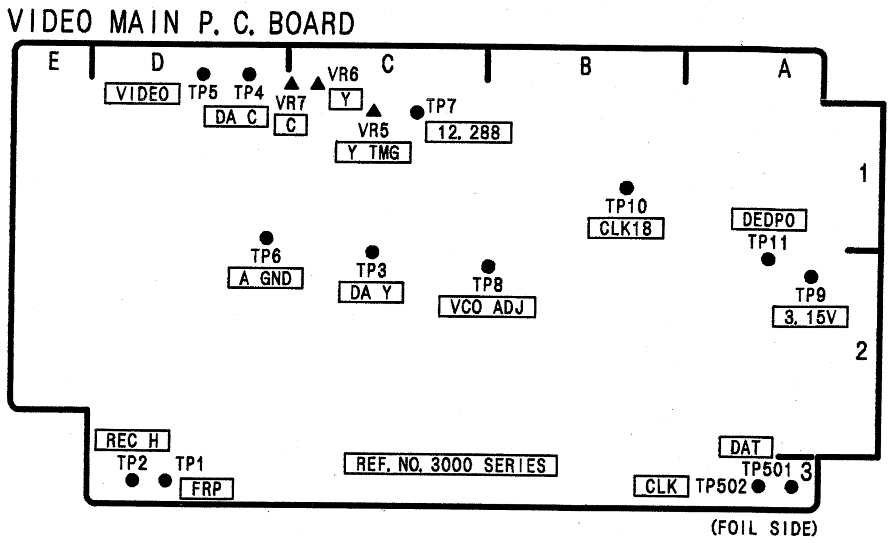
Test Points		
TP100	B-1	Ⓒ
TP101	E-3	Ⓕ
TP102	A-2	Ⓕ
TP107	A-4	Ⓕ
TP113	A-2	Ⓕ
TP115	A-3	Ⓕ
TP116	E-3	Ⓕ
TP201	E-4	Ⓕ
TP301	B-1	Ⓕ
TP302	C-1	Ⓕ
TP402	A-2	Ⓕ
TP431	A-1	Ⓒ
TP432	A-1	Ⓒ
TP433	E-2	Ⓒ
TP434	E-2	Ⓒ
TP501	A-1	Ⓕ
TP502	A-1	Ⓕ
TP505	E-2	Ⓕ
TP902	E-3	Ⓕ
TG114	C-1	Ⓒ
TG300	E-2	Ⓕ

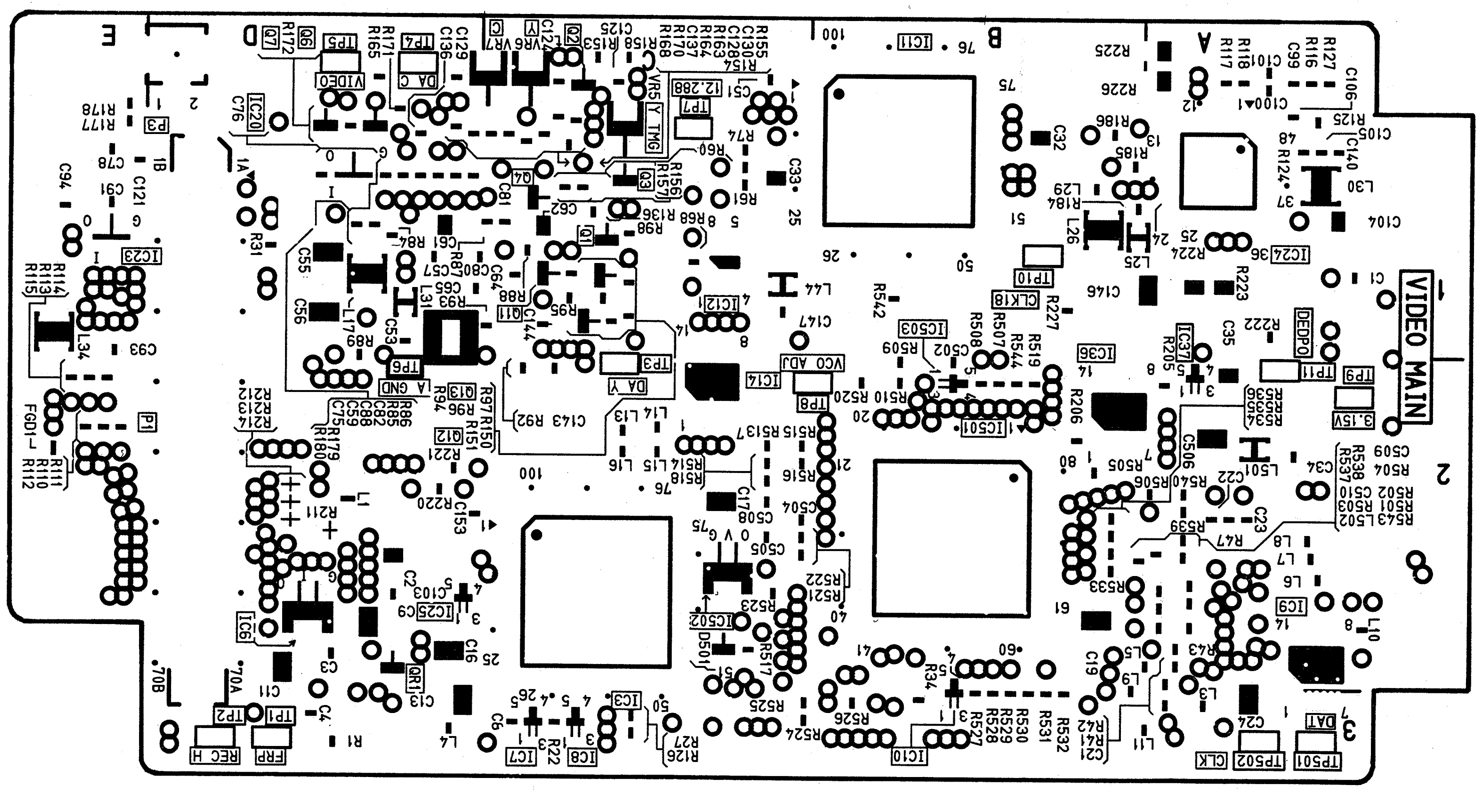
Adjustments		
VR100		
VR101	A-1	Ⓕ
VR401	A-2	Ⓕ
VR402	A-2	Ⓕ
VR501	C-1	Ⓕ
VR502	B-1	Ⓕ

Connectors		
P600	A-4	Ⓒ
P601	A-4	Ⓒ
P602	A-3	Ⓒ
P603	A-3	Ⓒ
P604	A-3	Ⓒ
P605	A-2	Ⓒ
P606	C-1	Ⓒ
P607	C-1	Ⓒ
P608	D-2	Ⓒ
P609	E-3	Ⓒ
P610	D-3	Ⓒ
P611	E-4	Ⓒ
P612	D-4	Ⓒ
P613	B-4	Ⓒ
P614	A-1	Ⓒ
P615	E-1	Ⓒ
P616	C-4	Ⓒ
P617	D-4	Ⓒ
P618	B-4	Ⓒ
P619	B-4	Ⓒ
P620	B-1	Ⓒ
P621	C-1	Ⓒ

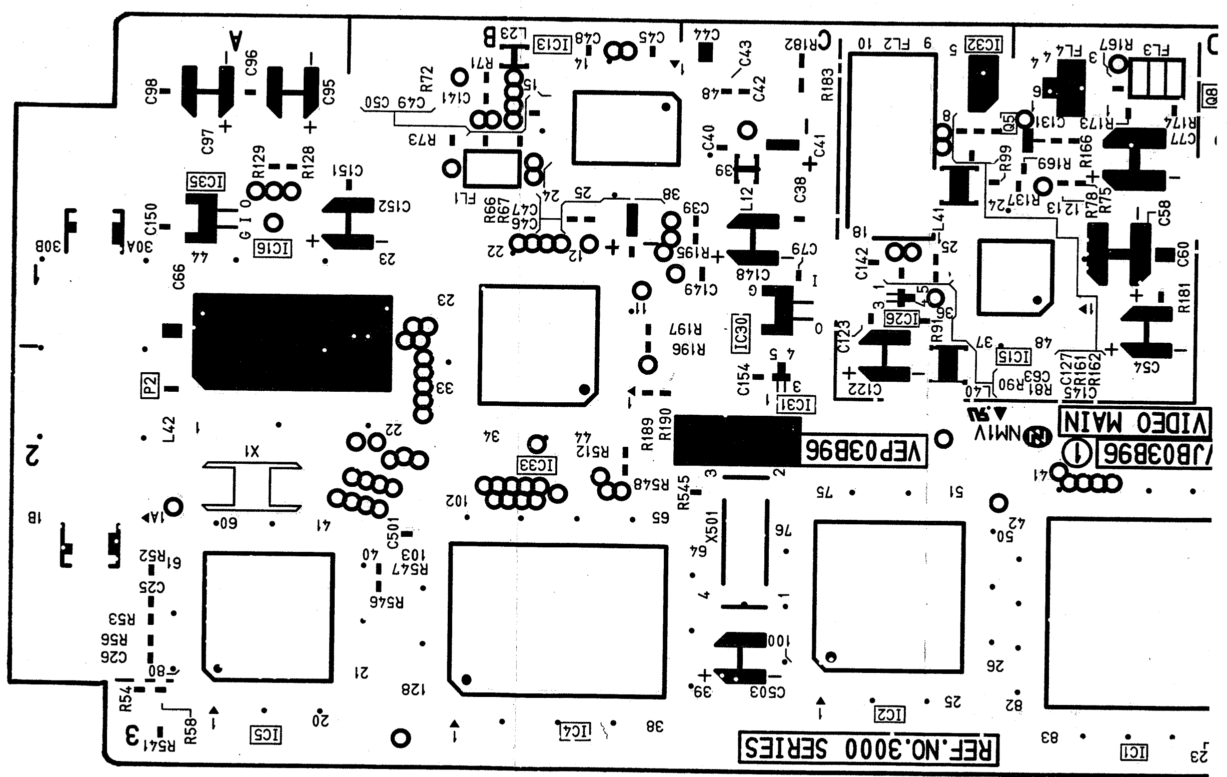
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

VIDEO MAIN P.C. BOARD (VEP03B96B)

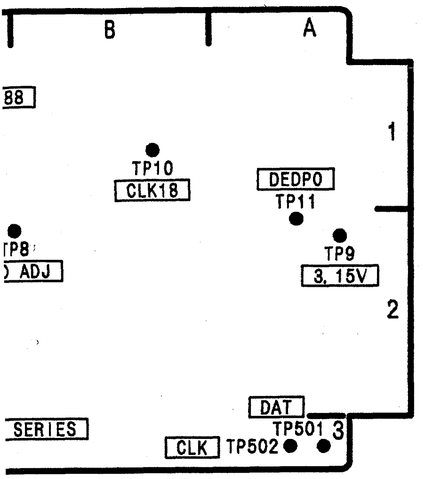

VIDEO MAIN P. C. BOARD
E
D
C
B
A
1
2
3
VIDEO
TP5
TP4
DA C
VR7
C
VR6
Y
VR5
Y TMG
TP7
12. 288
TP10
CLK18
DEDPO
TP11
TP9
3. 15V
TP6
A GND
TP3
DA Y
TP8
VCO ADJ
REC H
TP2
TP1
FRP
REF. NO. 3000 SERIES
DAT
TP501
CLK
TP502
(FOIL SIDE)


VIDEO MAIN
REF. NO. 3000 SERIES

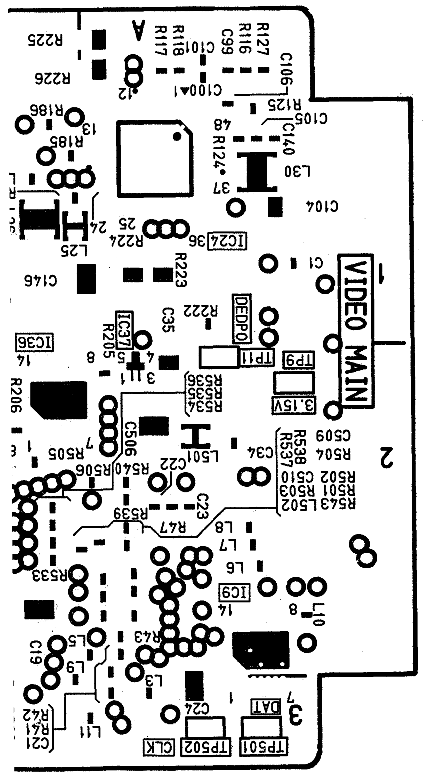
(FIOL SIDE)


VIDEO MAIN
VEP03B96
REF.NO.3000 SERIES

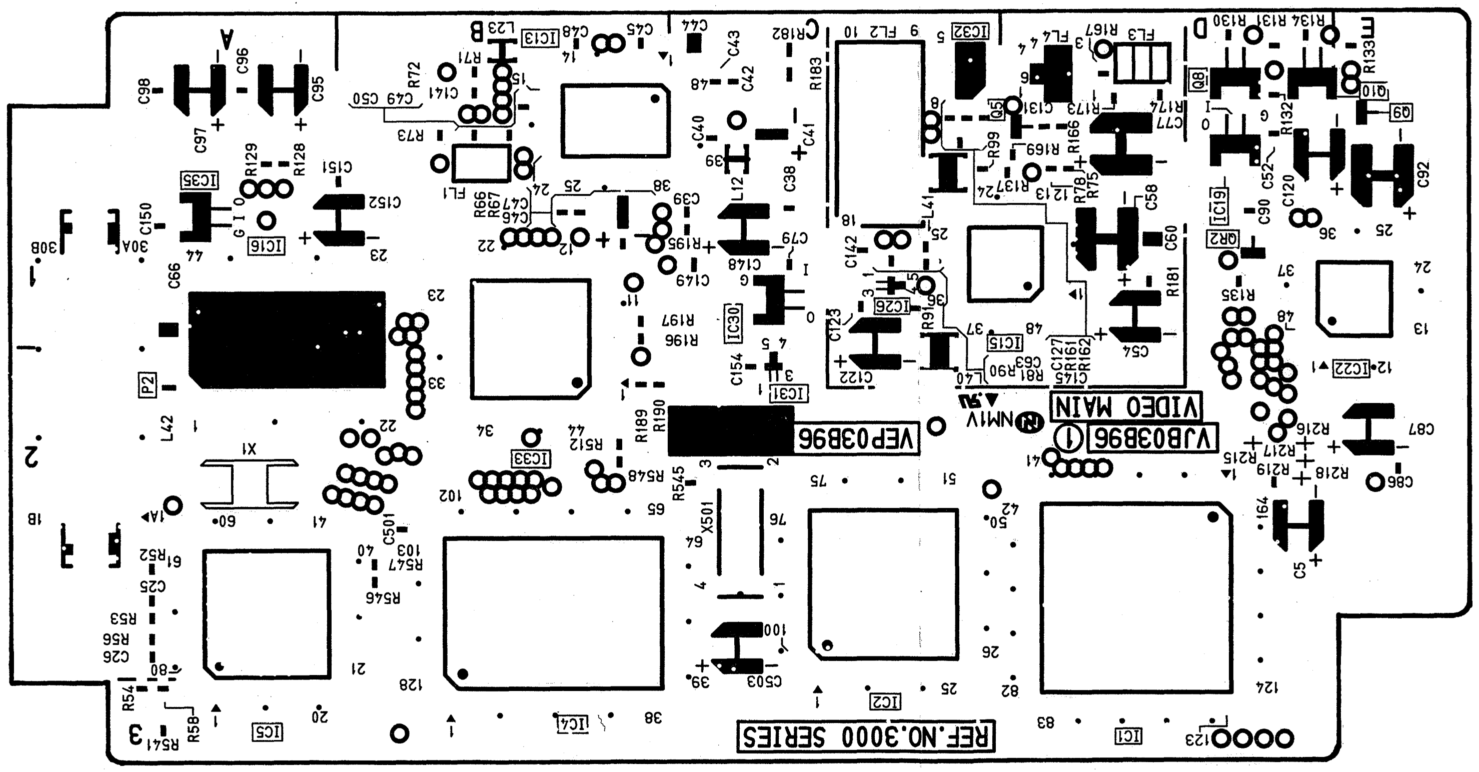
(COMPONENT SIDE)


B
A
1
2
3
88
TP10
CLK18
DEDPO
TP11
TP8
ADJ
TP9
3, 15V
SERIES
DAT
TP501
CLK
TP502

(FOIL SIDE)


VIDEO MAIN
DEDPO
TP11
TP9
3.15V
DAT
TP501
TP502
CLK
2
3

(FIOL SIDE)


VIDEO MAIN
VJB03B96
VEP03B96
REF.NO.3000 SERIES
A
B
C
D
E
1
2
3

(COMPONENT SIDE)

VIDEO MAIN		
Transistors		
Q1	C-1	Ⓕ
Q2	C-1	Ⓕ
Q3	C-1	Ⓕ
Q4	C-1	Ⓕ
Q5	C-1	Ⓒ
Q6	D-1	Ⓕ
Q7	D-1	Ⓕ
Q8	D-1	Ⓒ
Q9	E-1	Ⓒ
Q10	E-1	Ⓒ
Q11	C-1	Ⓕ
Q12	D-2	Ⓕ
Q13	D-2	Ⓕ
Transistor-Resistors		
QR1	D-2	Ⓕ
QR2	D-1	Ⓒ
Integrated Circuit		
IC1	D-3	Ⓒ
IC2	C-3	Ⓒ
IC3	C-3	Ⓕ
IC4	B-3	Ⓒ
IC5	A-3	Ⓒ
IC6	D-2	Ⓕ
IC7	C-3	Ⓕ
IC9	A-2	Ⓕ
IC10	B-3	Ⓕ
IC11	B-1	Ⓕ
IC12	C-1	Ⓕ
IC13	B-1	Ⓒ
IC14	C-2	Ⓕ
IC15	D-1	Ⓒ
IC16	A-1	Ⓒ
IC19	D-1	Ⓒ
IC20	D-1	Ⓕ
IC22	E-2	Ⓒ
IC23	E-1	Ⓕ
IC24	A-1	Ⓕ
IC25	D-2	Ⓕ
IC26	C-1	Ⓒ
IC30	C-1	Ⓒ
IC32	C-1	Ⓕ
IC33	B-2	Ⓒ
IC35	A-1	Ⓕ
IC36	B-2	Ⓕ
IC37	A-1	Ⓕ
IC501	B-2	Ⓕ
IC502	C-2	Ⓕ
IC503	B-1	Ⓕ
Test Points		
TP1	D-3	Ⓕ
TP2	D-3	Ⓕ
TP3	C-2	Ⓕ
TP4	D-1	Ⓕ
TP5	D-1	Ⓕ
TP6	D-2	Ⓕ
TP7	C-1	Ⓕ
TP8	B-2	Ⓕ
TP9	A-2	Ⓕ
TP10	B-1	Ⓕ
TP11	A-2	Ⓕ
TP501	A-3	Ⓕ
TP502	A-3	Ⓕ
Adjustments		
VR5	C-1	Ⓕ
VR6	C-1	Ⓕ
VR7	C-1	Ⓕ
Connectors		
P1	E-2	Ⓕ
P2	A-2	Ⓒ
P3	D-1	Ⓕ

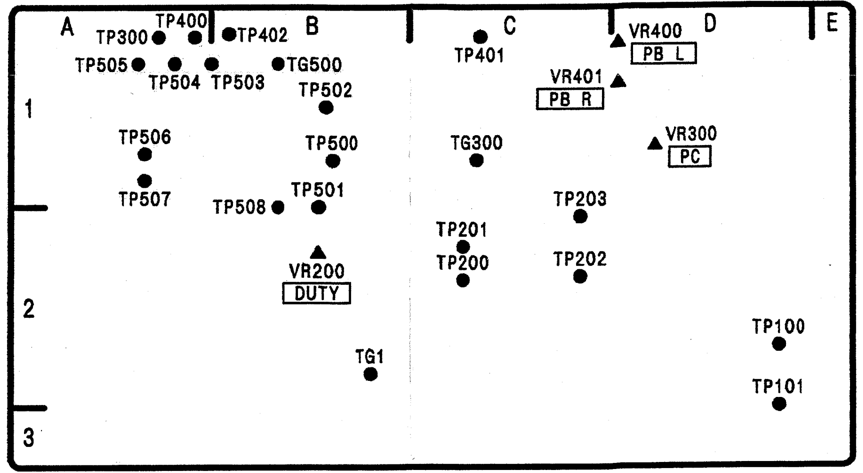
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

RF P.C. BOARD (VEP03B95A)

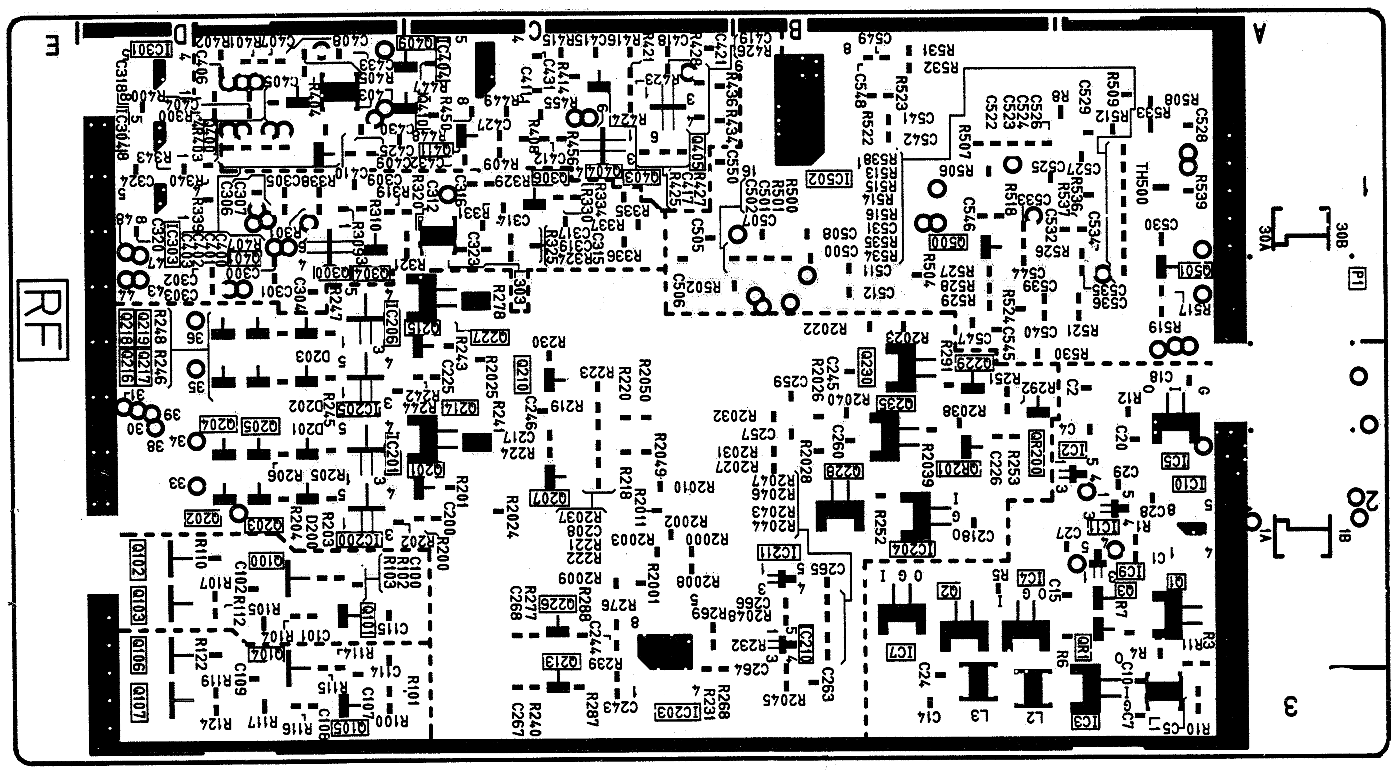
RF		
Transistors		
Q1	A-2	Ⓕ
Q2	B-2	Ⓕ
Q3	A-2	Ⓒ
Q100	D-2	Ⓕ
Q101	D-2	Ⓕ
Q102	D-2	Ⓕ
Q103	D-2	Ⓕ
Q104	D-2	Ⓕ
Q105	D-2	Ⓕ
Q106	D-2	Ⓕ
Q107	D-3	Ⓕ
Q201	C-2	Ⓕ
Q202	D-2	Ⓕ
Q203	D-2	Ⓕ
Q204	D-2	Ⓕ
Q205	D-2	Ⓕ
Q207	C-2	Ⓕ
Q208	D-2	Ⓒ
Q209	D-2	Ⓒ
Q210	C-2	Ⓕ
Q211		
Q212	C-3	Ⓒ
Q213	C-2	Ⓕ
Q214	C-2	Ⓕ
Q215	C-1	Ⓕ
Q216	D-2	Ⓕ
Q217	D-2	Ⓕ
Q218	D-1	Ⓕ
Q219	D-1	Ⓕ
Q221	D-2	Ⓒ
Q222	D-1	Ⓒ
Q224		
Q225	C-2	Ⓒ
Q226	C-2	Ⓕ
Q227	C-1	Ⓕ
Q228	B-2	Ⓕ
Q229	B-2	Ⓕ
Q230	B-2	Ⓕ
Q231	C-2	Ⓒ
Q232	C-2	Ⓒ
Q233	C-2	Ⓒ
Q234	C-1	Ⓒ
Q235	B-2	Ⓕ
Q300	D-1	Ⓕ
Q304	D-1	Ⓕ
Q305	C-1	Ⓒ
Q306	C-1	Ⓕ
Q307	C-1	Ⓒ
Q400	D-1	Ⓕ
Q401	D-1	Ⓕ
Q403	C-1	Ⓕ
Q404	C-1	Ⓕ
Q405	C-1	Ⓕ
Q406	B-1	Ⓒ
Q407	B-1	Ⓒ
Q408	B-2	Ⓒ
Q409	C-1	Ⓕ
Q410	C-1	Ⓕ
Q411	C-1	Ⓕ
Q500	B-1	Ⓕ
Q501	A-1	Ⓕ
Transistor-Resistors		
QR1	A-2	Ⓒ
QR100	D-2	Ⓒ
QR101	D-3	Ⓒ
QR200	B-2	Ⓕ
QR201	B-2	Ⓕ
QR400	C-1	Ⓒ
QR401	B-1	Ⓒ
Integrated Circuit		
IC1	B-2	Ⓒ
IC2	A-2	Ⓕ
IC3	A-3	Ⓕ
IC4	B-2	Ⓕ
IC5	A-2	Ⓕ
IC6	A-2	Ⓒ
IC7	B-2	Ⓕ
IC100	D-3	Ⓒ
IC101	D-2	Ⓒ
IC200	D-2	Ⓕ
IC201	D-2	Ⓕ
IC203	C-3	Ⓕ
IC204	B-2	Ⓕ
IC205	D-2	Ⓕ
IC206	D-1	Ⓕ
IC207	C-2	Ⓒ
IC208	B-2	Ⓒ
IC300	D-1	Ⓒ
IC301	D-1	Ⓕ
IC302	C-1	Ⓒ
IC303	D-1	Ⓕ
IC304	D-1	Ⓕ
IC400	D-1	Ⓒ
IC401	C-1	Ⓒ
IC402	C-1	Ⓒ
IC403	D-1	Ⓒ
IC404	B-1	Ⓕ
IC500	C-2	Ⓒ
IC501	A-1	Ⓒ
IC502	B-1	Ⓕ
Test Points		
TP100	D-2	Ⓒ
TP101	D-2	Ⓒ
TP200	C-2	Ⓒ
TP201	C-2	Ⓒ
TP202	C-2	Ⓒ
TP203	C-2	Ⓒ
TP300	A-1	Ⓒ
TP400	A-1	Ⓒ
TP401	C-1	Ⓒ
TP402	A-1	Ⓒ
TP500	B-1	Ⓒ
TP501	B-2	Ⓒ
TP502	B-1	Ⓒ
TP503	A-1	Ⓒ
TP504	A-1	Ⓒ
TP505	A-1	Ⓒ
TP506	A-1	Ⓒ
TP507	A-1	Ⓒ
TP508	B-2	Ⓒ
TG1	B-1	Ⓒ
TG300	C-1	Ⓒ
TG500	B-1	Ⓒ
Adjustments		
VR200	B-2	Ⓒ
VR400	C-1	Ⓒ
VR401	C-1	Ⓒ
Connectors		
P1	A-1	Ⓕ
P2	A-2	Ⓒ
P3	D-2	Ⓒ
P4	D-1	Ⓒ

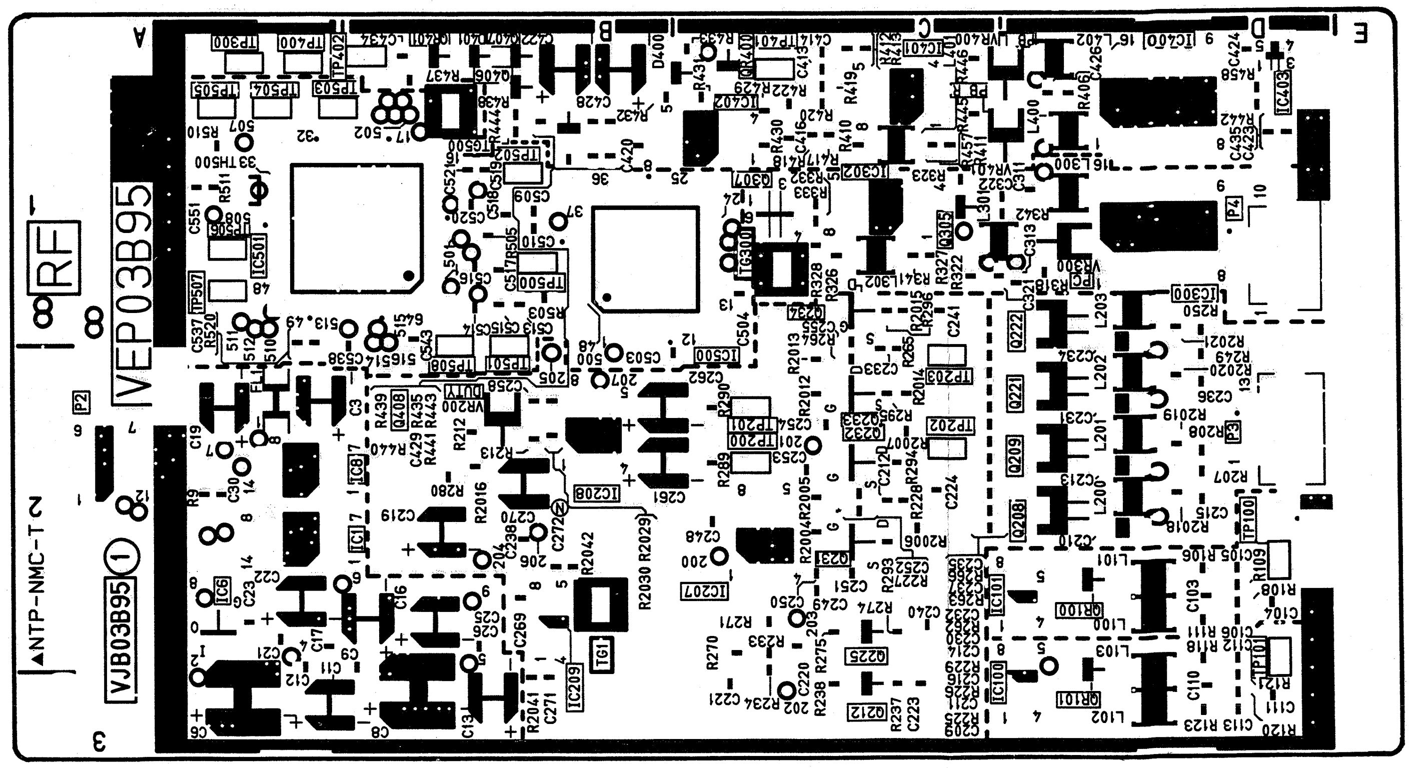
ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

RF P. C. BOARD


A
B
C
D
E
1
2
3
TP300
TP400
TP402
TP505
TP504
TP503
TG500
TP502
TP401
VR400
PB L
VR401
PB R
VR300
PC
TP506
TP507
TP500
TP501
TP508
TG300
TP201
TP200
TP203
TP202
VR200
DUTY
TG1
TP100
TP101

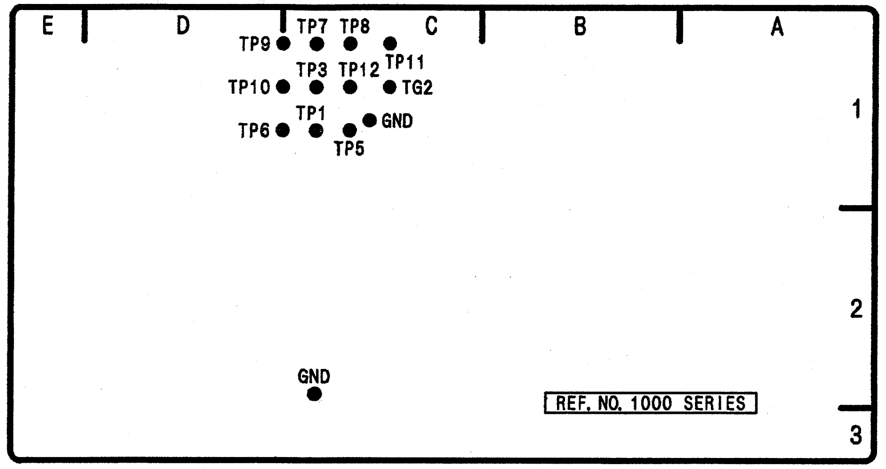
(COMPONENT SIDE)


RF
A
B
C
D
E
1
2
3

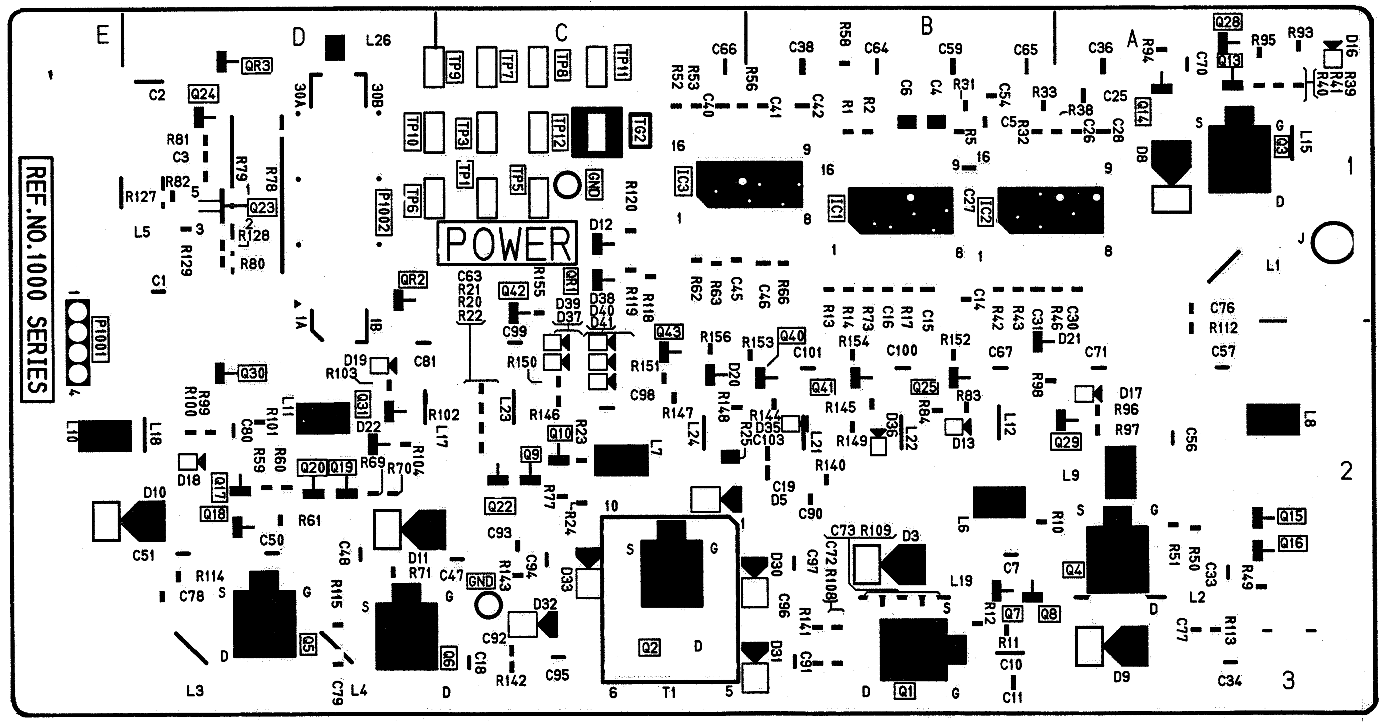

A
B
C
D
E
1
2
3
RF
VEP03B95
VJB03B95 ①
▲NTP-NMC-T

POWER P.C. BOARD (VEP01643A)

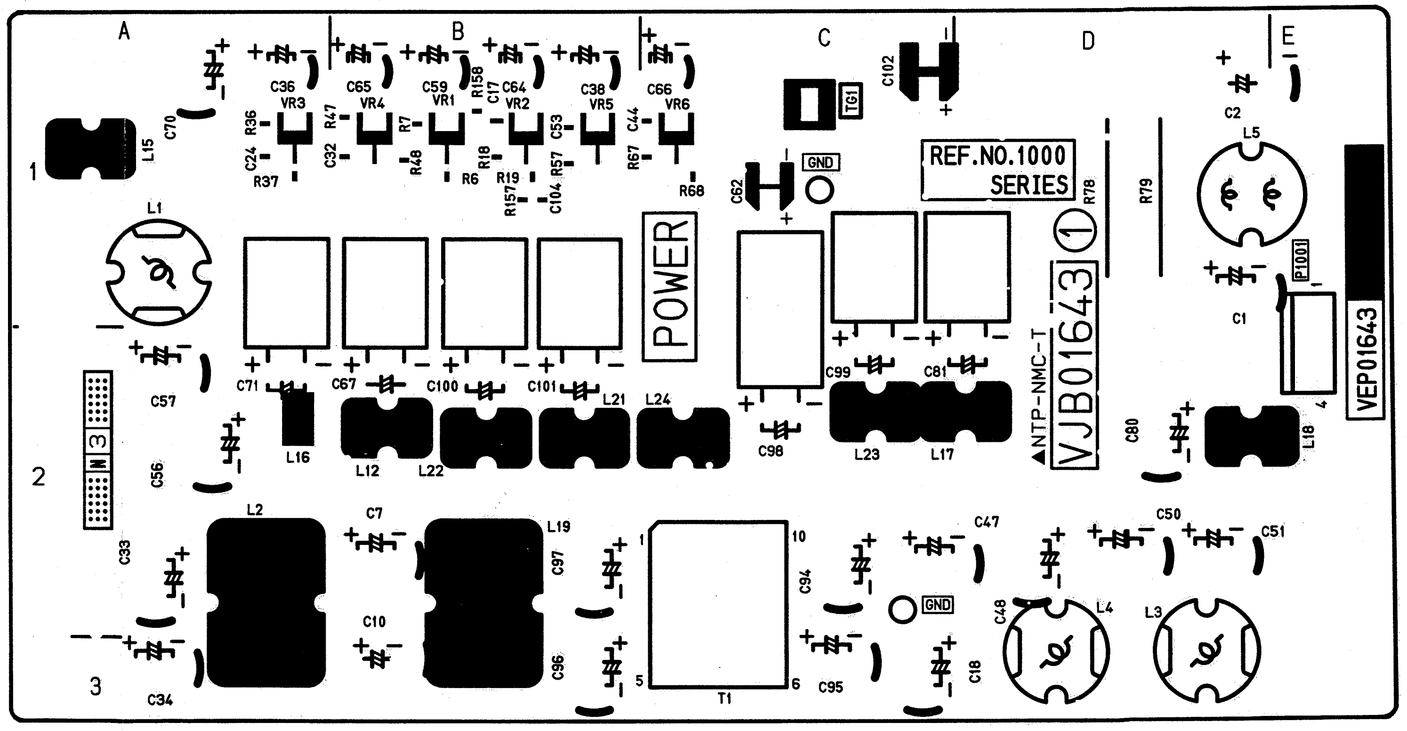
POWER P. C. BOARD


E
D
C
B
A
TP9
TP7
TP8
TP11
TP10
TP3
TP12
TG2
TP1
GND
TP6
TP5
1
2
GND
REF. NO. 1000 SERIES
3

(FOIL SIDE)


E
D
C
B
A
REF.NO.1000 SERIES
POWER
IC1
IC2
IC3
T1
P1001
P1002
L1
L2
L3
L4
L5
1
2
3

(FOIL SIDE)


A
B
C
D
E
REF.NO.1000 SERIES
POWER
VJB01643
①
NTP-NMC-T
VEP01643
P1001
TG1
GND
VR1
VR2
VR3
VR4
VR5
VR6
L1
L2
L3
L4
L5
T1
1
2
3

(COMPONENT SIDE)

POWER

Transistors

Q1001	B-3	Ⓕ
Q1002	C-3	Ⓕ
Q1003	A-1	Ⓕ
Q1004	A-2	Ⓕ
Q1005	D-3	Ⓕ
Q1006	C-3	Ⓕ
Q1007	B-2	Ⓕ
Q1008	B-2	Ⓕ
Q1009	C-2	Ⓕ
Q1010	C-2	Ⓕ
Q1013	A-1	Ⓕ
Q1014	A-1	Ⓕ
Q1015	A-2	Ⓕ
Q1016	A-2	Ⓕ
Q1017	D-2	Ⓕ
Q1018	D-2	Ⓕ
Q1019	D-2	Ⓕ
Q1020	D-2	Ⓕ
Q1022	C-2	Ⓕ
Q1023	D-1	Ⓕ
Q1024	D-1	Ⓕ
Q1025	B-2	Ⓕ
Q1028	A-1	Ⓕ
Q1029	A-2	Ⓕ
Q1030	D-2	Ⓕ
Q1031	D-2	Ⓕ
Q1040	B-2	Ⓕ
Q1041	B-2	Ⓕ
Q1042	C-1	Ⓕ
Q1043	C-2	Ⓕ

Transistor-Resistors

QR1001	C-1	Ⓕ
QR1002	D-1	Ⓕ
QR1003	D-1	Ⓕ

Integrated Circuit

IC1001	C-1	Ⓕ
IC1002	B-1	Ⓕ
IC1003	B-1	Ⓕ

Test Points

TP1	C-1	Ⓕ
TP3	C-1	Ⓕ
TP5	C-1	Ⓕ
TP6	D-1	Ⓕ
TP7	C-1	Ⓕ
TP8	C-1	Ⓕ
TP9	C-1	Ⓕ
TP10	D-1	Ⓕ
TP11	C-1	Ⓕ
TP12	C-1	Ⓕ
TG1001	C-1	Ⓒ
TG1002	C-1	Ⓕ

Adjustments

VR1001	B-1	Ⓒ
VR1002	B-1	Ⓒ
VR1003	A-1	Ⓒ
VR1004	B-1	Ⓒ
VR1005	B-1	Ⓒ
VR1006	C-1	Ⓒ

Connectors

P1001	E-1	
P1002	D-1	Ⓕ

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

AUDIO LCD

Transistors

Q4001	C-2	Ⓕ
Q4002	A-4	Ⓕ
Q4003	A-4	Ⓕ
Q4004	C-1	Ⓒ
Q4007	B-1	Ⓒ
Q4008	A-2	Ⓕ
Q4009	A-2	Ⓕ
Q4010	A-1	Ⓕ
Q4101	D-4	Ⓕ
Q4102	D-4	Ⓒ
Q4103	D-4	Ⓒ
Q4107	D-2	Ⓕ
Q4110	A-2	Ⓕ
Q4111	B-2	Ⓕ
Q4201	C-4	Ⓕ
Q4202	C-3	Ⓒ
Q4203	C-3	Ⓒ
Q4207	D-2	Ⓕ
Q4210	A-2	Ⓕ
Q4211	A-2	Ⓕ
Q4302	B-4	Ⓕ
Q4305	C-4	Ⓕ
Q4306	D-4	Ⓕ
Q4307	D-4	Ⓕ
Q4402	A-4	Ⓕ
Q4405	C-3	Ⓕ
Q4406	C-3	Ⓕ
Q4407	C-4	Ⓕ
Q4702	B-3	Ⓕ
Q4703	A-3	Ⓕ
Q4704	B-3	Ⓒ
Q4705	B-3	Ⓒ
Q6501	E-3	Ⓕ
Q6502	E-3	Ⓕ
Q6503	F-1	Ⓕ

Transistor-Resistors

QR4001	A-2	Ⓕ
QR4006	A-1	Ⓕ
QR4007	A-1	Ⓕ
QR4010	D-1	Ⓕ
QR4012	B-1	Ⓒ
QR4013	B-1	Ⓕ
QR4102	D-2	Ⓕ
QR4103	B-1	Ⓕ
QR4104	B-1	Ⓕ
QR4105	B-2	Ⓕ
QR4106	B-2	Ⓕ
QR4107	B-1	Ⓕ
QR4108	B-1	Ⓕ
QR4201	D-2	Ⓕ
QR4202	D-2	Ⓕ
QR4203	A-3	Ⓕ
QR4204	A-3	Ⓕ
QR4205	A-3	Ⓕ
QR4206	B-2	Ⓕ
QR4207	A-1	Ⓕ
QR4208	A-1	Ⓕ
QR4301	D-4	Ⓕ
QR4302	D-4	Ⓕ
QR4303	D-4	Ⓕ
QR4304	C-4	Ⓕ
QR4401	D-4	Ⓕ
QR4402	D-4	Ⓕ
QR4403	C-4	Ⓕ
QR4404	C-4	Ⓕ
QR4507	B-3	Ⓕ
QR4508	C-2	Ⓕ
QR4601	F-1	Ⓕ
QR6501	G-1	Ⓕ
QR6502	G-2	Ⓕ
QR6503	F-1	Ⓕ
QR6504	F-1	Ⓕ

Integrated Circuits

IC4001	B-2	Ⓒ
IC4002	C-2	Ⓕ
IC4003	E-1	Ⓕ
IC4004	B-2	Ⓕ
IC4005	D-3	Ⓕ
IC4006	C-1	Ⓕ
IC4007	D-1	Ⓒ
IC4008	D-1	Ⓒ
IC4009	C-2	Ⓕ
IC4010	C-1	Ⓕ
IC4011	B-1	Ⓕ
IC4012	B-1	Ⓕ
IC4013	A-1	Ⓕ
IC4014	D-1	Ⓒ
IC4015	C-2	Ⓕ
IC4016	D-2	Ⓕ
IC4017	B-4	Ⓕ
IC4102	D-2	Ⓕ
IC4103	D-4	Ⓕ
IC4105	D-3	Ⓕ
IC4202	D-2	Ⓕ
IC4203	D-3	Ⓕ
IC4205	C-3	Ⓕ
IC4501	C-2	Ⓕ
IC4502	B-4	Ⓕ
IC4503	C-3	Ⓒ
IC4602	E-2	Ⓕ
IC4603	E-2	Ⓕ
IC4701	B-3	Ⓕ
IC4702	B-3	Ⓕ
IC4703	C-4	Ⓒ
IC4704	A-2	Ⓕ
IC6501	F-1	Ⓕ
IC6502	G-3	Ⓕ
IC6503	E-3	Ⓕ
IC6505	G-4	Ⓕ

Test Points

TP4101	D-1	Ⓕ
TP4102	E-2	Ⓕ
TP4201	D-1	Ⓕ
TP4202	E-2	Ⓕ
TP4501	B-3	Ⓕ
TP4505	C-2	Ⓕ
TP4601	F-2	Ⓕ
TP4602	F-1	Ⓕ
TP6501	E-3	Ⓕ
TP6502	G-1	Ⓕ
TP6503	G-1	Ⓕ
TP6504	G-1	Ⓕ
TP6505	F-1	Ⓕ
TP6506	F-1	Ⓕ
TG4001	D-2	Ⓕ

Adjustments

VR4001	C-1	Ⓕ
VR4002	C-1	Ⓕ
VR4101	F-3	
VR4102	D-3	
VR4103	C-2	
VR4201	F-3	
VR4202	C-3	
VR4203	D-2	
VR4301	B-3	
VR4401	B-4	
VR4501	C-3	
VR4503	C-4	Ⓕ
VR4701		

Switches

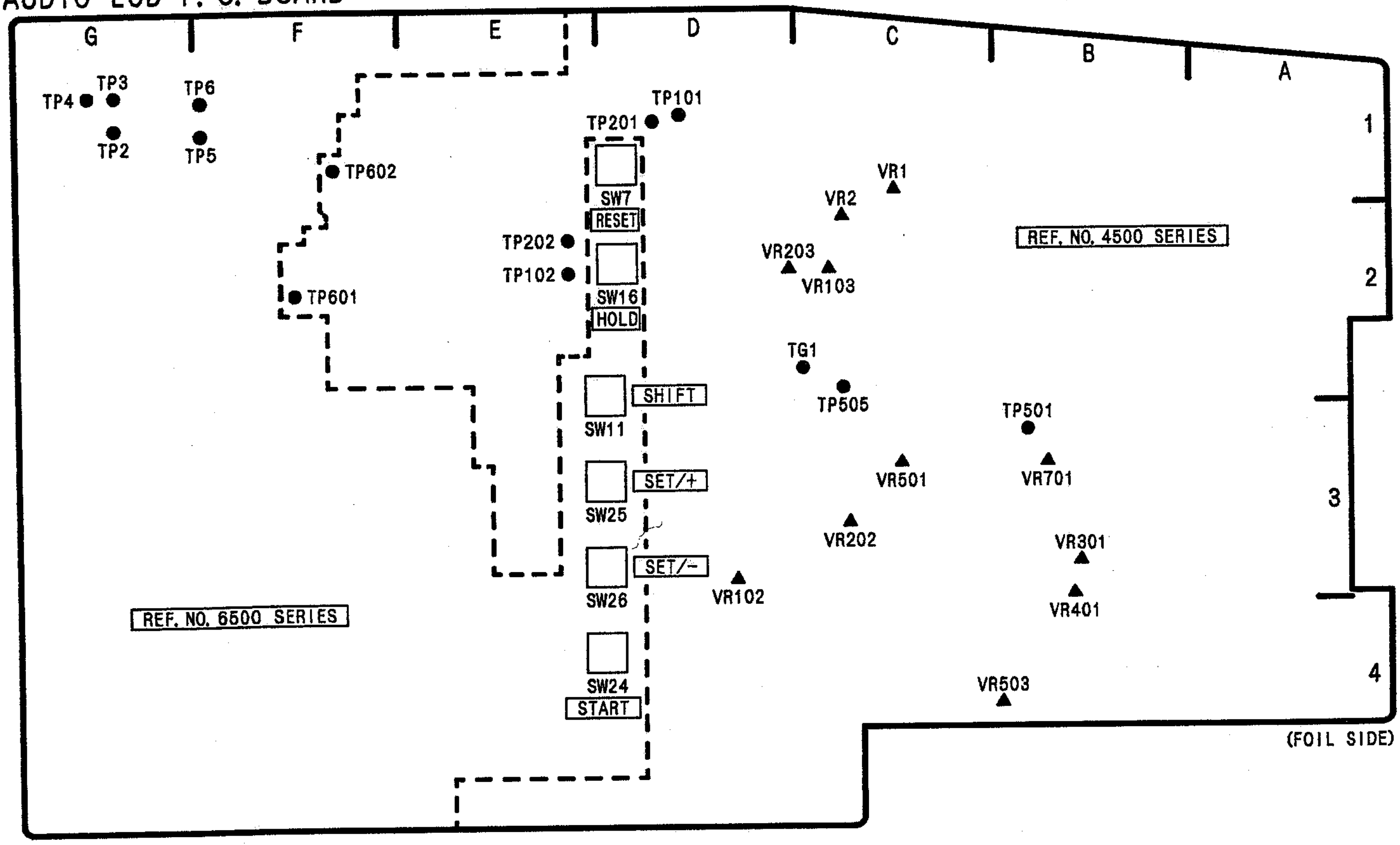
SW4701	G-1	Ⓒ
SW6501	G-1	
SW6502	G-1	
SW6503	E-4	
SW6504	G-2	
SW6505	G-3	
SW6506	G-4	
SW6507	D-1	
SW6508	F-3	
SW6509	F-3	
SW6510	E-3	
SW6511	D-3	
SW6512	F-4	
SW6514	F-4	
SW6516	D-2	
SW6524	D-4	
SW6525	D-3	
SW6526	D-3	

Connectors

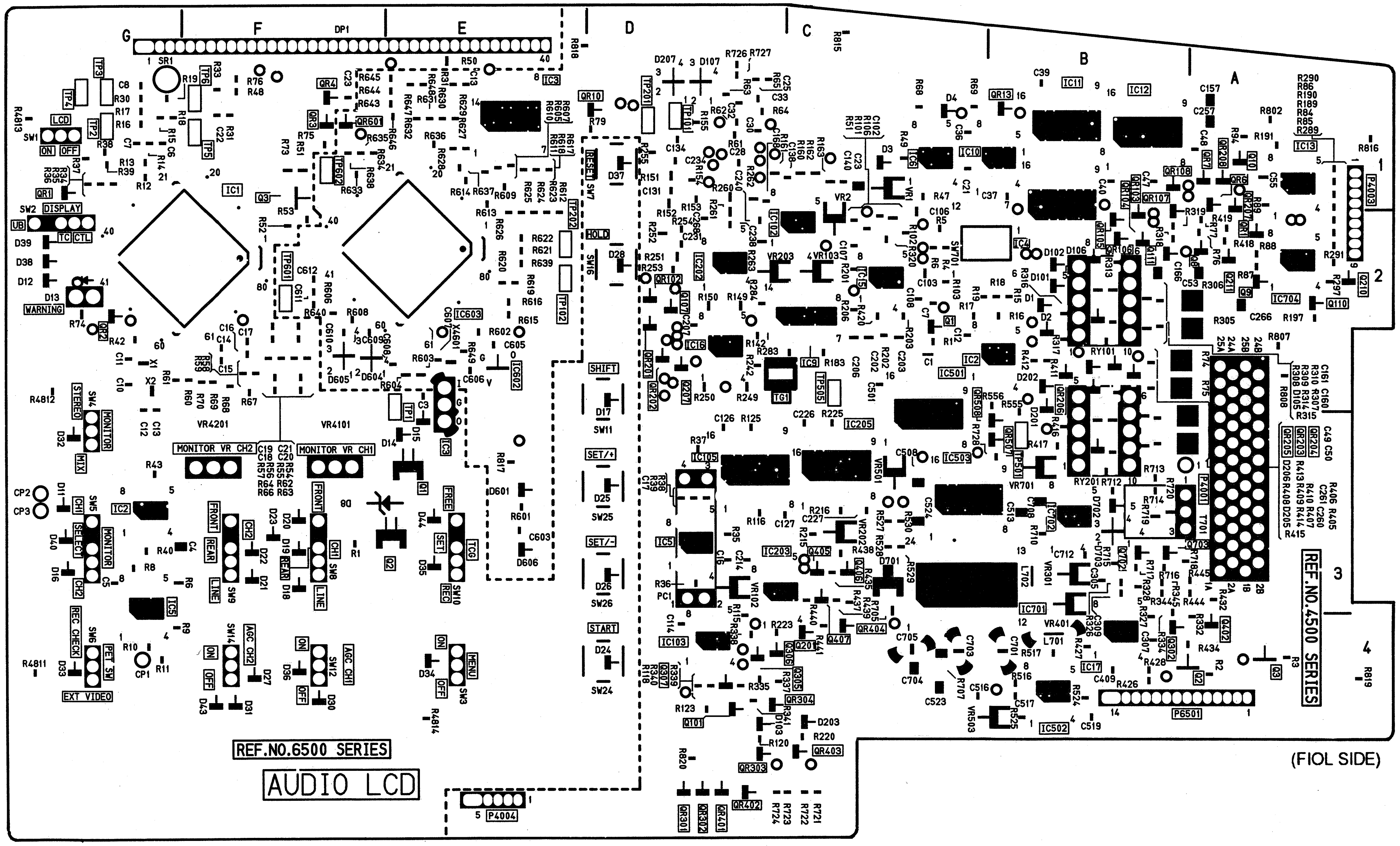
P4001	A-3	
P4002	G-4	Ⓒ
P4003	A-1	
P4004	E-4	
P4005	A-1	Ⓒ
P6501	A-4	

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE

AUDIO LCD P. C. BOARD


G
F
E
D
C
B
A
1
2
3
4
TP3
TP4
TP2
TP6
TP5
TP602
TP601
TP101
TP201
SW7
RESET
TP202
TP102
SW16
HOLD
SHIFT
SW11
SET/+
SW25
SET/−
SW26
SW24
START
VR1
VR2
VR203
VR103
TG1
TP505
TP501
VR501
VR701
VR202
VR301
VR102
VR401
VR503
REF. NO. 4500 SERIES
REF. NO. 6500 SERIES
(FOIL SIDE)

AUDIO LCD P.C. BOARD (VEP04522B)


G
F
E
D
C
B
A
DP1
LCD
DISPLAY
WARNING
STEREO
MONITOR
MIX
MONITOR VR CH2
MONITOR VR CH1
VR4201
VR4101
SELECT
FRONT
REAR
LINE
REC CHECK
PET SW
EXT VIDEO
AGC CH2
AGC CH1
FREE
SET
REC
MENU
RESET SW7
HOLD
SHIFT
SET/+
SET/-
START
SW11
SW25
SW26
SW24
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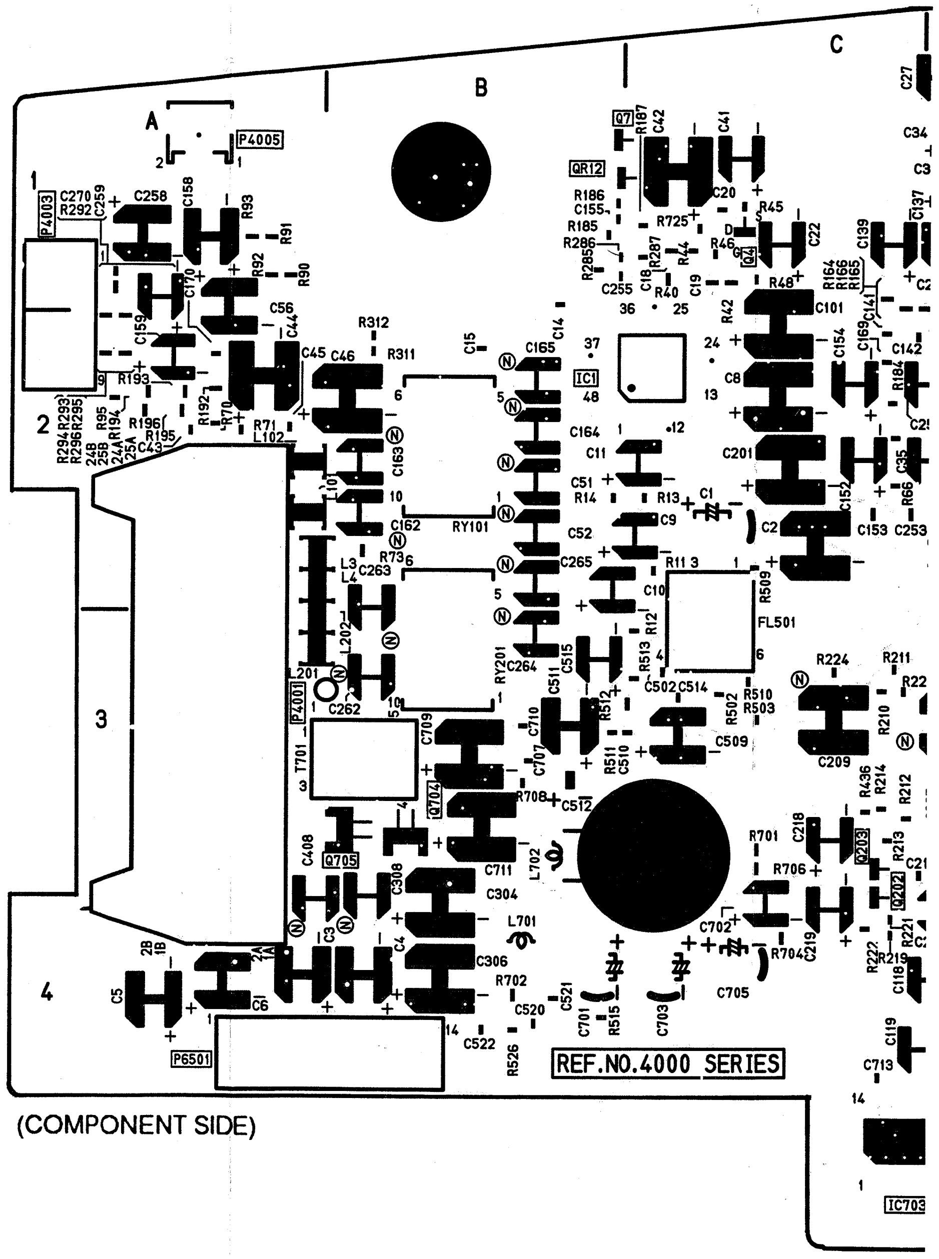
AUDIO LCD
P4004
P6501
REF.NO.4500 SERIES
1
2
3
4

(FIOL SIDE)


A
B
C
P4005
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RY101
RY201
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FL501
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IC703
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2
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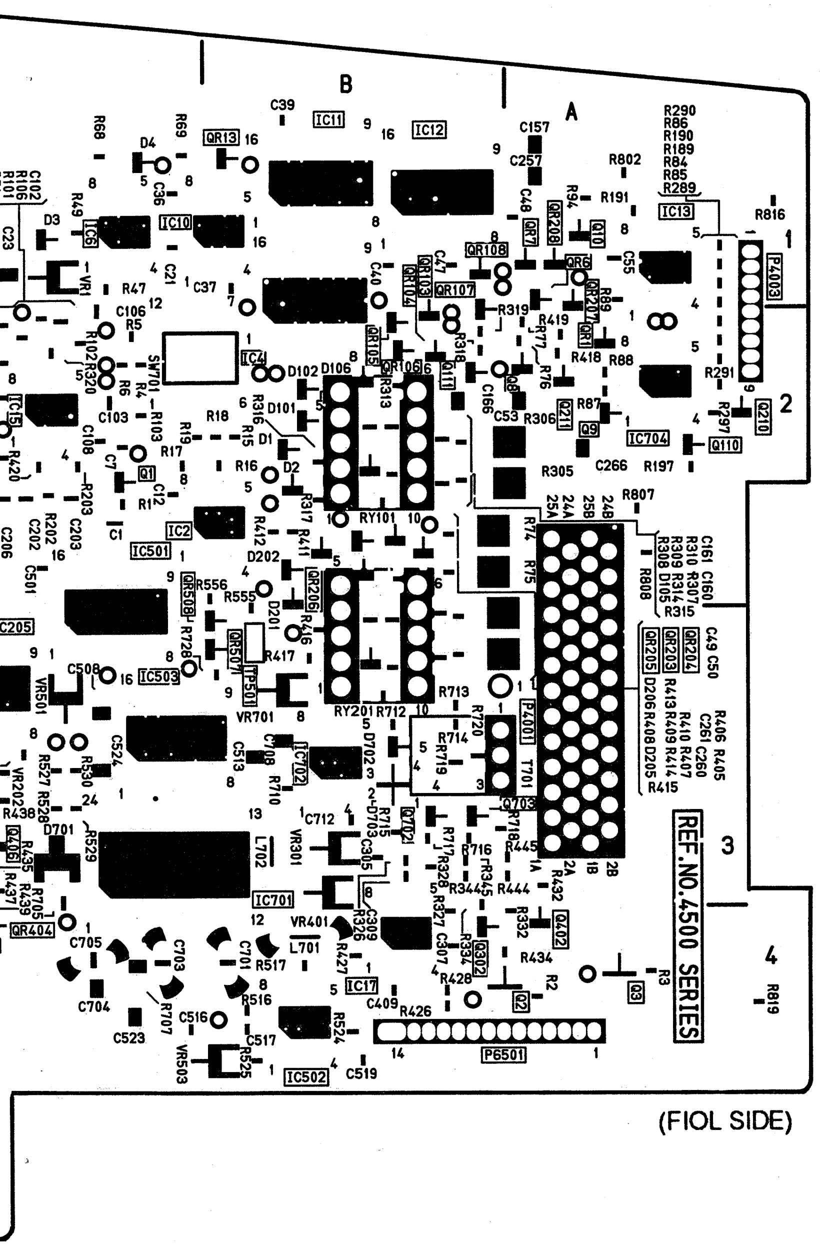
4

(COMPONENT SIDE)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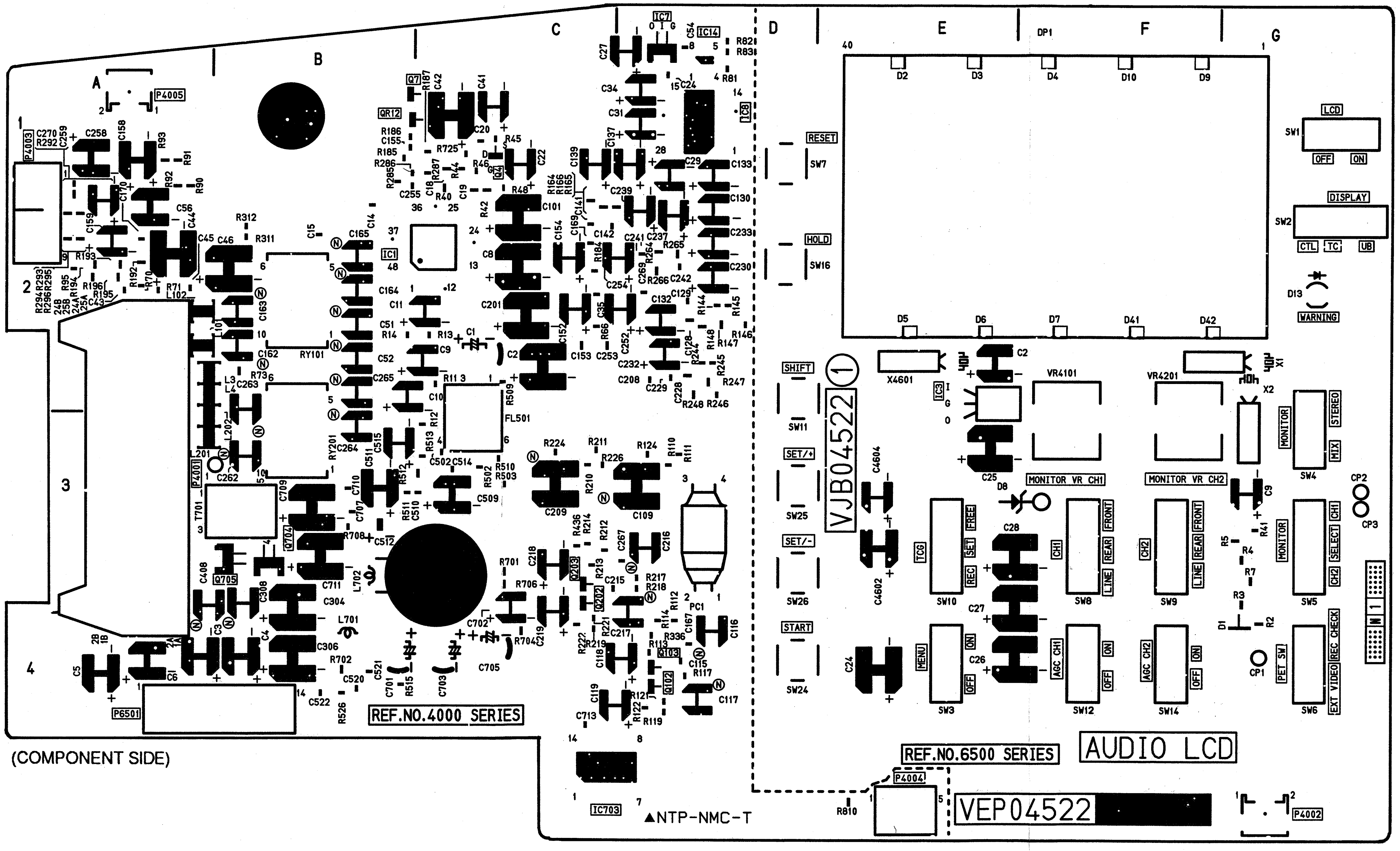
IC12
IC13
P4003

(FIOL SIDE)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AUDIO LCD
VJB04522①
VEP04522
▲NTP-NMC-T
A
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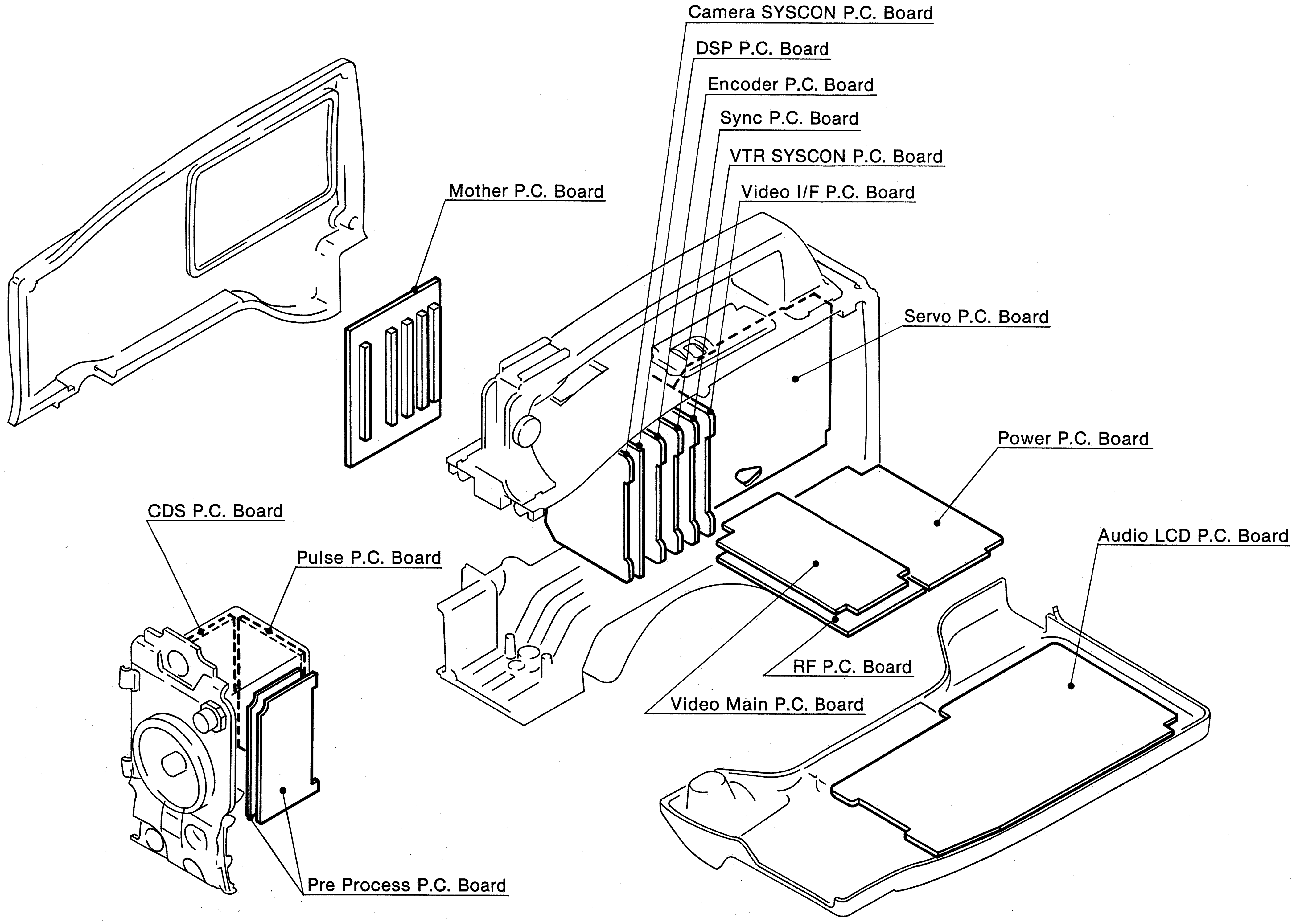
C
D
E
F
G
P4005
P4003
P6501
P4001
P4004
P4002
IC703
IC7
IC14
IC1
IC3
FL501
T701
RY101
RY201
DP1
LCD
OFF
ON
DISPLAY
CTL
TC
UB
WARNING
RESET
HOLD
SHIFT
SET/+
SET/-
START
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW14
SW16
SW24
SW25
SW26
X4601
X2
VR4101
VR4201
MONITOR VR CH1
MONITOR VR CH2
MONITOR
STEREO
MIX
SELECT
CH1
CH2
TCG
REC
SET
FREE
LINE
REAR
FRONT
MENU
AGC CH1
AGC CH2
PET SW
EXT VIDEO
REC CHECK

(COMPONENT SIDE)

CIRCUIT BOARD LOCATION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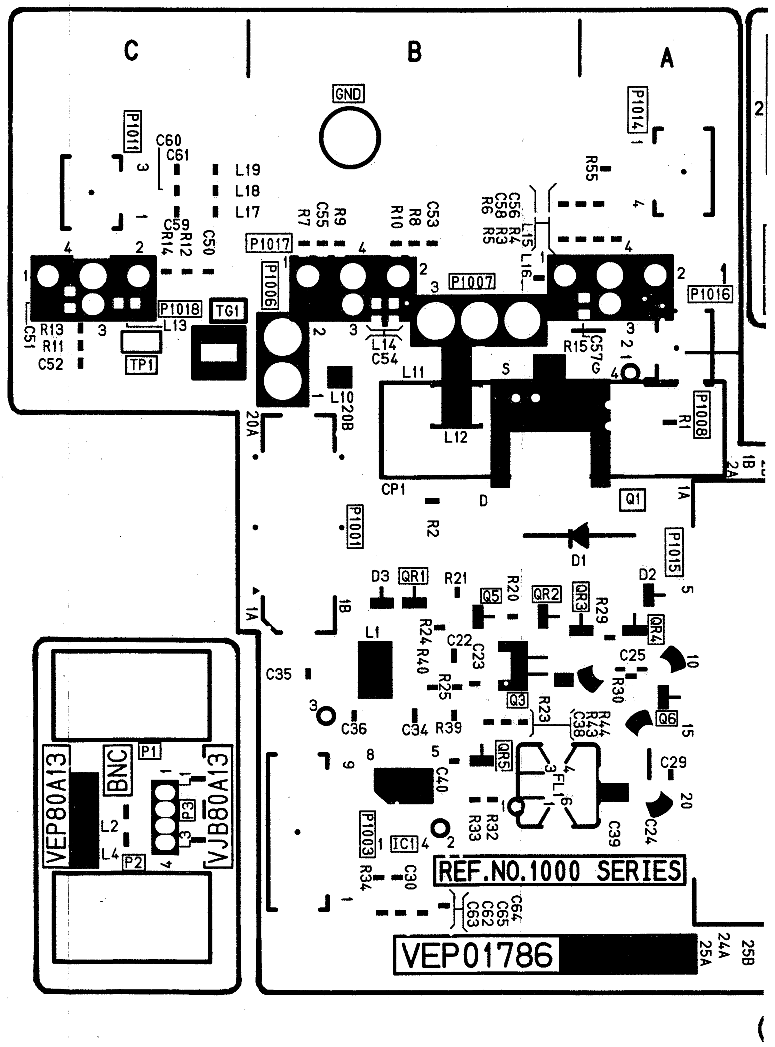
DSP P.C. Board
Encoder P.C. Board
Sync P.C. Board
VTR SYSCON P.C. Board
Video I/F P.C. Board
Mother P.C. Board
Servo P.C. Board
Power P.C. Board
Audio LCD P.C. Board
CDS P.C. Board
Pulse P.C. Board
RF P.C. Board
Video Main P.C. Board
Pre Process P.C. Board

REAR JACK P.C. BOARD (VEP01786/
FRONT MIC P.C. BOARD (VEP80A14/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B
A
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C60
C61
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L18
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R12
R14
C50
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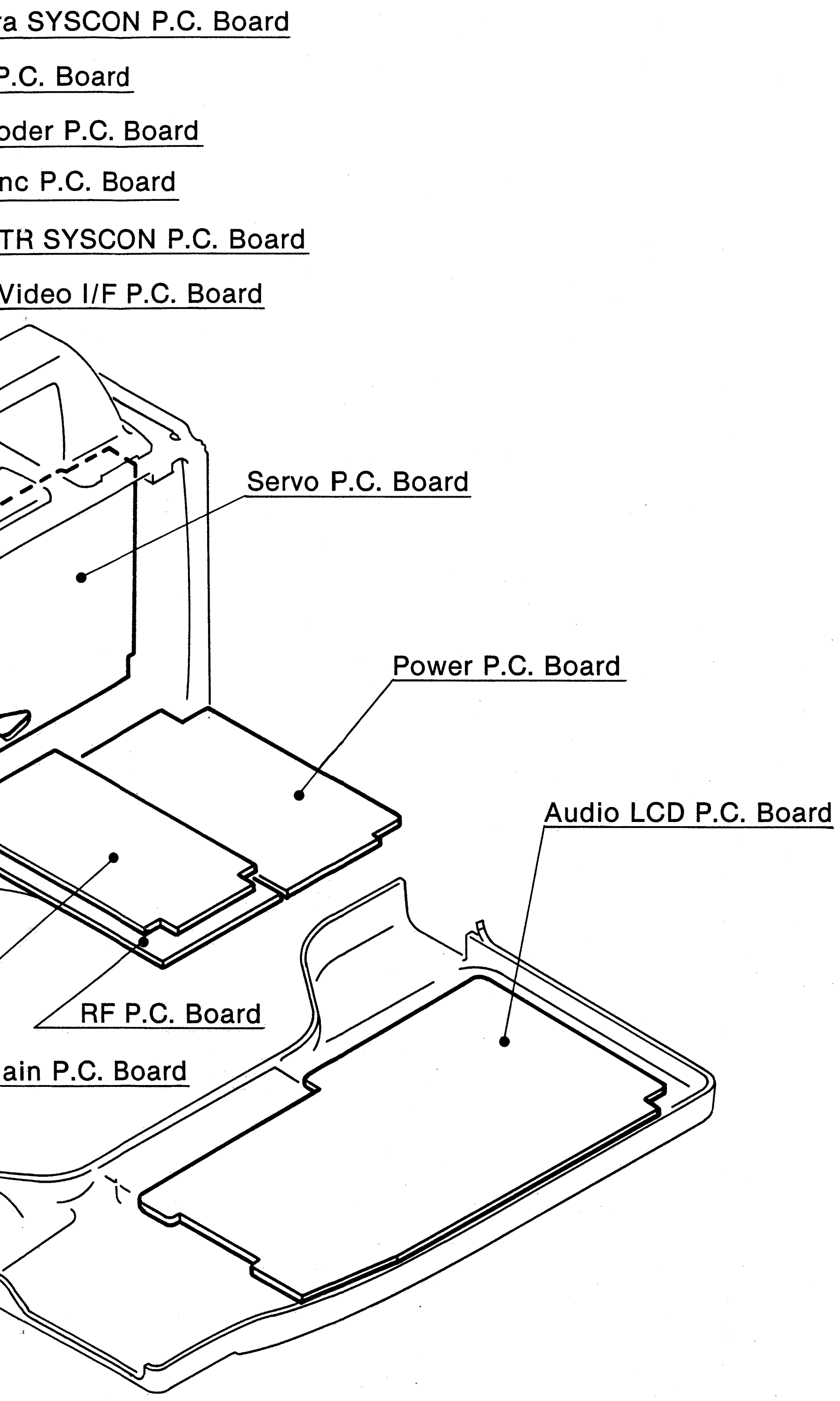
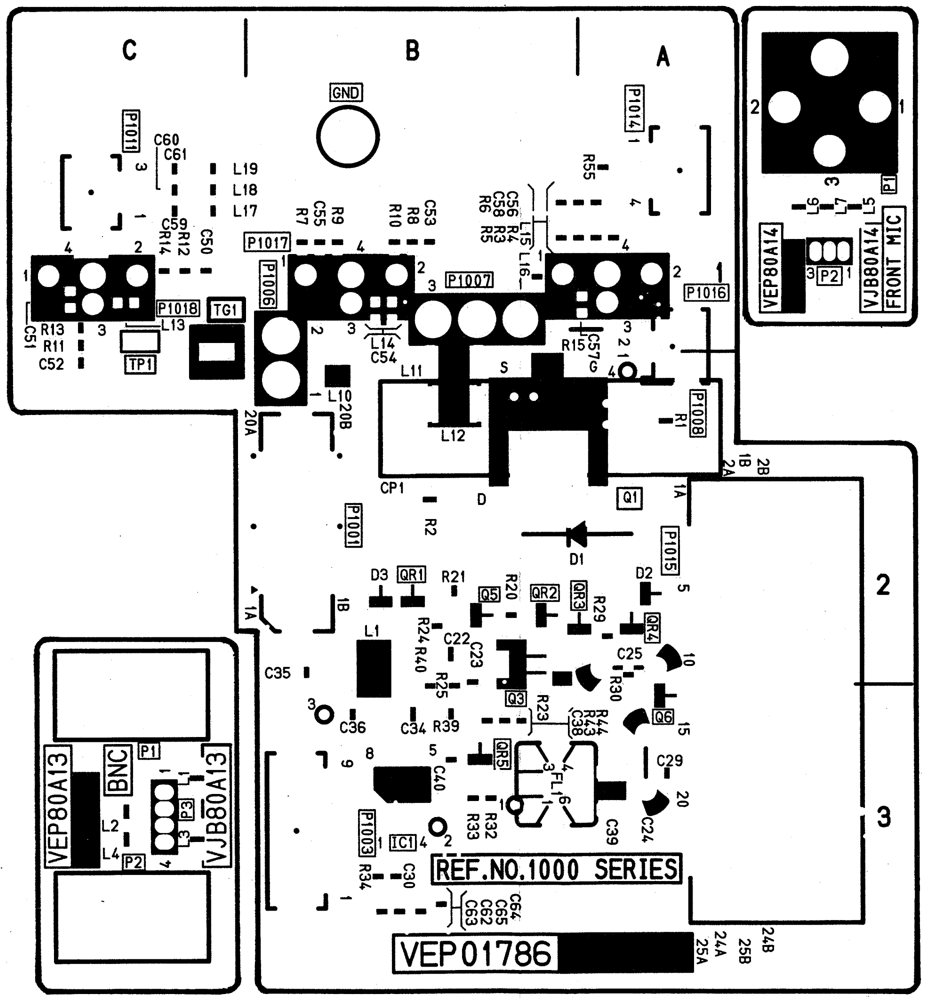
R7
C55
R9
R10
R8
C53
R6
C58
C56
R5
R3
R4
L15
L16
P1014
R55
P1018
TG1
P1006
P1007
P1016
R13
R11
C52
C51
L13
TP1
L14
C54
L11
R15
C57
G
S
L10
20B
20A
L12
P1008
R1
CP1
D
Q1
R2
P1001
D1
P1015
D3
QR1
R21
Q5
R20
QR2
QR3
R29
D2
QR4
1A
1B
2A
L1
R24
R40
C22
C23
C25
R30
C35
R25
Q3
C36
C34
R39
R23
C38
R43
R44
Q6
QR5
C40
FL1
C29
R32
R33
C39
C24
P1003
IC1
R34
C30
REF.NO.1000 SERIES
C64
C65
C62
C63
VEP01786
24A
25A
25B
VEP80A13
BNC
P1
P2
P3
L2
L4
L1
L3
VJB80A13

REAR JACK P.C. BOARD (VEP01786A) / BNC P.C. BOARD (VEP80A13A) / FRONT MIC P.C. BOARD (VEP80A14A)


a SYSCON P.C. Board
.C. Board
oder P.C. Board
nc P.C. Board
TR SYSCON P.C. Board
Video I/F P.C. Board
Servo P.C. Board
Power P.C. Board
Audio LCD P.C. Board
RF P.C. Board
ain P.C. Board

REAR JACK					
Transistors		**Integrated Circuits**		P1010	A-2 Ⓒ
Q1001	A-2 Ⓕ	IC1001	B-3 Ⓕ	P1011	C-1 Ⓕ
Q1002	B-2 Ⓒ	**Test Points**		P1012	B-3 Ⓒ
Q1003	B-2 Ⓕ	TP1001	C-1 Ⓕ	P1014	A-1 Ⓕ
Q1005	B-2 Ⓕ	TG1001	C-1 Ⓕ	P1015	A-3
Q1006	A-3 Ⓕ	**Adjustments**		P1016	A-1
Q1007	B-3 Ⓒ	VR1001	A-3 Ⓒ	P1017	B-1
Q1008	B-3 Ⓒ	VR1002	A-3 Ⓒ	P1018	C-1
Q1009	A-3 Ⓒ	**Connectors**			
Q1010	A-3 Ⓒ	P1001	B-2 Ⓒ		
Q1011	A-3 Ⓒ	P1003	B-3 Ⓕ		
Transistor-Resistors		P1004	B-3 Ⓒ		
QR1001	B-2 Ⓕ	P1006	B-1		
QR1002	B-2 Ⓕ	P1007	B-1		
QR1003	A-2 Ⓕ	P1008	A-2 Ⓕ		
QR1004	A-2 Ⓕ	P1009	B-2 Ⓒ		
QR1005	B-3 Ⓕ				
QR1006	A-3 Ⓒ				

ADDRESS INFORMATION
Ⓒ... COMPONENT SIDE
Ⓕ... FOIL SIDE


C
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P1011
P1014
P1017
P1007
P1016
P1018
TG1
TP1
P1006
P1008
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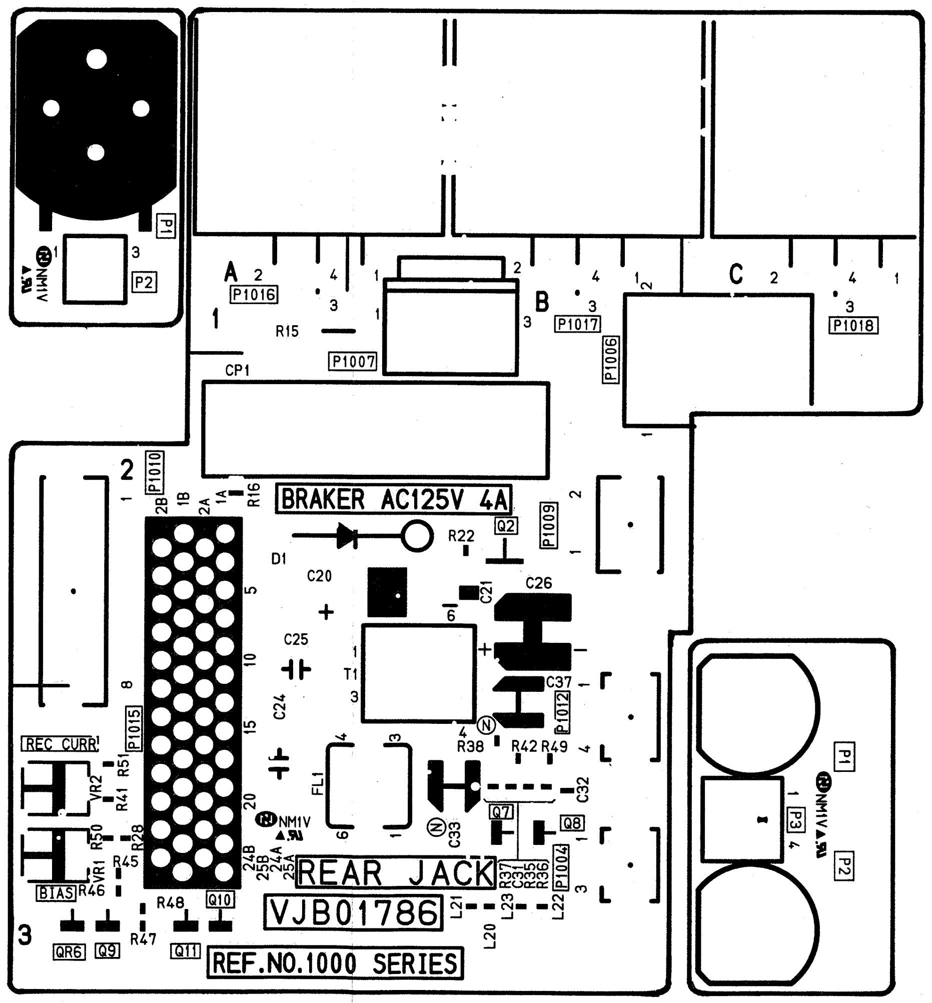
P1015
P1003
IC1
Q1
QR1
QR2
QR3
QR4
QR5
Q3
Q5
Q6
D1
D2
D3
L1
L12
FL1
CP1
VEP80A14
VJB80A14
FRONT MIC
P1
P2
VEP80A13
BNC
VJB80A13
P3
REF.NO.1000 SERIES
VEP01786
2
3

(FOIL SIDE)


A
B
C
P1016
P1017
P1018
P1007
P1006
P1010
P1009
P1015
P1012
P1004
CP1
R15
BRAKER AC125V 4A
Q2
Q7
Q8
Q10
Q11
QR6
Q9
T1
FL1
D1
REC CURR
BIAS
VR1
VR2
REAR JACK
VJB01786
REF.NO.1000 SERIES
P1
P2
P3
NM1V
2
3

(COMPONENT SIDE)

SECTION 4

IC INFORMATION

ICs INFORMATION

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74AC00SJ	7400	5
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74AC11SJ	7411	5
74AC138SJ	74138	6
74AC139SJ	74139	6
74AC32SJ	7432	9
74AC374SJ	74374	9
74AC574SJ	74574	10
74AC74SJ	7474	10
74AC86SJ	7486	10
74ALS245ASJ	74245	8
74ALS541SJ	74541	10
74F00SJ	7400	5
74F04SJ	7404	5
74F08SJ	7408	5
74F112SJ	74112	5
74F11SJ	7411	5
74F138SJ	74138	6
74F151ASJ	74151	7
74F157ASJ	74157	7
74F244SJ	74244	8
74F245SJ	74245	8
74F32SJ	7432	9
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74F573SJ	74573	10
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AD828AR	AD828AR	11
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AN3834K	AN3834S	15
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AN78N05	AN78N00	17
AN78N09	AN78N00	17
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GS9002CPM	GS9002	26
GS9005A-CPJ		
GS9007-CKA		
GS9010-CKC	GS9010	24
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NJM79L09UA	AN79L00	17
NJU7112AM		
OP177GS	OP177GS	47
PC74HC75T	7475	10
S80725ANDN	S80700AN	48
S80727ANDQ	S80700AN	48
S81350HG		
S8420BF		
SC371025VFU	SC371025VFU	48
SLA7220F5A		
SLA909SF1G	SLA909SF1G	49
SMP08FS	SMP08FS	49
SN74AS244NS	74244	8
SN74AS74NS	7474	10
SN74LS04NS	7404	5
SN74LS05NS	7405	5
SN74LS123NS	74123	6
SN74LS221NS	74221	8
SN74LS38NS	7438	9
SN74S1051NS	SN74S1051NS	50
SN74S1053NS		
SN75158P	SN75158PS	50
STK12C68S45T		
T160G11-1233		
T160G16-1220	T160G16-1220	50
T160G22-1225	T160G22-1225	53
T160G41-1437	T160G41-1437	54
T163G26-1018		
T163G26-1022		
T74HC191AF	T74HC191A	55
T74HCT374AF	T74HCT374A	56

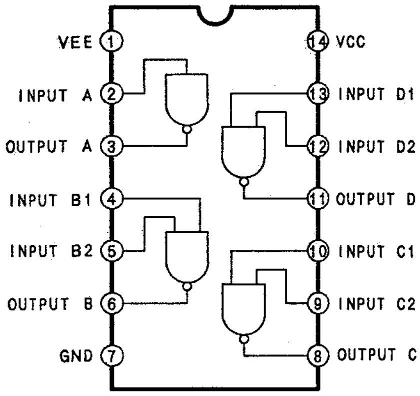
PART NO.	REF. NO.	REF. PAGE
T74HCT541AF	74541	10
T74LCX244F	74244	8
T74VHC00F	7400	5
T74VHC08F	7408	5
T74VHC157F	74157	7
T74VHC244F	74244	8
T74VHC245F	74245	8
T74VHC574F	74574	10
T74VHC74F	7474	10
T74VHCT244F	74244	8
T74VHCU04F	7404	5
TA75W01FU		
TA75W393FU		
TB6519F		
TC4S30F	TC4S30F	56
TC4S584F	TC4S584F	56
TC4S66F	TC4S66F	56
TC4S69F	TC4S69F	56
TC4S71F	TC7S32F	57
TC4W53F	TC4W53FU	56
TC4W53FU	TC4W53FU	56
TC4W66F	TC4W66F	56
TC74ACT541F	74541	10
TC7S00FU	TC7S00F	56
TC7S04F	TC7S04F	56
TC7S04FU	TC7S04F	56
TC7S08FU	TC7S08F	57
TC7S14F	TC7S14F	57
TC7S32F	TC7S32F	57
TC7S32FU	TC7S32F	57
TC7S32FU	TC7S32F	57
TC7S66F	TC7S66F	57
TC7S66FUTL	TC7S66F	57
TC7S86FUTL	TC7S86F	57
TC7SH00FU	TC7S00F	57
TC7SH04FU	TC7S04F	57
TC7SH08FU	TC7S08F	57
TC7SH32F	TC7S32F	57
TC7SH86FUTL	TC7S86F	57
TC7SU04F	TC7S04F	57
TC7W00F	TC7W00F	57
TC7W00FUTL	TC7W00F	57
TC7W02FU	TC7W02F	57
TC7W04F	TC7W04F	57
TC7W04FUTL	TC7W04F	57
TC7W08F	TC7W08F	57
TC7W08FUTL	TC7W08F	57
TC7W125FUTL	TC7W125FU	57
TC7W14FU	TC7W14F	57
TC7W32F	TC7W32F	57
TC7W32FU	TC7W32F	57
TC7W74F	TC7W74F	58
TC7W74FU	TC7W74F	58
TC7WU04F	TC7W04F	57
TCVHC04FS		

PART NO.	REF. NO.	REF. PAGE
TCVHC08FSEL		
TCVHC125FSEL		
TCVHC74FS		
TE7751	TE7751	59
TL084CNS	TL084	58
TL1451CDB	TL1451CNS	58
TL1451CNS	TL1451CNS	58
TL7705CPSB	TL7705	58
TLC549IPS	TLC548C/549C	58
TMP82C79F2	TMP82C79F2	61
TMPZ84C43AF6	TMPZ84C43AF6	60
TMS320C25PHL		
UPC1093J		
UPC1663G	UPC1663	61
UPC1862GS	UPC1862GS	62
UPC2384-GA		
UPC317H		
UPC319G2	UPC319	61
UPC339G2	UPC339	63
UPC393G2		
UPC4082G2	UPC4082	63
UPC4556G2	UPC4556	63
UPC4558G2	UPC4558	64
UPC4741G2	UPC4741	64
UPC5022GA089		
UPC5022GA121		
UPC5102GS030		
UPD16310GF	UPD16310GF	64
UPD16510GR		
UPD42101G-3	UPD42101G	63
UPD42102G-3	UPD42102G	63
UPD42280G3	UPD42280	65
UPD6456T611Y	UPD6456	66
UPD6486GF3BA	UPD6486GF	67
UPD65013BC16		
UPD65650J203		
UPD65845G039	UPD65845G039	68
UPD65868D022	UPD65868D022	69
UPD71055GB	UPD71055G	71
UPD75316BE58		
UPD75328G742		
UPD75P328		
VSI1997		
VSI2000		
VY06632		
VY06633		
XC62AP2302P	X62APXX02M	72
XC62AP3002ML	X62APXX02M	72
XC62AP3002P	X62APXX02M	72
XC62AP3002PL	X62APXX02M	72
XC62AP3202P		
XC62AP5002ML	X62APXX02M	72
XC62AP5002P	X62APXX02M	72
XC62DN3002ML	X62DNXX02M	72
XC62DN5002P	X62DNXX02M	72
XC62DP5002P	X62DNXX02M	72
Y7C19935VC	Y7C19935VC	72
Z84C4310FEC		

NOTE: The following ICs which are not described on the REF. PAGE, are not contained the IC Block drawing in this issue.

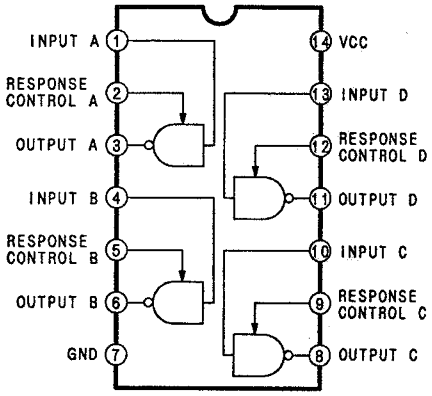
1488
(QUAD LINE (RS232C) DRIVER)

(TOP VIEW)

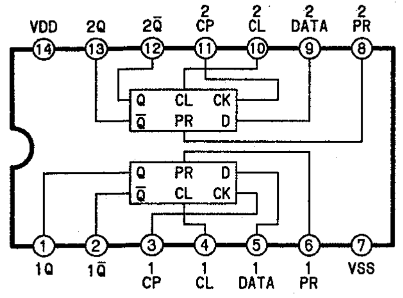

VEE 1
INPUT A 2
OUTPUT A 3
INPUT B1 4
INPUT B2 5
OUTPUT B 6
GND 7
14 VCC
13 INPUT D1
12 INPUT D2
11 OUTPUT D
10 INPUT C1
9 INPUT C2
8 OUTPUT C

1489
(QUAD LINE (RS232C) RECEIVER)

(TOP VIEW)


INPUT A 1
RESPONSE CONTROL A 2
OUTPUT A 3
INPUT B 4
RESPONSE CONTROL B 5
OUTPUT B 6
GND 7
14 VCC
13 INPUT D
12 RESPONSE CONTROL D
11 OUTPUT D
10 INPUT C
9 RESPONSE CONTROL C
8 OUTPUT C

4013
(DUAL D-TYPE FLIP-FLOP)


VDD 14
2Q 13
2Q̄ 12
2 CP 11
2 CL 10
2 DATA 9
2 PR 8
Q CL CK
Q̄ PR D
Q PR D
Q̄ CL CK
1 1Q
2 1Q̄
3 1 CP
4 1 CL
5 1 DATA
6 1 PR
7 VSS

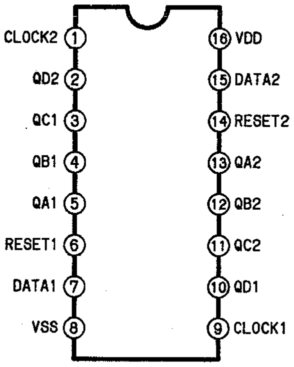
TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK↑	DATA	RESET	SET	Q	$\bar{Q}$	
↑	0	0	0	0	1	
↑	1	0	0	1	0	
↓	×	0	0	Q	$\bar{Q}$	NO CHANGE
×	×	1	0	0	1	
×	×	0	1	1	0	
×	×	1	1	1	1	

X=DON'T CARE
↑=LEVEL CHANGE

4015
(DUAL 4-STAGE SHIFT REGISTER)

(TOP VIEW)


CLOCK2 1
QD2 2
QC1 3
QB1 4
QA1 5
RESET1 6
DATA1 7
VSS 8
16 VDD
15 DATA2
14 RESET2
13 QA2
12 QB2
11 QC2
10 QD1
9 CLOCK1

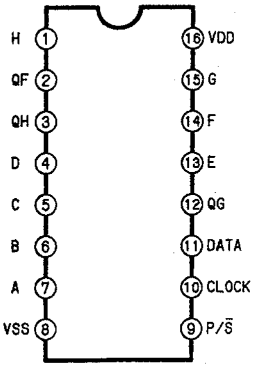
TRUTH TABLE

CL▲	D	R	Q1	QN
↑	0	0	0	QN-1
↑	1	0	1	QN-1
↓	×	0	Q1	QN (NO CHANGE)
×	×	1	0	0

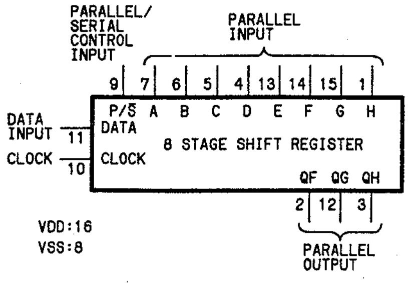
▲ LEVEL CHANGE
× DON'T CARE CASE

4021
(8-STAGE STATIC SHIFT REGISTER)

(TOP VIEW)


H 1
QF 2
QH 3
D 4
C 5
B 6
A 7
VSS 8
16 VDD
15 G
14 F
13 E
12 QG
11 DATA
10 CLOCK
9 P/S̄

BLOCK DIAGRAM


PARALLEL/ SERIAL CONTROL INPUT
PARALLEL INPUT
9
7
6
5
4
13
14
15
1
P/S̄
A
B
C
D
E
F
G
H
DATA INPUT
11
DATA
8 STAGE SHIFT REGISTER
CLOCK
10
CLOCK
QF
QG
QH
2
12
3
VDD:16
VSS:8
PARALLEL OUTPUT

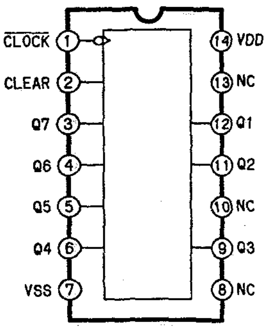
TRUTH TABLE

CL▲	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PL-1	PL-N	Q1 (INTERNAL)	QN	
×	×	1	0	0	0	0	
×	×	1	0	1	0	1	
×	×	1	1	0	1	0	
×	×	1	1	1	1	1	
↑	0	0	×	×	0	QN-1	
↑	1	0	×	×	1	QN-1	
↓	×	0	×	×	Q1	QN	NC

▲-LEVEL CHANGE × -DON'T CARE CASE

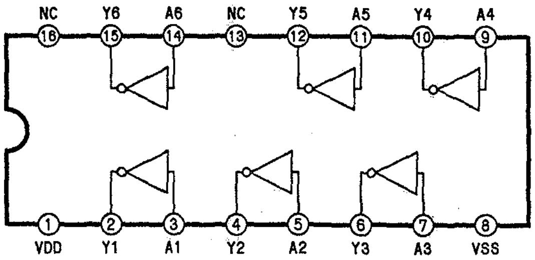
4024
(7-STAGE BINARY RIPPLE COUNTER)

(TOP VIEW)


$\overline{\text{CLOCK}}$ 1
CLEAR 2
Q7 3
Q6 4
Q5 5
Q4 6
VSS 7
14 VDD
13 NC
12 Q1
11 Q2
10 NC
9 Q3
8 NC

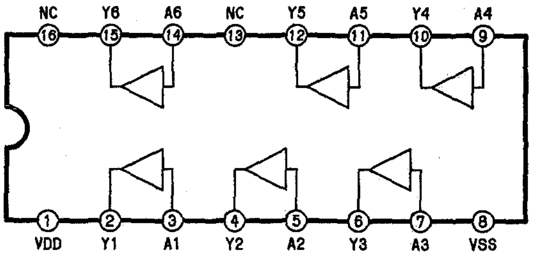
4049
(HEX.INVERTING BUFFER/CONVERTER)

(TOP VIEW)


NC 16
Y6 15
A6 14
NC 13
Y5 12
A5 11
Y4 10
A4 9
VDD 1
Y1 2
A1 3
Y2 4
A2 5
Y3 6
A3 7
VSS 8

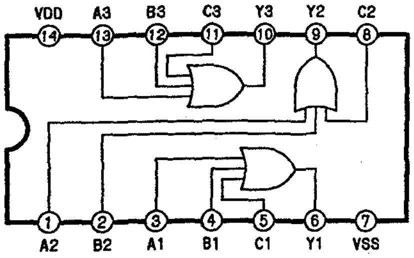
4050
(HEX.BUFFER/CONVERTER)

(TOP VIEW)

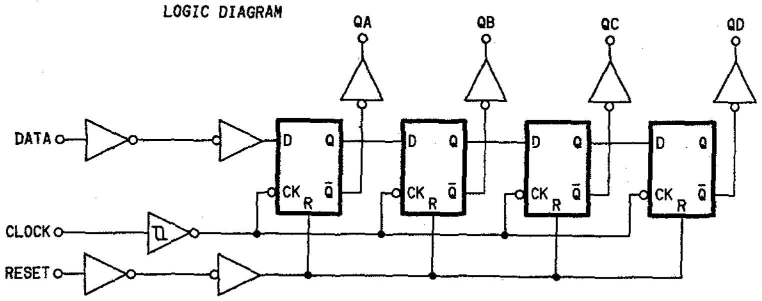

NC 16
Y6 15
A6 14
NC 13
Y5 12
A5 11
Y4 10
A4 9
VDD 1
Y1 2
A1 3
Y2 4
A2 5
Y3 6
A3 7
VSS 8

4075
(TRIPLE 3-INPUT OR GATE)

(TOP VIEW)

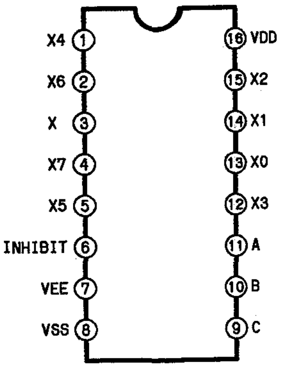

VDD 14
A3 13
B3 12
C3 11
Y3 10
Y2 9
C2 8
A2 1
B2 2
A1 3
B1 4
C1 5
Y1 6
VSS 7

LOGIC DIAGRAM


QA
QB
QC
QD
DATA
CLOCK
RESET
D
Q
CK
R
$\overline{Q}$

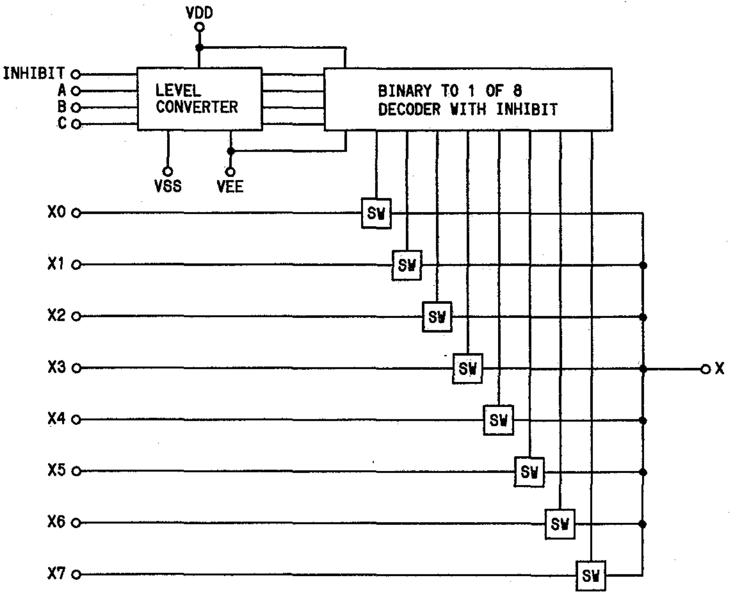
4051
(SINGLE 8-CHANNEL MULTIPLEXER/DEMULTIPLEXER)

(TOP VIEW)


X4 ①
X6 ②
X ③
X7 ④
X5 ⑤
INHIBIT ⑥
VEE ⑦
VSS ⑧
⑯ VDD
⑮ X2
⑭ X1
⑬ X0
⑫ X3
⑪ A
⑩ B
⑨ C

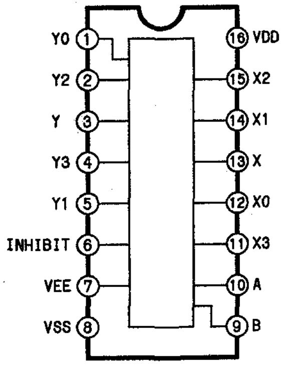
TRUTH TABLE

INPUT STATES				"ON"CHANNEL(S)
INHIBIT	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	×	×	×	NONE


VDD
INHIBIT
A
B
C
LEVEL CONVERTER
BINARY TO 1 OF 8 DECODER WITH INHIBIT
VSS
VEE
X0
X1
X2
X3
X4
X5
X6
X7
SW
X

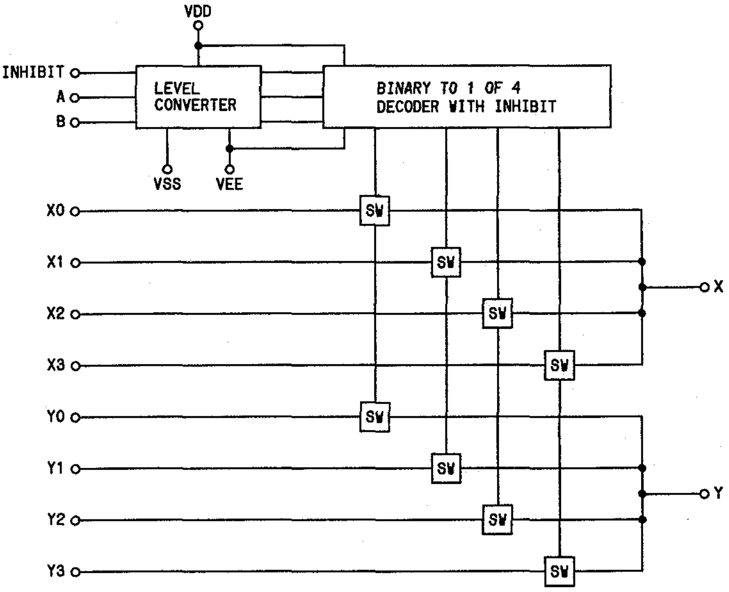
4052
(DIFFERENTIAL 4-CHANNEL MULTIPLEXER/DEMULTIPLEXER)

(TOP VIEW)


Y0 ①
Y2 ②
Y ③
Y3 ④
Y1 ⑤
INHIBIT ⑥
VEE ⑦
VSS ⑧
⑯ VDD
⑮ X2
⑭ X1
⑬ X
⑫ X0
⑪ X3
⑩ A
⑨ B

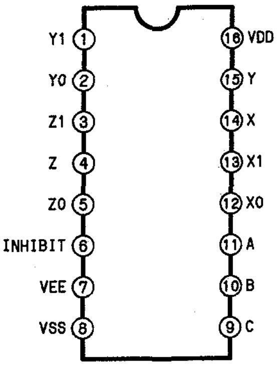
TRUTH TABLE

INPUT STATES			"ON"CHANNEL(S)
INHIBIT	B	A	
0	0	0	X0, Y0
0	0	1	X1, Y1
0	1	0	X2, Y2
0	1	1	X3, Y3
1	×	×	NONE


VDD
INHIBIT
A
B
LEVEL CONVERTER
BINARY TO 1 OF 4 DECODER WITH INHIBIT
VSS
VEE
X0
X1
X2
X3
Y0
Y1
Y2
Y3
SW
X
Y

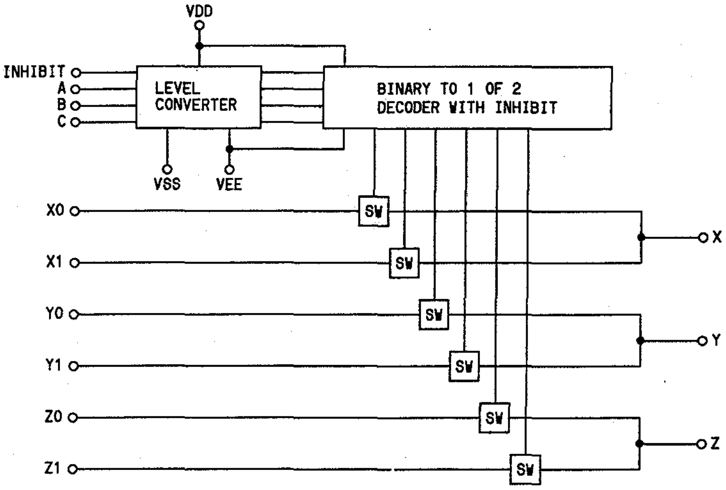
4053
(TRIPLE 2-CHANNEL MULTIPLEXER/DEMULTIPLEXER)

(TOP VIEW)

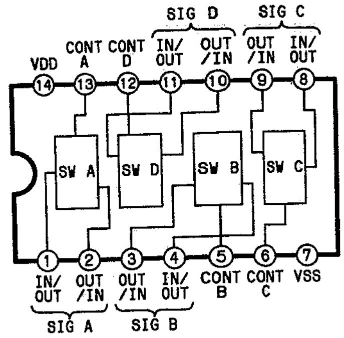

Y1 ①
Y0 ②
Z1 ③
Z ④
Z0 ⑤
INHIBIT ⑥
VEE ⑦
VSS ⑧
⑯ VDD
⑮ Y
⑭ X
⑬ X1
⑫ X0
⑪ A
⑩ B
⑨ C

TRUTH TABLE

INPUT STATES				"ON"CHANNEL(S)
INHIBIT	C	B	A	
0	0	0	0	X0, Y0, Z0
0	0	0	1	X1, Y1, Z1
1	×	×	×	NONE


VDD
INHIBIT
A
B
C
LEVEL CONVERTER
BINARY TO 1 OF 2 DECODER WITH INHIBIT
VSS
VEE
X0
X1
Y0
Y1
Z0
Z1
SW
X
Y
Z

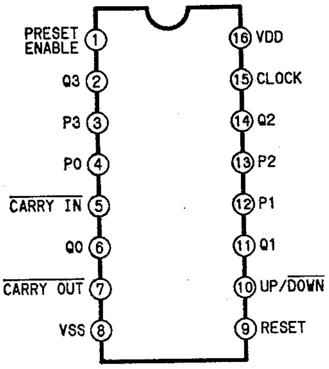
4066
(QUAD BILATERAL SWITCH)
(TOP VIEW)


SIG D
SIG C
VDD
CONT A
CONT D
IN/ OUT
OUT /IN
OUT /IN
IN/ OUT
14
13
12
11
10
9
8
SW A
SW D
SW B
SW C
1
2
3
4
5
6
7
IN/ OUT
OUT /IN
OUT /IN
IN/ OUT
CONT B
CONT C
VSS
SIG A
SIG B

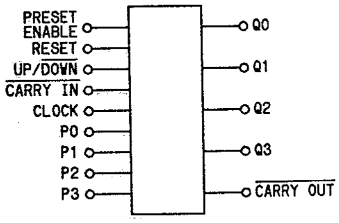
TRUTH TABLE

CONTROL	SWITCH
H	ON
L	OFF

4516
(4-BIT UP/DOWN BINARY COUNTER)
(TOP VIEW)


PRESET ENABLE 1
Q3 2
P3 3
P0 4
$\overline{\text{CARRY IN}}$ 5
Q0 6
$\overline{\text{CARRY OUT}}$ 7
VSS 8
16 VDD
15 CLOCK
14 Q2
13 P2
12 P1
11 Q1
10 UP/$\overline{\text{DOWN}}$
9 RESET

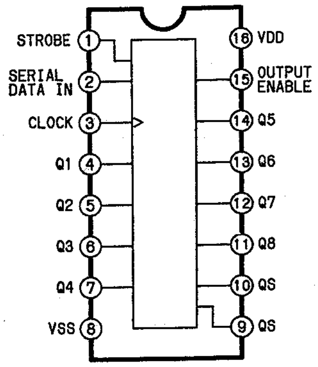
BLOCK DIAGRAM


PRESET ENABLE
RESET
UP/$\overline{\text{DOWN}}$
$\overline{\text{CARRY IN}}$
CLOCK
P0
P1
P2
P3
Q0
Q1
Q2
Q3
$\overline{\text{CARRY OUT}}$

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/$\overline{\text{DOWN}}$	PRESET ENABLE	RESET	ACTION
H	×	L	L	NO COUNT
L	H	L	L	COUNT UP
L	L	L	L	COUNT DOWN
×	×	H	L	PRESET
×	×	×	H	RESET

4094
(8-STAGE SHIFT/STORE BUS REGISTER)
(TOP VIEW)

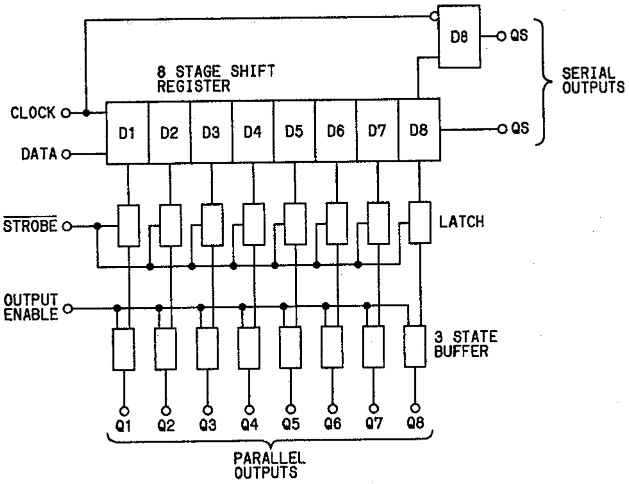

STROBE 1
SERIAL DATA IN 2
CLOCK 3
Q1 4
Q2 5
Q3 6
Q4 7
VSS 8
16 VDD
15 OUTPUT ENABLE
14 Q5
13 Q6
12 Q7
11 Q8
10 QS
9 QS

TRUTH TABLE

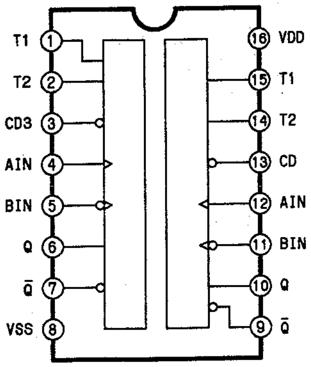
CL▲	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS		SERIAL OUTPUTS	
				Q1	QN	QS	Q'S
↑	0	×	×	OC	OC	Q7	NC
↓	0	×	×	OC	OC	NC	Q7
↑	1	0	×	NC	NC	Q7	NC
↑	1	1	0	0	QN-1	Q7	NC
↑	1	1	1	1	QN-1	Q7	NC
↓	1	1	1	NC	NC	NC	Q7

▲-LEVEL CHANGE ×-DON'T CARE CASE

BLOCK DIAGRAM


D8
QS
SERIAL OUTPUTS
8 STAGE SHIFT REGISTER
CLOCK
DATA
D1
D2
D3
D4
D5
D6
D7
D8
QS
$\overline{\text{STROBE}}$
LATCH
OUTPUT ENABLE
3 STATE BUFFER
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
PARALLEL OUTPUTS

4538
(DUAL PRECISION MONOSTABLE MULTIVIBRATOR)
(TOP VIEW)


T1 1
T2 2
CD3 3
AIN 4
BIN 5
Q 6
$\overline{Q}$ 7
VSS 8
16 VDD
15 T1
14 T2
13 CD
12 AIN
11 BIN
10 Q
9 $\overline{Q}$

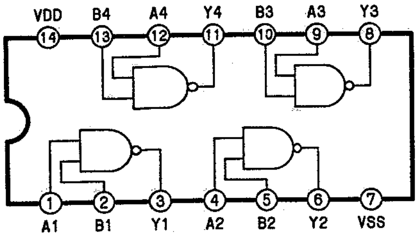
TRUTH TABLE

INPUT			OUTPUT	
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$
↑	H	H	⊓	⊔
↑	L	H	Q	$\overline{Q}$
H	↓	H	Q	$\overline{Q}$
L	↓	H	⊓	⊔
×	×	L	L	H

7400

(QUAD 2-INPUT NAND GATE)

(TOP VIEW)


VDD
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
VSS

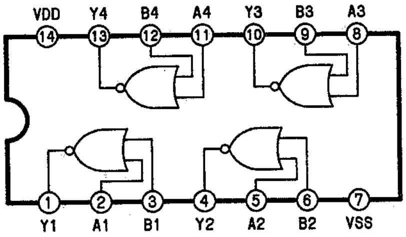
TRUTH TABLE (74HC)

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

7402

(QUAD 2-INPUT NOR GATE)

(TOP VIEW)


VDD
Y4
B4
A4
Y3
B3
A3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
Y1
A1
B1
Y2
A2
B2
VSS

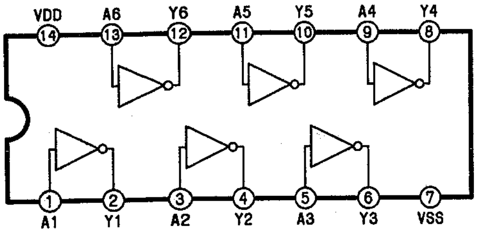
TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

7404

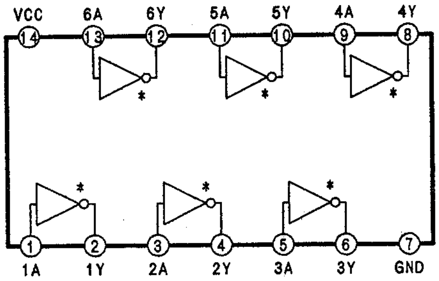
(HEX.INVERTER)

(TOP VIEW)


VDD
A6
Y6
A5
Y5
A4
Y4
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
Y1
A2
Y2
A3
Y3
VSS

7405

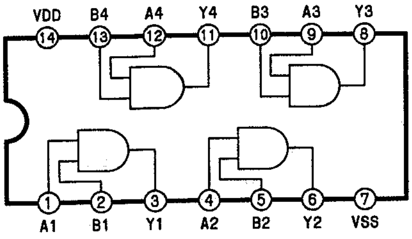
(HEX O. C. INVERTER)


VCC
6A
6Y
5A
5Y
4A
4Y
14
13
12
11
10
9
8
*
*
*
*
*
*
1
2
3
4
5
6
7
1A
1Y
2A
2Y
3A
3Y
GND

7408

(QUAD 2-INPUT AND GATE)

(TOP VIEW)

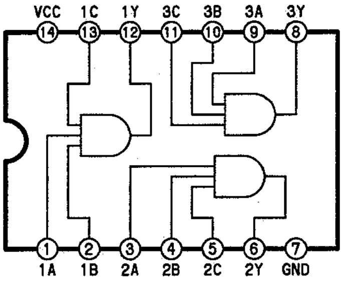

VDD
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
VSS

TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

7411

(TRIPLE 3-INPUT AND GATE)

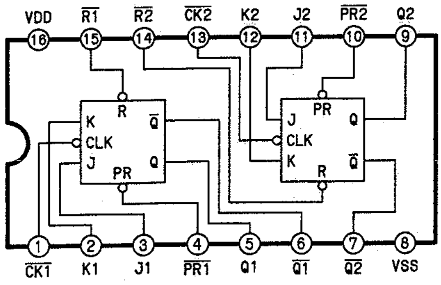

VCC
1C
1Y
3C
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
2A
2B
2C
2Y
GND

Y=A.B.C

74112

(DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR)

(TOP VIEW)


VDD
$\overline{R1}$
$\overline{R2}$
$\overline{CK2}$
K2
J2
$\overline{PR2}$
Q2
16
15
14
13
12
11
10
9
K
R
$\overline{Q}$
CLK
J
PR
Q
J
PR
Q
CLK
K
R
$\overline{Q}$
1
2
3
4
5
6
7
8
$\overline{CK1}$
K1
J1
$\overline{PR1}$
Q1
$\overline{Q1}$
$\overline{Q2}$
VSS

CLK:CLOCK
$\overline{PR}$:$\overline{PRESET}$
$\overline{R}$:$\overline{RESET}$

TRUTH TABLE (74HC112)

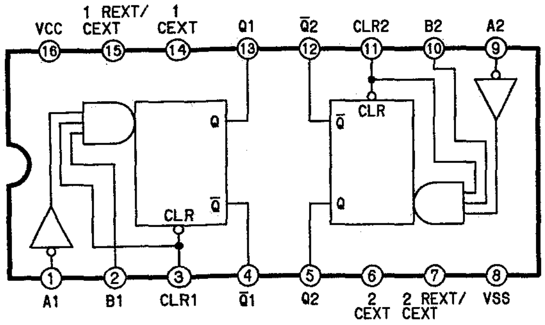
INPUTS					OUTPUTS	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	×	×	Q0	$\overline{Q}$0

* :UNSTABLE

74123

(DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR)

(TOP VIEW)


VCC
1 REXT/ CEXT
1 CEXT
Q1
Q̄2
CLR2
B2
A2
16
15
14
13
12
11
10
9
Q
CLR
Q̄
Q̄
CLR
Q
1
2
3
4
5
6
7
8
A1
B1
CLR1
Q̄1
Q2
2 CEXT
2 REXT/ CEXT
VSS

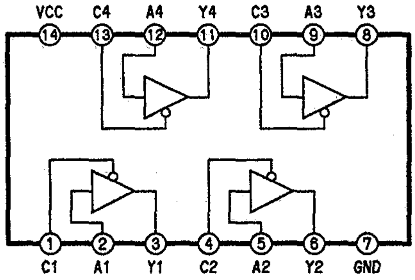
TRUTH TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	×	×	L	H
×	H	×	L	H
×	×	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

74125

(3 STATE QUAD BUFFER)

(TOP VIEW)


VCC
C4
A4
Y4
C3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
C1
A1
Y1
C2
A2
Y2
GND

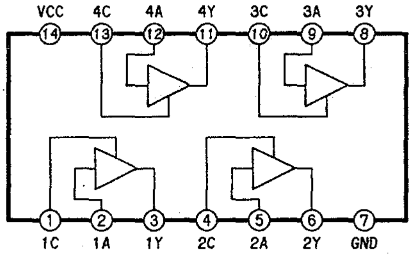
TRUTH TABLE

INPUTS		OUTPUT
A	C	Y
H	L	H
L	L	L
X	H	Z

74126

(QUAD 3 STATE BUS BUFFERS)

(TOP VIEW)


VCC
4C
4A
4Y
3C
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1C
1A
1Y
2C
2A
2Y
GND

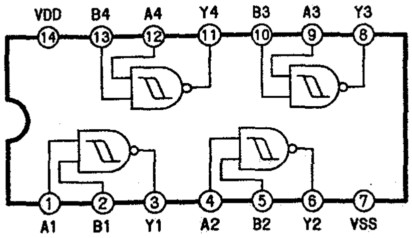
TRUTH TABLE

INPUTS		OUTPUTS
A	C	Y
H	H	H
L	H	L
X	L	Z

74132

(QUAD 2-INPUT NAND SCHMITT TRIGGER)

(TOP VIEW)


VDD
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
VSS

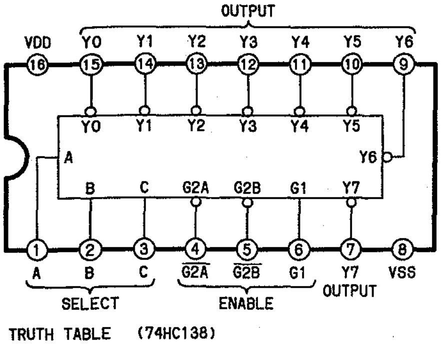
TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

74138

(3-TO-8 LINE DECODER)

(TOP VIEW)


OUTPUT
VDD
Y0
Y1
Y2
Y3
Y4
Y5
Y6
16
15
14
13
12
11
10
9
Y0
Y1
Y2
Y3
Y4
Y5
A
Y6
B
C
G2A
G2B
G1
Y7
1
2
3
4
5
6
7
8
A
B
C
G̅2̅A̅
G̅2̅B̅
G1
Y7
VSS
SELECT
ENABLE
OUTPUT

TRUTH TABLE (74HC138)

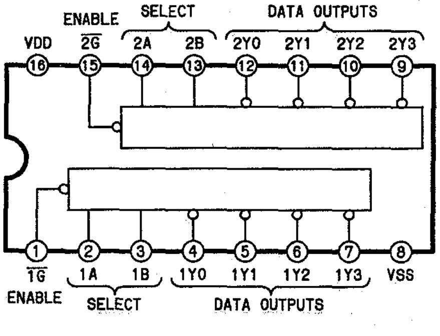
INPUTS			OUTPUTS							
ENABLE		SELECT								
G1	$\overline{G2}$•	C B A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
×	H	× × ×	H	H	H	H	H	H	H	H
L	×	× × ×	H	H	H	H	H	H	H	H
H	L	L L L	L	H	H	H	H	H	H	H
H	L	L L H	H	L	H	H	H	H	H	H
H	L	L H L	H	H	L	H	H	H	H	H
H	L	L H H	H	H	H	L	H	H	H	H
H	L	H L L	H	H	H	H	L	H	H	H
H	L	H L H	H	H	H	H	H	L	H	H
H	L	H H L	H	H	H	H	H	H	L	H
H	L	H H H	H	H	H	H	H	H	H	L

• $\overline{G2}=\overline{G2A}+\overline{G2B}$

74139

(DUAL 2-TO-4 LINE DECODER)

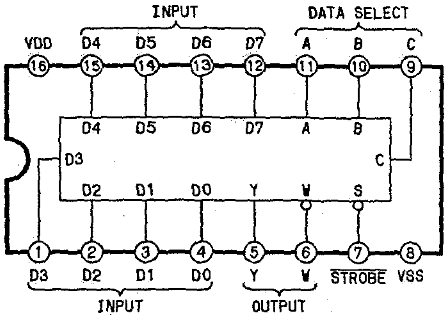
(TOP VIEW)


ENABLE
SELECT
DATA OUTPUTS
VDD
2̅G̅
2A
2B
2Y0
2Y1
2Y2
2Y3
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
1̅G̅
1A
1B
1Y0
1Y1
1Y2
1Y3
VSS
ENABLE
SELECT
DATA OUTPUTS

TRUTH TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	×	×	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

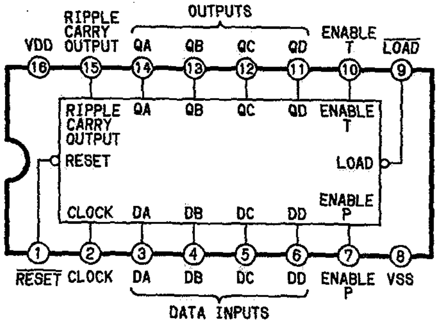
74151
(8-CHANNEL DIGITAL MULTIPLEXER)
(TOP VIEW)


INPUT
DATA SELECT
VDD
D4
D5
D6
D7
A
B
C
16
15
14
13
12
11
10
9
D3
D2
D1
D0
Y
W
S
1
2
3
4
5
6
7
8
STROBE
VSS
OUTPUT

TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

74161
(4-BIT SYNCHRONOUS BINARY COUNTER)
(TOP VIEW)


RIPPLE CARRY OUTPUT
OUTPUTS
ENABLE T
LOAD
VDD
QA
QB
QC
QD
16
15
14
13
12
11
10
9
RESET
CLOCK
DA
DB
DC
DD
ENABLE P
1
2
3
4
5
6
7
8
VSS
DATA INPUTS

TRUTH TABLE (74HC160/74HC161)

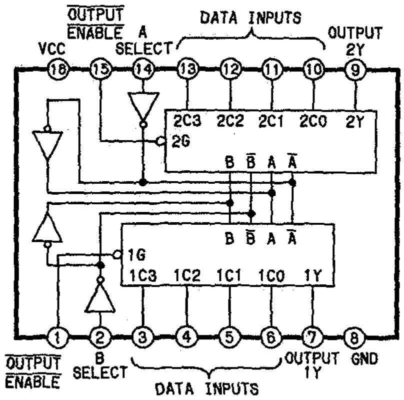
INPUT					OUTPUT
CLOCK	$\overline{\text{RESET}}$	$\overline{\text{LOAD}}$	ENABLE P	ENABLE T	Qn
X	L	X	X	X	L
↑	H	L	X	X	LOAD
↑	H	H	H	H	COUNT
X	H	H	L	X	NO COUNT
X	H	H	X	L	NO COUNT

H:HIGH L:LOW X:H or L
n:A~D

FUNCTION TABLE (74161)

INPUT					OUTPUT		FUNCTION
CLEAR	LOAD	CK	ENABLE P	ENABLE T	QA QB QC QD	RIPPLE CARRY	
H	H	↑	H	H		—	COUNT
H	L		X	X	DA DB DC DD	—	DATA SET
L	X	X	X	X	L L L L	—	CLEAR
H	X	X	X	H	H H H H	H	—

74153
(DUAL 4 TO 1 DATA SELECTORS)
(TOP VIEW)


OUTPUT ENABLE
A SELECT
DATA INPUTS
OUTPUT 2Y
VCC
16
15
14
13
12
11
10
9
2C3
2C2
2C1
2C0
2Y
2G
B
$\overline{B}$
A
$\overline{A}$
1G
1C3
1C2
1C1
1C0
1Y
1
2
3
4
5
6
7
8
OUTPUT ENABLE
B SELECT
DATA INPUTS
OUTPUT 1Y
GND

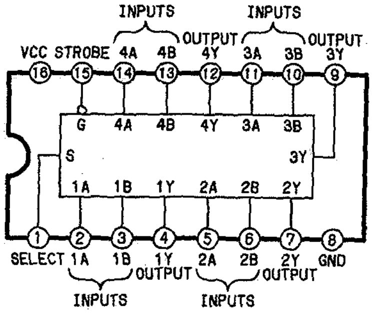
TRUTH TABLE

INPUT			OUTPUT
SELECT		$\overline{\text{OUTPUT ENABLE}}$	Y
B	A		
X	X	H	L
L	L	L	C0
L	H	L	C1
H	L	L	C2
H	H	L	C3

H:HIGH L:LOW X:H or L

74157.74158
(QUAD 2-INPUT MULTIPLEXER)

(TOP VIEW)

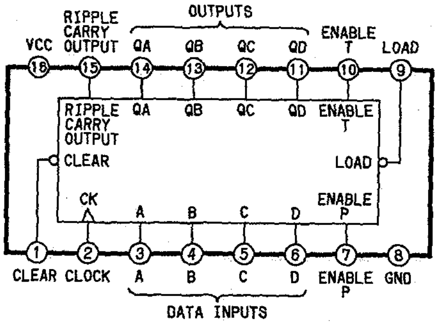

INPUTS
OUTPUT
INPUTS
OUTPUT
VCC
STROBE
4A
4B
4Y
3A
3B
3Y
16
15
14
13
12
11
10
9
G
S
1A
1B
1Y
2A
2B
2Y
1
2
3
4
5
6
7
8
SELECT
GND
OUTPUT
INPUTS

TRUTH TABLE (74HC157)

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	HC157	HC158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

74163
(4-BIT SYNCHRONOUS BINARY COUNTER WITH SYNCHRONOUS CLEAR)

(TOP VIEW)

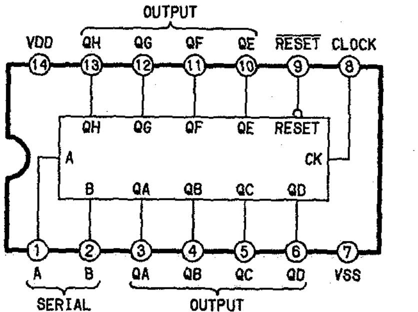

RIPPLE CARRY OUTPUT
OUTPUTS
ENABLE T
LOAD
VCC
QA
QB
QC
QD
16
15
14
13
12
11
10
9
CLEAR
CK
A
B
C
D
ENABLE P
1
2
3
4
5
6
7
8
CLOCK
GND
DATA INPUTS

TRUTH TABLE

CLK	CLR	ENP	ENT	LOAD	FUNCTION
↑	L	X	X	X	CLEAR
X	H	H	L	H	COUNT & RC DISABLED
X	H	L	H	H	COUNT DISABLED
X	H	L	L	H	COUNT & RC DISABLED
↑	H	X	X	L	LOAD
↑	H	H	H	H	INCREMENT COUNTER

74164
(8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER)

(TOP VIEW)


OUTPUT
VDD
QH
QG
QF
QE
RESET
CLOCK
14
13
12
11
10
9
8
A
B
QA
QB
QC
QD
CK
1
2
3
4
5
6
7
VSS
SERIAL INPUT
OUTPUT

TRUTH TABLE (74HC164)

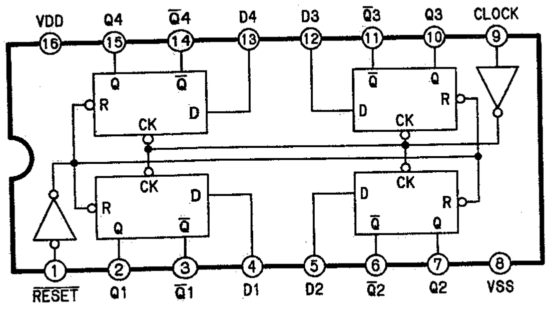
INPUT				OUTPUT		
$\overline{\text{RESET}}$	CLOCK	A	B	QA	QB	QH
L	X	X	X	L	L	L
H	↓	X	X	NO CHANGE		
H	↑	L	X	L	QA	QG
H	↑	X	L	L	QA	QG
H	↑	H	H	H	QA	QG

H:HIGH L:LOW X:H or L

74175

(QUAD D-TYPE FLIP-FLOP WITH CLEAR)

(TOP VIEW)


VDD
Q4
$\overline{Q4}$
D4
D3
$\overline{Q3}$
Q3
CLOCK
16
15
14
13
12
11
10
9
Q
$\overline{Q}$
R
D
CK
1
2
3
4
5
6
7
8
$\overline{RESET}$
Q1
$\overline{Q1}$
D1
D2
$\overline{Q2}$
Q2
VSS

TRUTH TABLE (74HC175)

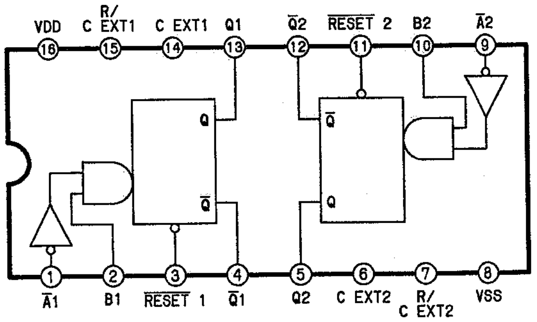
INPUT			OUTPUT	
CLOCK	$\overline{RESET}$	D	Q	$\overline{Q}$
×	L	×	L	H
↑	H	H	H	L
↑	H	L	L	H
L	H	×	NO CHANGE	

H:HIGH L:LOW X:H or L

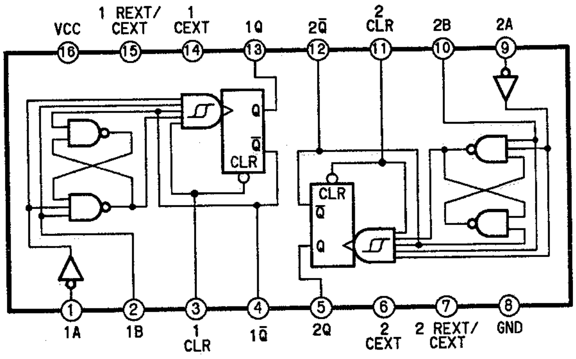
74221

(DUAL NON-RETRIGGERABLE MONOSTABLE MULTIVIBRATOR)

(TOP VIEW)


VDD
R/ C EXT1
C EXT1
Q1
$\overline{Q2}$
$\overline{RESET}$ 2
B2
$\overline{A2}$
16
15
14
13
12
11
10
9
Q
$\overline{Q}$
1
2
3
4
5
6
7
8
$\overline{A1}$
B1
$\overline{RESET}$ 1
$\overline{Q1}$
Q2
C EXT2
R/ C EXT2
VSS

(74HC221)


VCC
1 REXT/ CEXT
1 CEXT
1Q
2$\overline{Q}$
2 CLR
2B
2A
16
15
14
13
12
11
10
9
Q
$\overline{Q}$
CLR
1
2
3
4
5
6
7
8
1A
1B
1 CLR
1$\overline{Q}$
2Q
2 CEXT
2 REXT/ CEXT
GND

(74221)

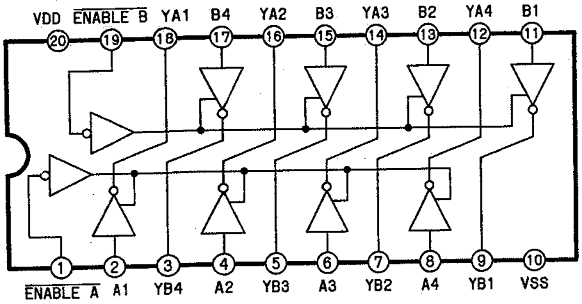
TRUTH TABLE (74HC221)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	×	×	L	H
×	H	×	L	H
×	×	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

74240

(INVERTING OCTAL 3-STATE BUFFER)

(TOP VIEW)


VDD
$\overline{ENABLE\ B}$
YA1
B4
YA2
B3
YA3
B2
YA4
B1
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
$\overline{ENABLE\ A}$
A1
YB4
A2
YB3
A3
YB2
A4
YB1
VSS

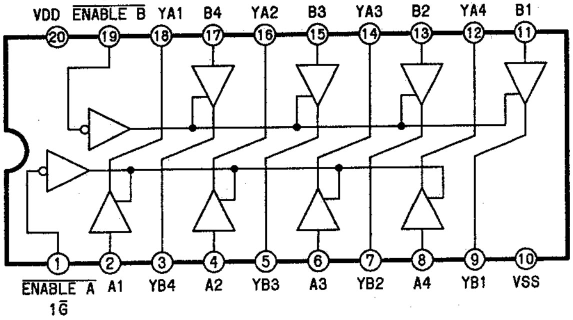
TRUTH TABLE (74HC240)

1$\overline{G}$	1A	1Y	2$\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

74244

(OCTAL 3-STATE BUFFER)

(TOP VIEW)

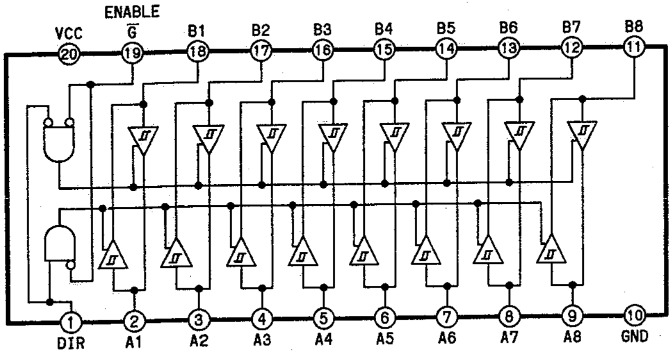

2$\overline{G}$
VDD
$\overline{ENABLE\ B}$
YA1
B4
YA2
B3
YA3
B2
YA4
B1
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
$\overline{ENABLE\ A}$
1$\overline{G}$
A1
YB4
A2
YB3
A3
YB2
A4
YB1
VSS

TRUTH TABLE (74HC244)

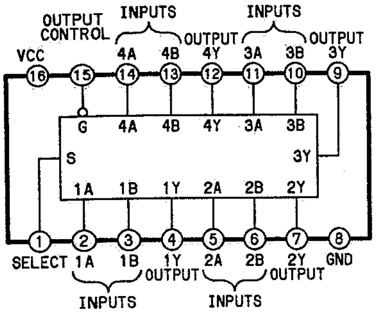
1$\overline{G}$	1A	1Y	2$\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

74245

(OCTAL 3-STATE BUS TRANSCEIVERS)


ENABLE $\overline{G}$
VCC
B1
B2
B3
B4
B5
B6
B7
B8
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
DIR
A1
A2
A3
A4
A5
A6
A7
A8
GND

74257
(QUAD 2-CHANNEL 3-STATE MULTIPLEXER)


OUTPUT CONTROL
INPUTS
OUTPUT
INPUTS
OUTPUT
VCC
4A
4B
4Y
3A
3B
3Y
16
15
14
13
12
11
10
9
G
4A
4B
4Y
3A
3B
S
3Y
1A
1B
1Y
2A
2B
2Y
1
2
3
4
5
6
7
8
SELECT
1A
1B
1Y
2A
2B
2Y
GND
OUTPUT
OUTPUT
INPUTS
INPUTS

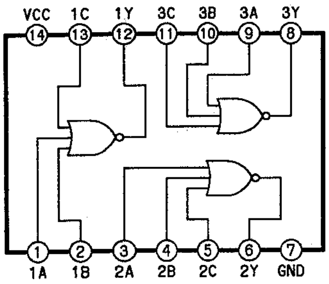
FUNCTION TABLE (74257)

INPUTS		OUTPUT Y
SELECT	OUTPUT CONTROL	
X	H	Z
L	L	A
H	L	B

TRUTH TABLE (74HC257)

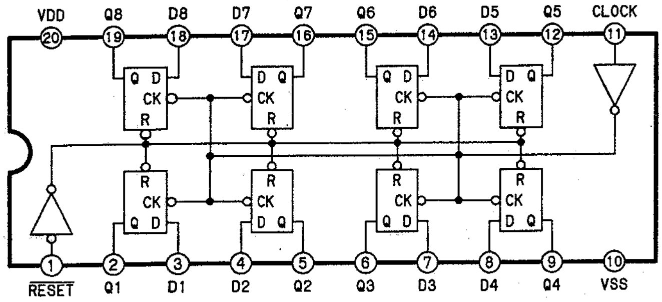
INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	×	×	×	Z
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H

7427
(TRIPLE 3-INPUT NOR GATE)


VCC
1C
1Y
3C
3B
3A
3Y
14
13
12
11
10
9
8
1
2
3
4
5
6
7
1A
1B
2A
2B
2C
2Y
GND

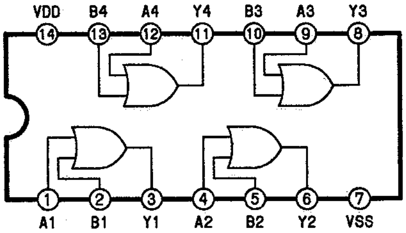
74273
(OCTAL D-TYPE FLIP-FLOP WITH CLEAR)

(TOP VIEW)

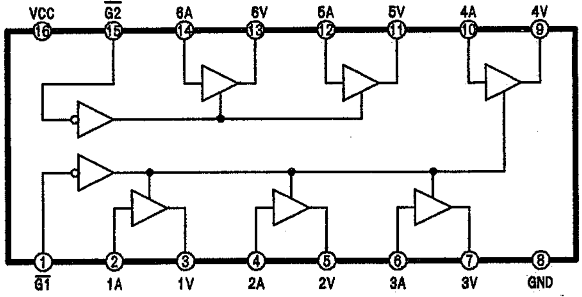

VDD
Q8
D8
D7
Q7
Q6
D6
D5
Q5
CLOCK
20
19
18
17
16
15
14
13
12
11
Q D
CK
R
D Q
CK
R
Q D
CK
R
D Q
CK
R
R
CK
Q D
R
CK
D Q
R
CK
Q D
R
CK
D Q
1
2
3
4
5
6
7
8
9
10
RESET
Q1
D1
D2
Q2
Q3
D3
D4
Q4
VSS

7432
(QUAD 2-INPUT OR GATE)

(TOP VIEW)

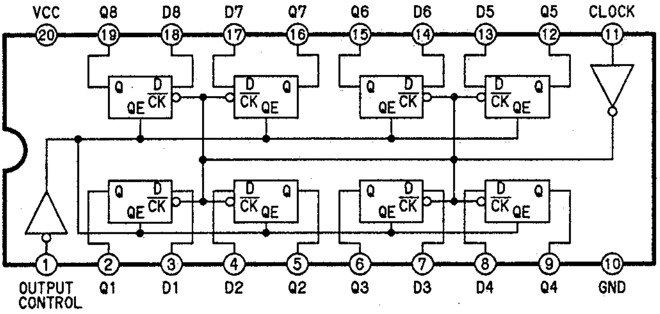

VDD
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
VSS

74367
(HEX 3-STATE BUS BUFFERS)


VCC
G2
6A
6V
5A
5V
4A
4V
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
G1
1A
1V
2A
2V
3A
3V
GND

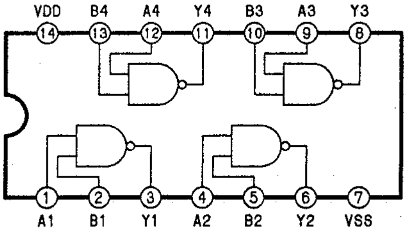
74374
(3-STATE OCTAL D-TYPE FLIP-FLOP)

(TOP VIEW)


VCC
Q8
D8
D7
Q7
Q6
D6
D5
Q5
CLOCK
20
19
18
17
16
15
14
13
12
11
Q D
QE CK
D Q
CK QE
Q D
QE CK
D Q
CK QE
Q D
QE CK
D Q
CK QE
Q D
QE CK
D Q
CK QE
1
2
3
4
5
6
7
8
9
10
OUTPUT CONTROL
Q1
D1
D2
Q2
Q3
D3
D4
Q4
GND

7438
(QUAD 2-INPUT O.C.NAND BUFFER)

(TOP VIEW)

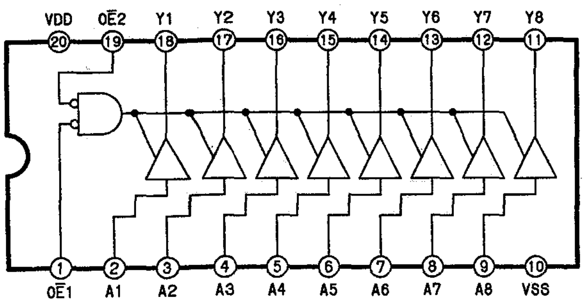

VDD
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
VSS

TRUTH TABLE (74HC273)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	×	×	L
H	↑	H	H
H	↑	L	L
H	L	×	Q0

74541
(OCTAL 3-STATE BUFFER)

(TOP VIEW)


VDD
$\overline{\text{OE}}$2
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
20
19
18
17
16
15
14
13
12
11
1
2
3
4
5
6
7
8
9
10
$\overline{\text{OE}}$1
A1
A2
A3
A4
A5
A6
A7
A8
VSS

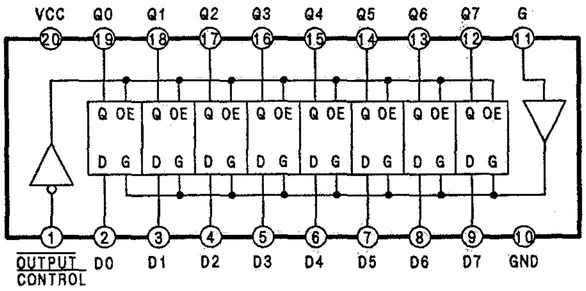
$\overline{\text{OE}}$1, $\overline{\text{OE}}$2 : $\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$

TRUTH TABLE

INPUT			OUTPUT
$\overline{\text{OE}}$1	$\overline{\text{OE}}$2	A	Y
L	L	L	L
L	L	H	H
H	×	×	Z
×	H	×	Z

X:H or L Z:HIGH IMPEDANCE

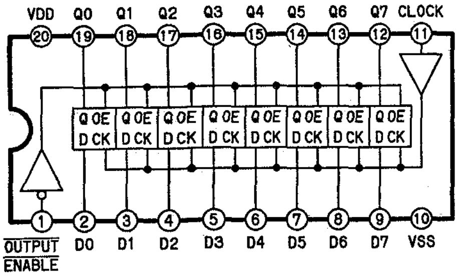
74573
(OCTAL 3 STATE D-LATCHES)


VCC
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
G
20
19
18
17
16
15
14
13
12
11
Q OE
D G
1
2
3
4
5
6
7
8
9
10
$\overline{\text{OUTPUT}}$ CONTROL
D0
D1
D2
D3
D4
D5
D6
D7
GND

INPUT		FUNCTION
OUTPUT CONTROL	LATCH ENABLE	
L	L	LATCH (HOLD)
L	H	Q=D
H	X	HIGH-Z

74574
(OCTAL D-TYPE FLIP-FLOP)

(TOP VIEW)


VDD
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CLOCK
20
19
18
17
16
15
14
13
12
11
Q OE
D CK
1
2
3
4
5
6
7
8
9
10
$\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$
D0
D1
D2
D3
D4
D5
D6
D7
VSS

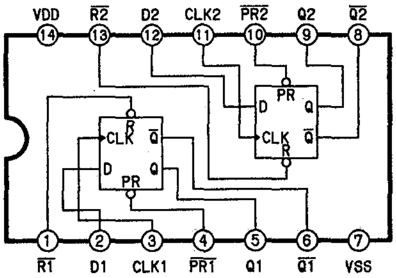
TRUTH TABLE (74HC574)

INPUT			OUTPUT
$\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$	CLOCK	DATA D	Q
L	↑	H	H
L	↑	L	L
L	↓	×	NO CHANGE
H	×	×	Z

X:H or L Z:HIGH IMPEDANCE

7474
(DUAL D-TYPE FLIP-FLOP)

(TOP VIEW)


VDD
$\overline{\text{R2}}$
D2
CLK2
$\overline{\text{PR2}}$
Q2
$\overline{\text{Q2}}$
14
13
12
11
10
9
8
D
PR
Q
CLK
R
$\overline{\text{Q}}$
1
2
3
4
5
6
7
$\overline{\text{R1}}$
D1
CLK1
$\overline{\text{PR1}}$
Q1
$\overline{\text{Q1}}$
VSS

CLK:CLOCK

$\overline{\text{PR}}$:$\overline{\text{PRESET}}$

$\overline{\text{R}}$:$\overline{\text{RESET}}$

D:DATA

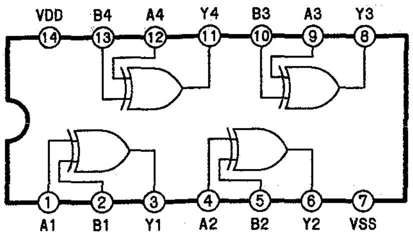
TRUTH TABLE (74HC74)

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\overline{\text{Q}}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	×	Q0	$\overline{\text{Q}}$0

*:UNSTABLE

7486
(QUAD EXCLUSIVE OR GATE)

(TOP VIEW)

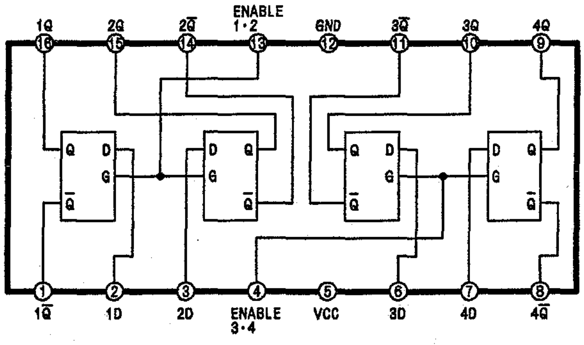

VDD
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
VSS

$Y=A\oplus B=\overline{A}B+A\overline{B}$

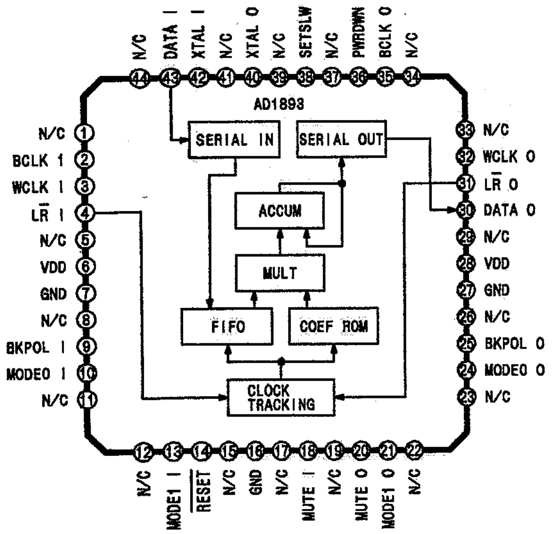
TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

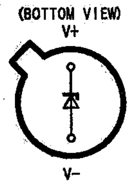
7475
(4-BIT LATCHES)


1Q
2Q
$2\overline{\text{Q}}$
ENABLE 1·2
GND
$3\overline{\text{Q}}$
3Q
4Q
16
15
14
13
12
11
10
9
Q
D
G
$\overline{\text{Q}}$
1
2
3
4
5
6
7
8
$1\overline{\text{Q}}$
1D
2D
ENABLE 3·4
VCC
3D
4D
$4\overline{\text{Q}}$

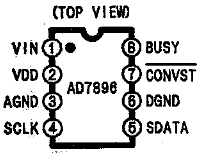
AD1893JST
(SAMPLING RATE CONVERTER)


AD1893
N/C 44
DATA I 43
XTAL I 42
N/C 41
XTAL O 40
N/C 39
SETSLW 38
N/C 37
PWRDWN 36
BCLK O 35
N/C 34
N/C 1
BCLK I 2
WCLK I 3
LR̄ I 4
N/C 5
VDD 6
GND 7
N/C 8
BKPOL I 9
MODE0 I 10
N/C 11
N/C 33
WCLK O 32
LR̄ O 31
DATA O 30
N/C 29
VDD 28
GND 27
N/C 26
BKPOL O 25
MODE0 O 24
N/C 23
N/C 12
MODE1 I 13
RESET 14
N/C 15
GND 16
N/C 17
MUTE I 18
N/C 19
MUTE O 20
MODE1 O 21
N/C 22
SERIAL IN
SERIAL OUT
ACCUM
MULT
FIFO
COEF ROM
CLOCK TRACKING

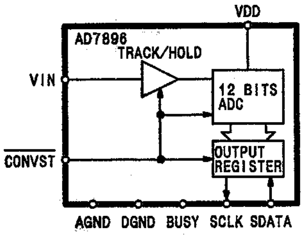
AD589
(VOLTAGE REGULATOR)


(BOTTOM VIEW)
V+
V−

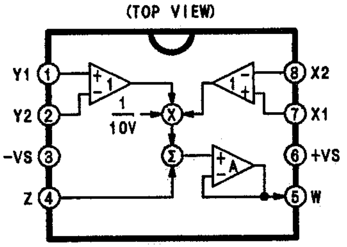
AD7896AR
(12 BITS A/D CONVERTER)


(TOP VIEW)
VIN 1
VDD 2
AGND 3
SCLK 4
8 BUSY
7 CONVST
6 DGND
5 SDATA
AD7896

BLOCK DIAGRAM

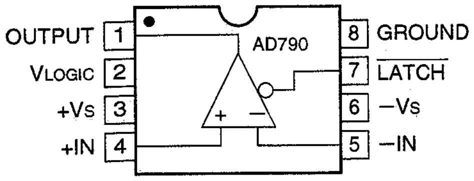

VDD
AD7896
TRACK/HOLD
VIN
12 BITS ADC
CONVST
OUTPUT REGISTER
AGND
DGND
BUSY
SCLK
SDATA

AD633JR
(ANALOG MULTIPLIER)

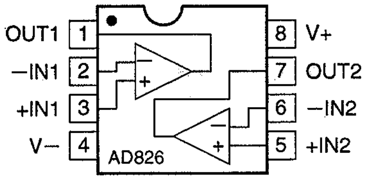

(TOP VIEW)
Y1 1
Y2 2
−VS 3
Z 4
8 X2
7 X1
6 +VS
5 W
1
1/10V
X
Σ
A
1

$$W = \frac{(X1-X2)\ (Y1-Y2)}{10V} + Z$$

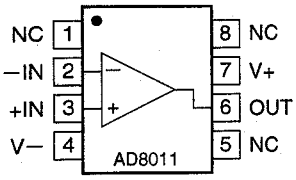
AD790 (FAST, PRECISION COMPARATOR)


OUTPUT 1
VLOGIC 2
+Vs 3
+IN 4
8 GROUND
7 LATCH
6 −Vs
5 −IN
AD790
+
−

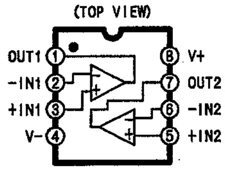
AD826AR (HIGH SPEED, LOW POWER DUAL OP AMP)


OUT1 1
−IN1 2
+IN1 3
V− 4
8 V+
7 OUT2
6 −IN2
5 +IN2
AD826

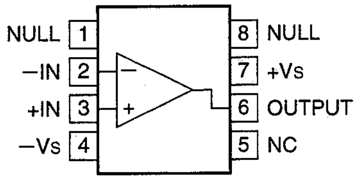
AD8011AR
(300MHz, 1mA CURRENT FEEDBACK OP AMP)


NC 1
−IN 2
+IN 3
V− 4
8 NC
7 V+
6 OUT
5 NC
AD8011

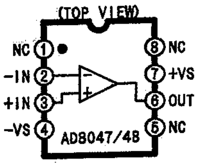
AD828AR
(VIDEO OP AMP)


(TOP VIEW)
OUT1 1
−IN1 2
+IN1 3
V− 4
8 V+
7 OUT2
6 −IN2
5 +IN2

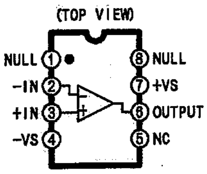
AD848JR
(TOP VIEW)


NULL 1
−IN 2
+IN 3
−Vs 4
8 NULL
7 +Vs
6 OUTPUT
5 NC

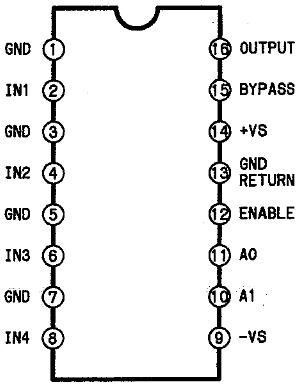
AD8047AR
(VIDEO OP AMP)


(TOP VIEW)
NC 1
−IN 2
+IN 3
−VS 4
8 NC
7 +VS
6 OUT
5 NC
AD8047/48

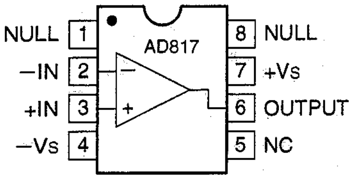
AD818AR
(VIDEO OP AMP)


(TOP VIEW)
NULL 1
−IN 2
+IN 3
−VS 4
8 NULL
7 +VS
6 OUTPUT
5 NC

AD9300 (SELECT SWITCH)
(TOP VIEW)

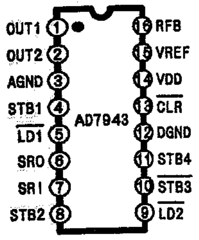

GND 1
IN1 2
GND 3
IN2 4
GND 5
IN3 6
GND 7
IN4 8
16 OUTPUT
15 BYPASS
14 +VS
13 GND RETURN
12 ENABLE
11 A0
10 A1
9 −VS

AD817AR (HIGH SPEED, LOW POWER OP AMP)

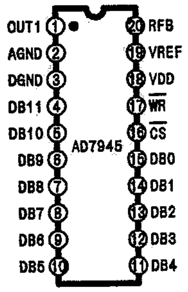

NULL 1
−IN 2
+IN 3
−Vs 4
8 NULL
7 +Vs
6 OUTPUT
5 NC
AD817

AD7943BR/AD7945BR
(12 BITS D/A CONVERTER)

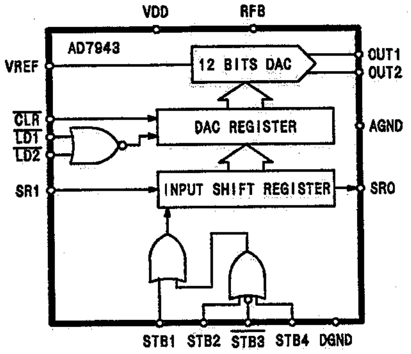
(TOP VIEW)


OUT1 1
OUT2 2
AGND 3
STB1 4
LD1 5
SRO 6
SR1 7
STB2 8
AD7943
16 RFB
15 VREF
14 VDD
13 CLR
12 DGND
11 STB4
10 STB3
9 LD2

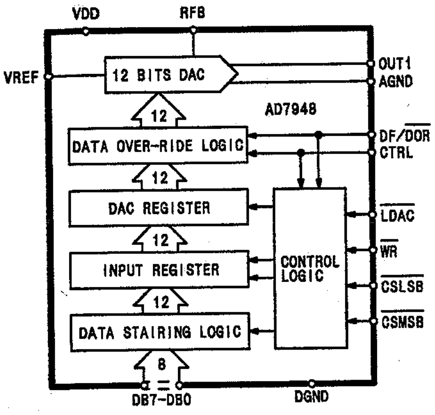
(TOP VIEW)


OUT1 1
AGND 2
DGND 3
DB11 4
DB10 5
DB9 6
DB8 7
DB7 8
DB6 9
DB5 10
AD7945
20 RFB
19 VREF
18 VDD
17 WR
16 CS
15 DB0
14 DB1
13 DB2
12 DB3
11 DB4

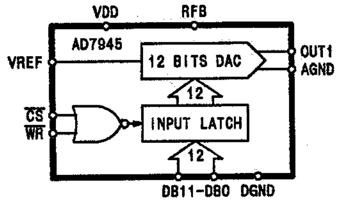
BLOCK DIAGRAM


VDD
RFB
AD7943
VREF
12 BITS DAC
OUT1
OUT2
CLR
LD1
LD2
DAC REGISTER
AGND
SR1
INPUT SHIFT REGISTER
SRO
STB1
STB2
STB3
STB4
DGND

BLOCK DIAGRAM

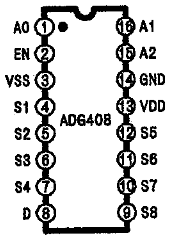

VDD
RFB
VREF
12 BITS DAC
OUT1
AGND
12
AD7948
DATA OVER-RIDE LOGIC
DF/DOR
CTRL
12
DAC REGISTER
LDAC
12
WR
INPUT REGISTER
CONTROL LOGIC
CSLSB
12
CSMSB
DATA STAIRING LOGIC
8
DB7-DB0
DGND

BLOCK DIAGRAM

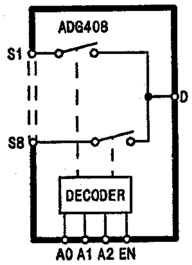

VDD
RFB
AD7945
VREF
12 BITS DAC
OUT1
AGND
12
CS
WR
INPUT LATCH
12
DB11-DB0
DGND

ADG408BR
(CMOS SWITCH)

(TOP VIEW)

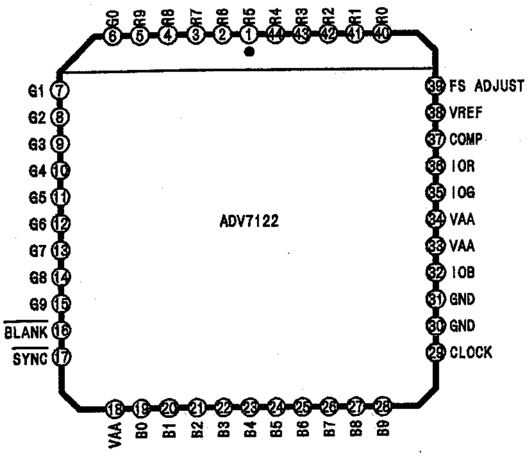

A0 1
EN 2
VSS 3
S1 4
S2 5
S3 6
S4 7
D 8
ADG408
16 A1
15 A2
14 GND
13 VDD
12 S5
11 S6
10 S7
9 S8

BLOCK DIAGRAM

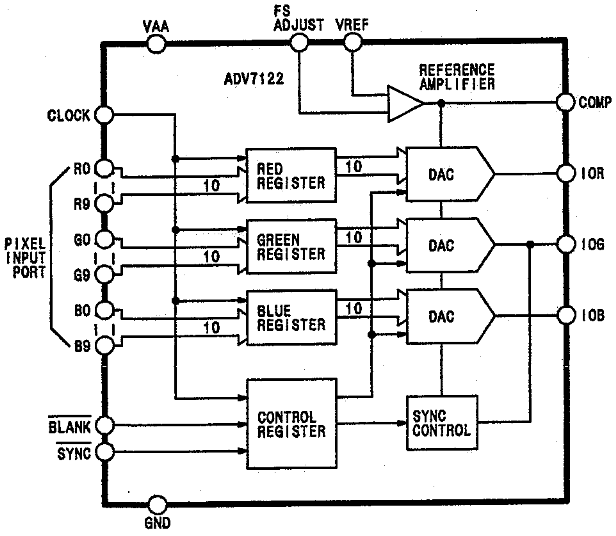

ADG408
S1
S8
D
DECODER
A0
A1
A2
EN

ADV7122
(VIDEO 10 BIT DA CONVERTER)

(TOP VIEW)

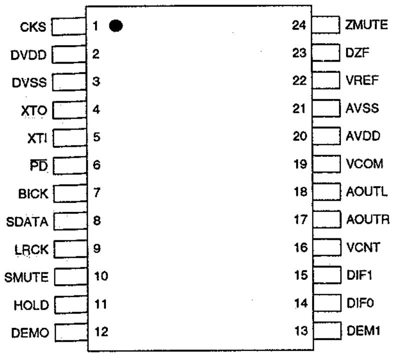

G0 6
R9 5
R8 4
R7 3
R6 2
R5 1
R4 44
R3 43
R2 42
R1 41
R0 40
G1 7
G2 8
G3 9
G4 10
G5 11
G6 12
G7 13
G8 14
G9 15
BLANK 16
SYNC 17
39 FS ADJUST
38 VREF
37 COMP
36 IOR
35 IOG
34 VAA
33 VAA
32 IOB
31 GND
30 GND
29 CLOCK
ADV7122
18 VAA
19 B0
20 B1
21 B2
22 B3
23 B4
24 B5
25 B6
26 B7
27 B8
28 B9

BLOCK DIAGRAM

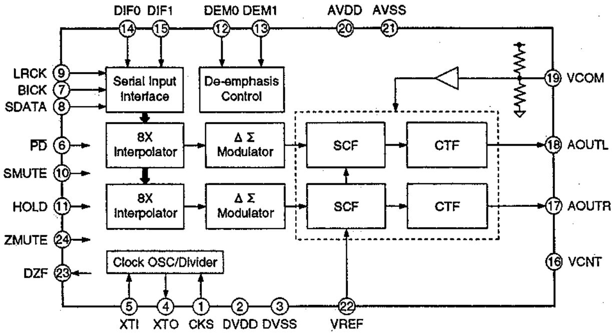

VAA
FS ADJUST
VREF
ADV7122
REFERENCE AMPLIFIER
COMP
CLOCK
R0
R9
RED REGISTER
10
10
DAC
IOR
PIXEL INPUT PORT
G0
G9
GREEN REGISTER
10
10
DAC
IOG
B0
B9
BLUE REGISTER
10
10
DAC
IOB
BLANK
SYNC
CONTROL REGISTER
SYNC CONTROL
GND

AK4320VM(1 BIT DAC)

(TOP VIEW)

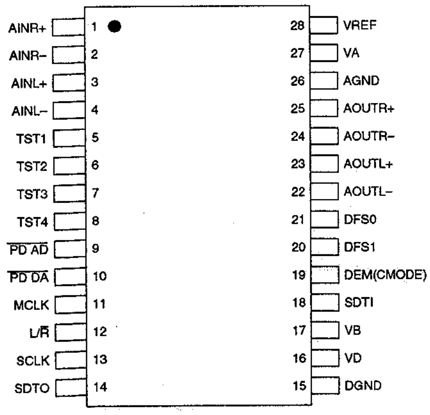

CKS 1
DVDD 2
DVSS 3
XTO 4
XTI 5
PD 6
BICK 7
SDATA 8
LRCK 9
SMUTE 10
HOLD 11
DEMO 12
24 ZMUTE
23 DZF
22 VREF
21 AVSS
20 AVDD
19 VCOM
18 AOUTL
17 AOUTR
16 VCNT
15 DIF1
14 DIF0
13 DEM1

BLOCK DIAGRAM

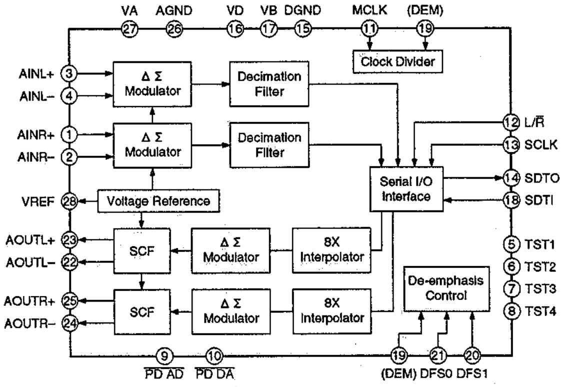

DIF0 DIF1
DEM0 DEM1
AVDD AVSS
LRCK 9
BICK 7
SDATA 8
Serial Input Interface
De-emphasis Control
PD 6
SMUTE 10
HOLD 11
ZMUTE 24
DZF 23
8X Interpolator
Δ Σ Modulator
SCF
CTF
Clock OSC/Divider
19 VCOM
18 AOUTL
17 AOUTR
16 VCNT
XTI XTO CKS DVDD DVSS
VREF

AK4503VF (AD,DA CONVERTER)

(TOP VIEW)


AINR+ 1
AINR– 2
AINL+ 3
AINL– 4
TST1 5
TST2 6
TST3 7
TST4 8
PD AD 9
PD DA 10
MCLK 11
L/R 12
SCLK 13
SDTO 14
28 VREF
27 VA
26 AGND
25 AOUTR+
24 AOUTR–
23 AOUTL+
22 AOUTL–
21 DFS0
20 DFS1
19 DEM(CMODE)
18 SDTI
17 VB
16 VD
15 DGND

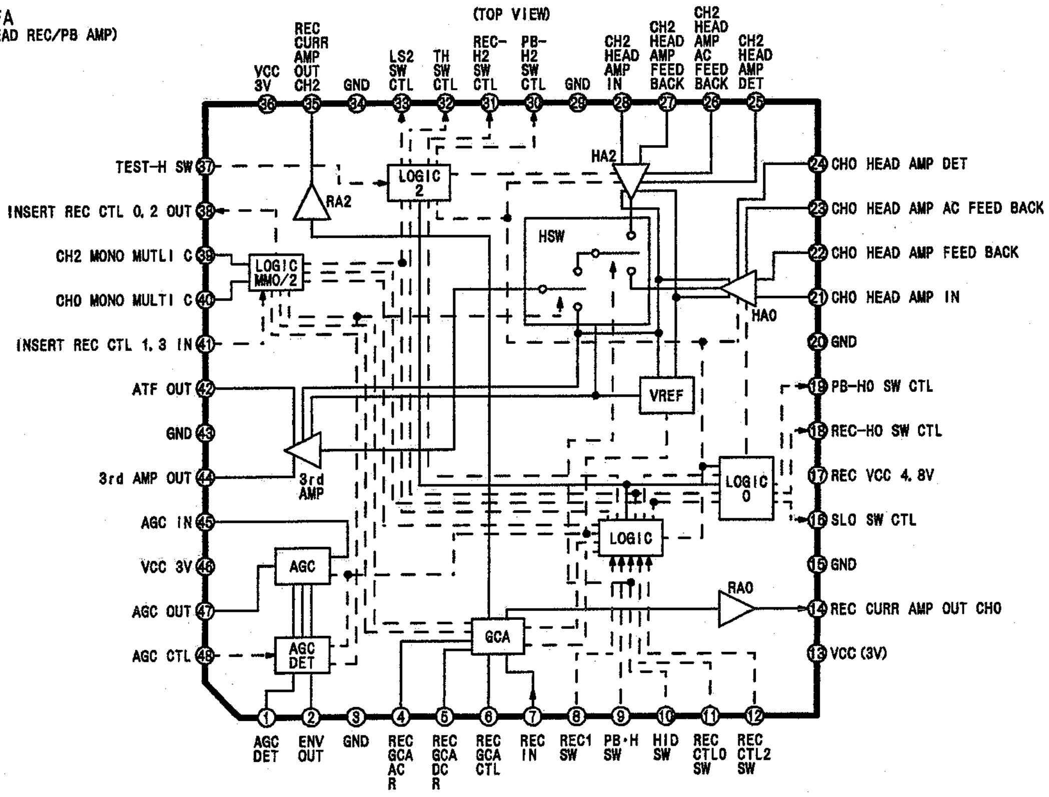
BLOCK DIAGRAM


VA AGND
VD VB DGND
MCLK (DEM)
Clock Divider
AINL+ 3
AINL– 4
AINR+ 1
AINR– 2
Δ Σ Modulator
Decimation Filter
VREF 28
Voltage Reference
Serial I/O Interface
12 L/R
13 SCLK
14 SDTO
18 SDTI
AOUTL+ 23
AOUTL– 22
AOUTR+ 25
AOUTR– 24
SCF
8X Interpolator
De-emphasis Control
5 TST1
6 TST2
7 TST3
8 TST4
PD AD PD DA
(DEM) DFS0 DFS1

AN3730FA

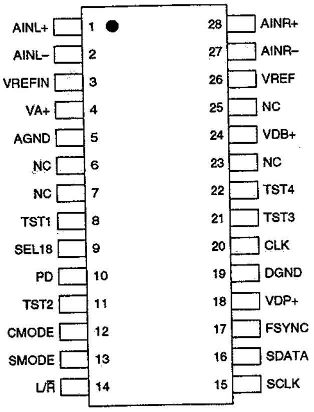
(DVC 2 HEAD REC/PB AMP)

(TOP VIEW)


VCC 3V
REC CURR AMP OUT CH2
GND
LS2 SW CTL
TH SW CTL
REC-H2 SW CTL
PB-H2 SW CTL
GND
CH2 HEAD AMP IN
CH2 HEAD AMP FEED BACK
CH2 HEAD AMP AC FEED BACK
CH2 HEAD AMP DET
TEST-H SW 37
INSERT REC CTL 0, 2 OUT 38
CH2 MONO MUTLI C 39
CH0 MONO MULTI C 40
INSERT REC CTL 1, 3 IN 41
ATF OUT 42
GND 43
3rd AMP OUT 44
AGC IN 45
VCC 3V 46
AGC OUT 47
AGC CTL 48
24 CH0 HEAD AMP DET
23 CH0 HEAD AMP AC FEED BACK
22 CH0 HEAD AMP FEED BACK
21 CH0 HEAD AMP IN
20 GND
19 PB-H0 SW CTL
18 REC-H0 SW CTL
17 REC VCC 4.8V
16 SL0 SW CTL
15 GND
14 REC CURR AMP OUT CH0
13 VCC (3V)
AGC DET
ENV OUT
GND
REC GCA AC R
REC GCA DC R
REC GCA CTL
REC IN
REC1 SW
PB·H SW
HID SW
REC CTL0 SW
REC CTL2 SW
LOGIC 2
RA2
HA2
HSW
LOGIC MMO/2
HA0
VREF
3rd AMP
LOGIC 0
LOGIC
AGC
AGC DET
RA0
GCA

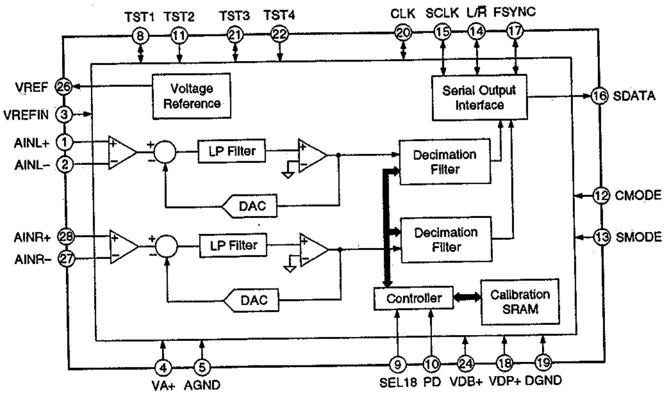
AK5340 (DA CONVERTER)

(TOP VIEW)



AINL+ 1
AINL– 2
VREFIN 3
VA+ 4
AGND 5
NC 6
NC 7
TST1 8
SEL18 9
PD 10
TST2 11
CMODE 12
SMODE 13
L/R̄ 14
28 AINR+
27 AINR–
26 VREF
25 NC
24 VDB+
23 NC
22 TST4
21 TST3
20 CLK
19 DGND
18 VDP+
17 FSYNC
16 SDATA
15 SCLK

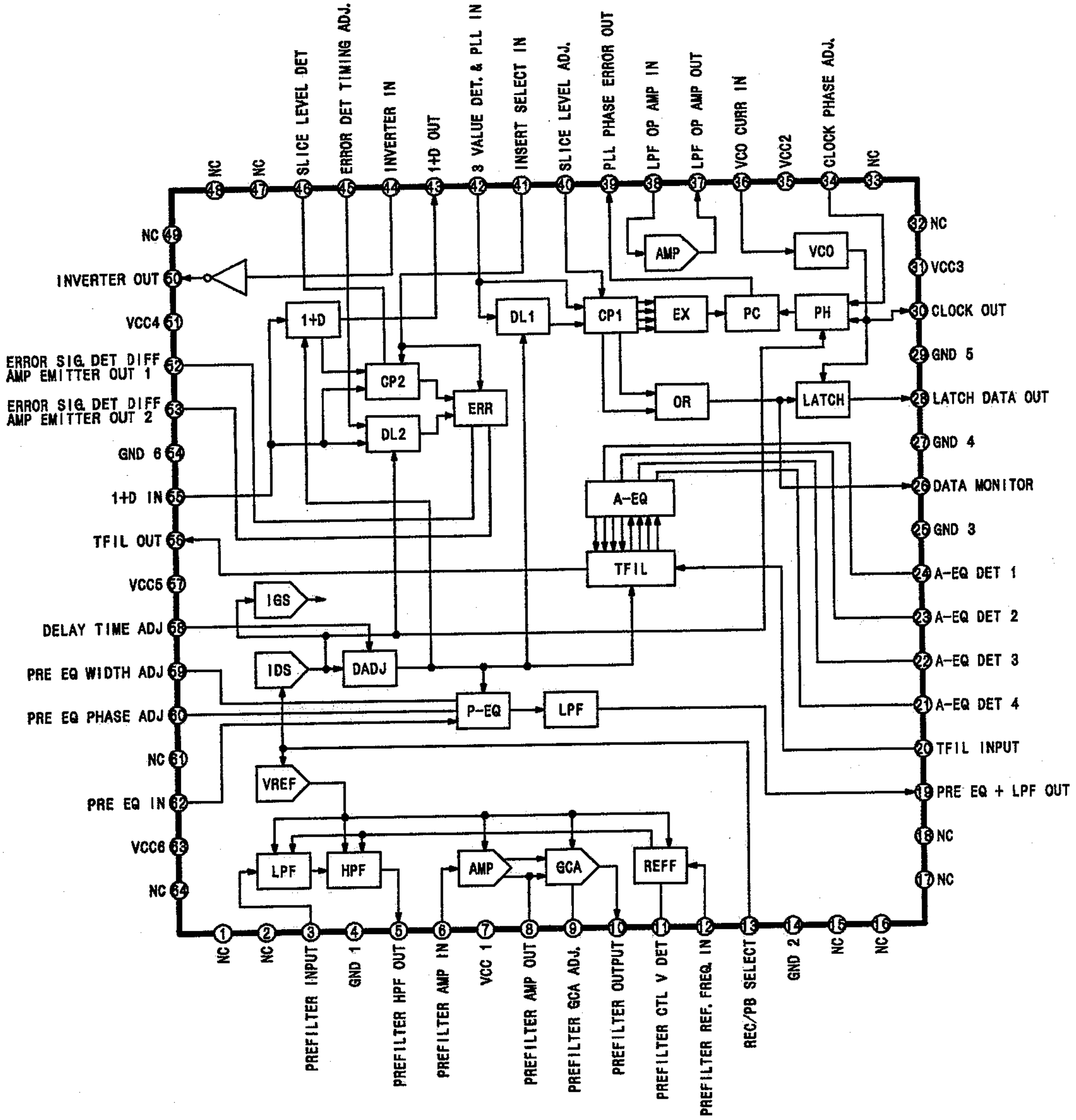
BLOCK DIAGRAM



TST1 TST2 TST3 TST4
8 11 21 22
CLK SCLK L/R̄ FSYNC
20 15 14 17
VREF 26
VREFIN 3
AINL+ 1
AINL– 2
AINR+ 28
AINR– 27
Voltage Reference
Serial Output Interface
16 SDATA
LP Filter
DAC
LP Filter
DAC
Decimation Filter
Decimation Filter
12 CMODE
13 SMODE
Controller
Calibration SRAM
4 5
VA+ AGND
9 10 24 18 19
SEL18 PD VDB+ VDP+ DGND

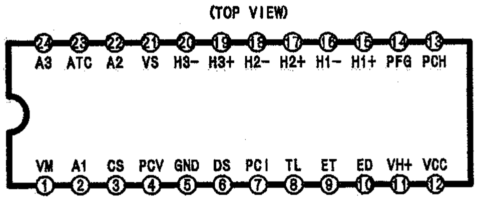
AN3740FAP
(PLAYBACK EQULIZER)

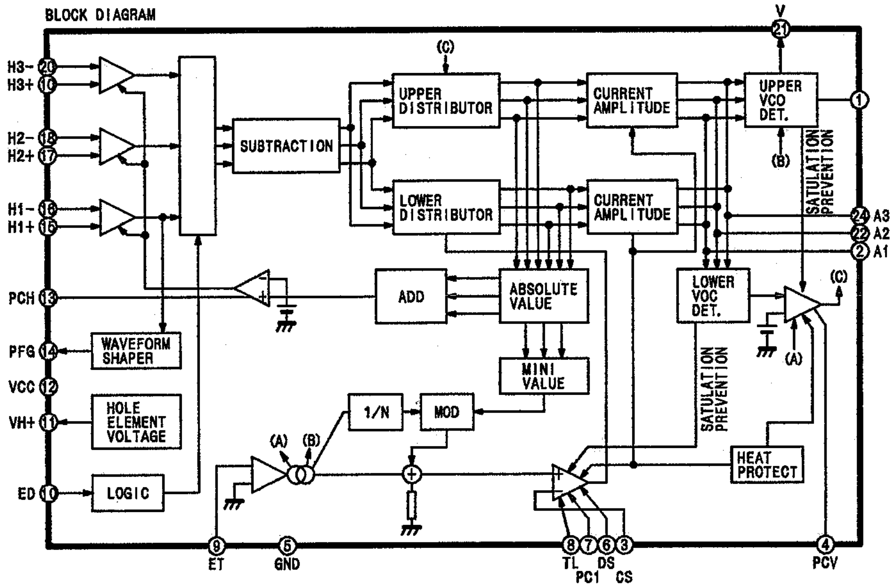
(TOP VIEW)



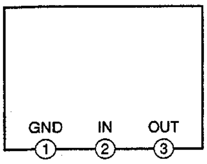
48 NC
47 NC
46 SLICE LEVEL DET
45 ERROR DET TIMING ADJ.
44 INVERTER IN
43 1+D OUT
42 3 VALUE DET. & PLL IN
41 INSERT SELECT IN
40 SLICE LEVEL ADJ.
39 PLL PHASE ERROR OUT
38 LPF OP AMP IN
37 LPF OP AMP OUT
36 VCO CURR IN
35 VCC2
34 CLOCK PHASE ADJ.
33 NC
32 NC
31 VCC3
30 CLOCK OUT
29 GND 5
28 LATCH DATA OUT
27 GND 4
26 DATA MONITOR
25 GND 3
24 A-EQ DET 1
23 A-EQ DET 2
22 A-EQ DET 3
21 A-EQ DET 4
20 TFIL INPUT
19 PRE EQ + LPF OUT
18 NC
17 NC
NC 49
INVERTER OUT 50
VCC4 51
ERROR SIG. DET DIFF AMP EMITTER OUT 1 52
ERROR SIG. DET DIFF AMP EMITTER OUT 2 53
GND 6 54
1+D IN 55
TFIL OUT 56
VCC5 57
DELAY TIME ADJ 58
PRE EQ WIDTH ADJ 59
PRE EQ PHASE ADJ 60
NC 61
PRE EQ IN 62
VCC6 63
NC 64
1 NC
2 NC
3 PREFILTER INPUT
4 GND 1
5 PREFILTER HPF OUT
6 PREFILTER AMP IN
7 VCC 1
8 PREFILTER AMP OUT
9 PREFILTER GCA ADJ.
10 PREFILTER OUTPUT
11 PREFILTER CTL V DET
12 PREFILTER REF. FREQ. IN
13 REC/PB SELECT
14 GND 2
15 NC
16 NC
AMP
VCO
1+D
DL1
CP1
EX
PC
PH
CP2
ERR
DL2
OR
LATCH
A-EQ
TFIL
IGS
IDS
DADJ
P-EQ
LPF
VREF
LPF
HPF
AMP
GCA
REFF

AN3834S

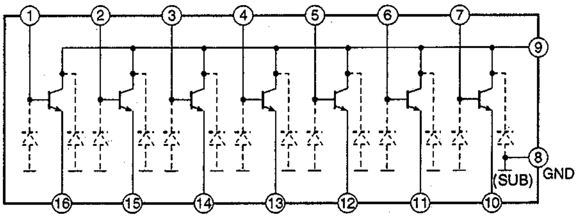

(TOP VIEW)
A3 ATC A2 VS H3- H3+ H2- H2+ H1- H1+ PFG PCH
24 23 22 21 20 19 18 17 16 15 14 13
VM A1 CS PCV GND DS PC1 TL ET ED VH+ VCC
1 2 3 4 5 6 7 8 9 10 11 12


BLOCK DIAGRAM
V
21
H3- 20
H3+ 19
H2- 18
H2+ 17
H1- 16
H1+ 15
PCH 13
PFG 14
VCC 12
VH+ 11
ED 10
SUBTRACTION
(C)
UPPER DISTRIBUTOR
LOWER DISTRIBUTOR
CURRENT AMPLITUDE
CURRENT AMPLITUDE
UPPER VCO DET.
(B)
SATULATION PREVENTION
LOWER VOC DET.
SATULATION PREVENTION
(C)
(A)
HEAT PROTECT
ADD
ABSOLUTE VALUE
MINI VALUE
WAVEFORM SHAPER
HOLE ELEMENT VOLTAGE
LOGIC
1/N
MOD
(A) (B)
1
24 A3
22 A2
2 A1
9 ET
5 GND
8 TL
7 PC1
6 DS
3 CS
4 PCV

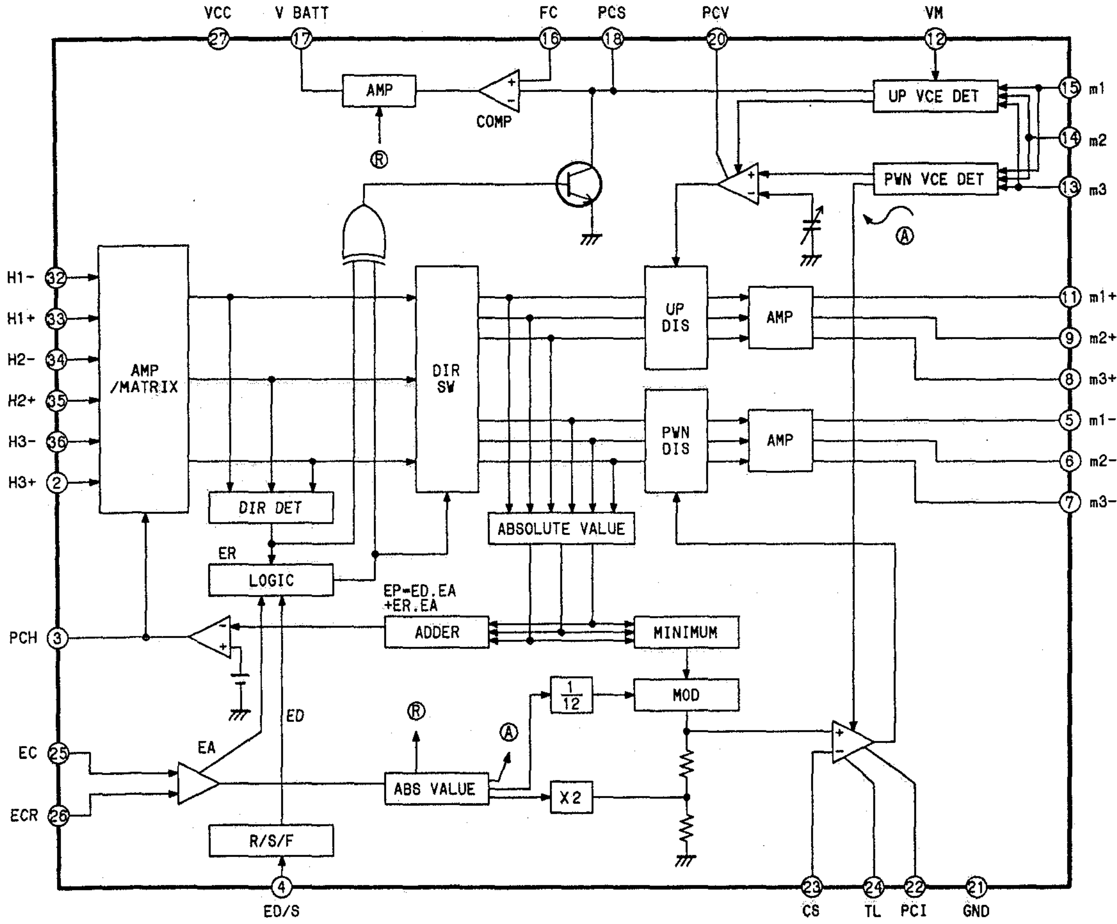
AN7905F


GND IN OUT
1 2 3

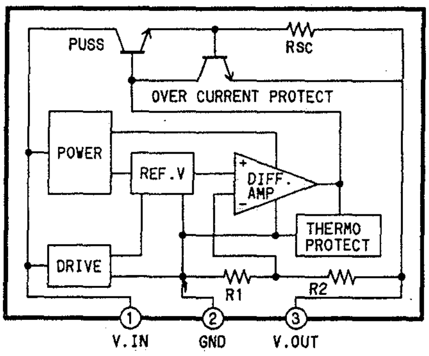
AN90B60S
(EQUIVALENT CIRCUIT)


1 2 3 4 5 6 7
9
8
(SUB)
GND
16 15 14 13 12 11 10

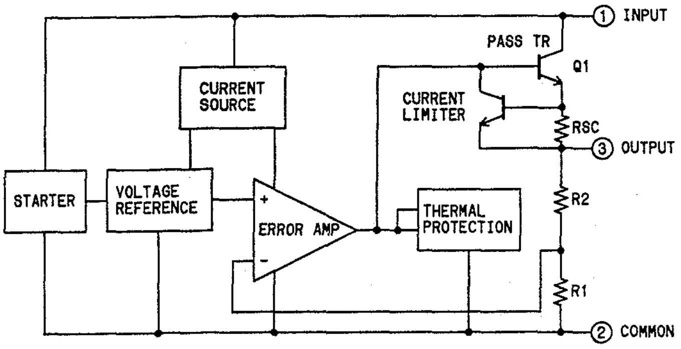
AN3890FBS

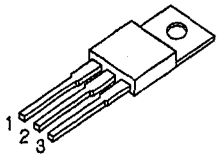

VCC 27
V BATT 17
FC 16
PCS 18
PCV 20
VM 12
AMP
COMP
R
UP VCE DET
PWN VCE DET
m1 15
m2 14
m3 13
A
H1- 32
H1+ 33
H2- 34
H2+ 35
H3- 36
H3+ 2
AMP /MATRIX
DIR SW
UP DIS
PWN DIS
AMP
AMP
m1+ 11
m2+ 9
m3+ 8
m1- 5
m2- 6
m3- 7
DIR DET
ABSOLUTE VALUE
ER
LOGIC
EP=ED.EA +ER.EA
ADDER
MINIMUM
PCH 3
1/12
MOD
ED
R
A
EC 25
EA
ECR 26
ABS VALUE
X2
R/S/F
4 ED/S
23 CS
24 TL
22 PCI
21 GND

AN7805


PUSS
RSC
OVER CURRENT PROTECT
POWER
REF.V
DIFF. AMP
THERMO PROTECT
DRIVE
R1
R2
1 V.IN
2 GND
3 V.OUT

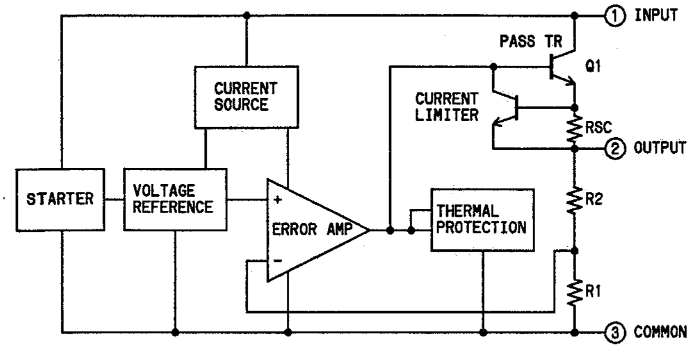
AN78M00
(3-TERMINAL POSITIVE OUTPUT VOLTAGE REGULATOR)


1 INPUT
PASS TR
Q1
CURRENT SOURCE
CURRENT LIMITER
RSC
3 OUTPUT
STARTER
VOLTAGE REFERENCE
ERROR AMP
THERMAL PROTECTION
R2
R1
2 COMMON

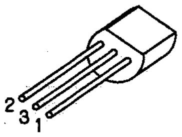


AN78L00

(3-TERMINAL POSITIVE OUTPUT VOLTAGE REGULATOR)

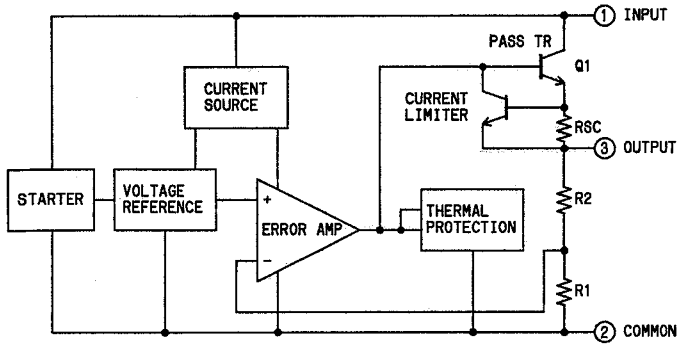


① INPUT
PASS TR
Q1
CURRENT SOURCE
CURRENT LIMITER
RSC
② OUTPUT
STARTER
VOLTAGE REFERENCE
+
ERROR AMP
-
THERMAL PROTECTION
R2
R1
③ COMMON

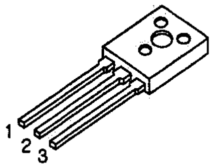


AN78N00

(3-TERMINAL POSITIVE OUTPUT VOLTAGE REGULATOR)

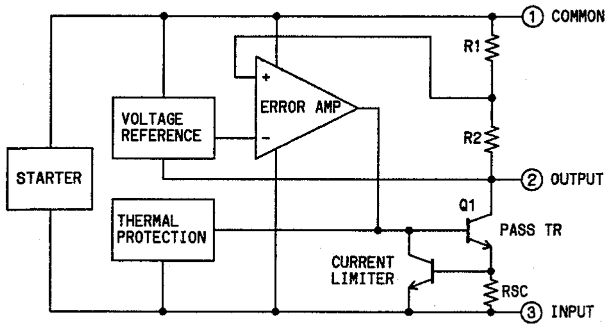


① INPUT
PASS TR
Q1
CURRENT SOURCE
CURRENT LIMITER
RSC
③ OUTPUT
STARTER
VOLTAGE REFERENCE
+
ERROR AMP
-
THERMAL PROTECTION
R2
R1
② COMMON

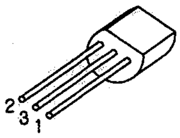


AN79L00

(3-TERMINAL NEGATIVE OUTPUT VOLTAGE REGULATOR)

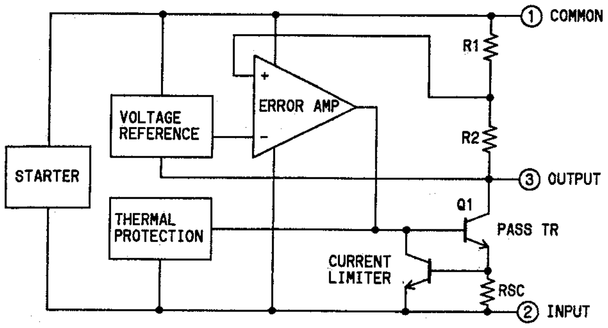


① COMMON
R1
+
ERROR AMP
-
VOLTAGE REFERENCE
R2
STARTER
② OUTPUT
Q1
THERMAL PROTECTION
PASS TR
CURRENT LIMITER
RSC
③ INPUT

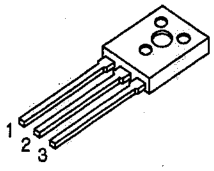


AN79N00

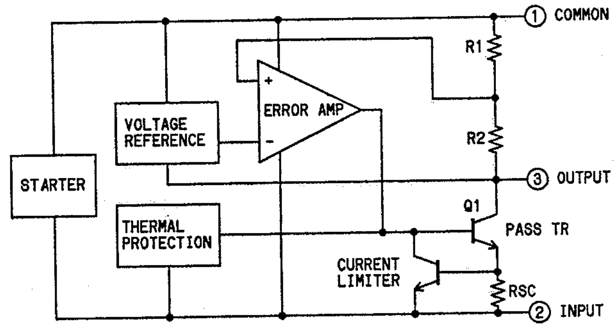
(3-TERMINAL NEGATIVE OUTPUT VOLTAGE REGULATOR)

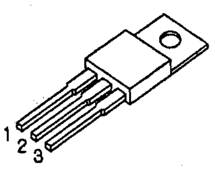


① COMMON
R1
+
ERROR AMP
-
VOLTAGE REFERENCE
R2
STARTER
③ OUTPUT
Q1
THERMAL PROTECTION
PASS TR
CURRENT LIMITER
RSC
② INPUT

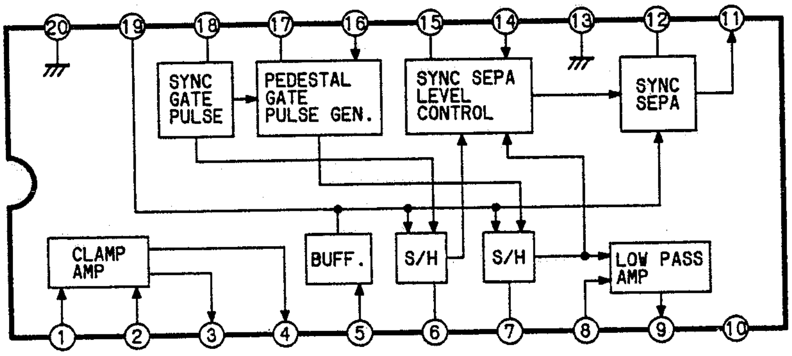


AN79M00
(3-TERMINAL NEGATIVE OUTPUT VOLTAGE REGULATOR)


① COMMON
R1
ERROR AMP
+
-
VOLTAGE REFERENCE
R2
STARTER
③ OUTPUT
Q1
THERMAL PROTECTION
PASS TR
CURRENT LIMITER
RSC
② INPUT

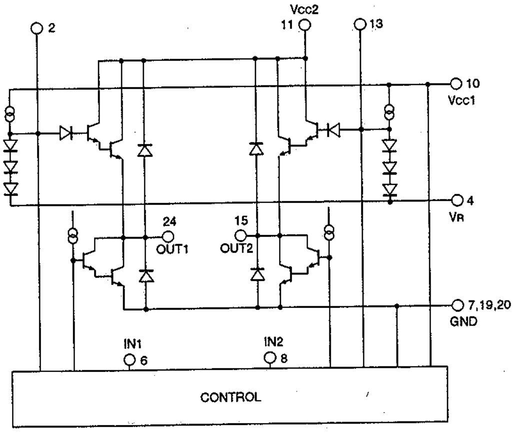


AN91A12S
(SYNC SEPARATOR)

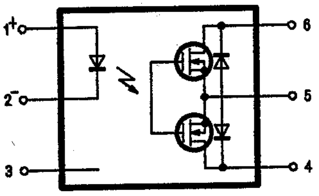

20
19
18
17
16
15
14
13
12
11
SYNC GATE PULSE
PEDESTAL GATE PULSE GEN.
SYNC SEPA LEVEL CONTROL
SYNC SEPA
CLAMP AMP
BUFF.
S/H
S/H
LOW PASS AMP
1
2
3
4
5
6
7
8
9
10

BA6219BFPY

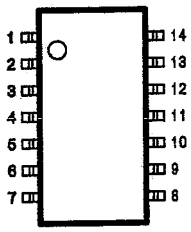
BLOCK DIAGRAM


2
Vcc2
11
13
10
Vcc1
4
VR
24
OUT1
15
OUT2
7,19,20
GND
IN1
6
IN2
8
CONTROL

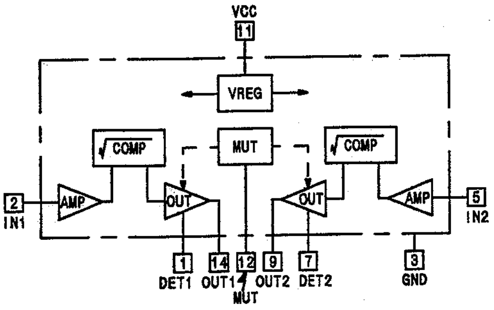
AQV212SX
(PHOTO MOS RELAY)



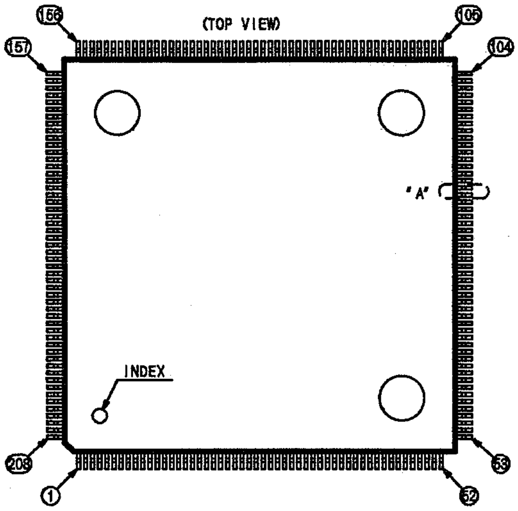
BA6138F
(1/2 MULTIPLE COMPRESSION AMP)


(TOP VIEW)
1
2
3
4
5
6
7
14
13
12
11
10
9
8

BLOCK DIAGRAM


VCC
11
VREG
√COMP
MUT
√COMP
2
IN1
AMP
OUT
OUT
AMP
5
IN2
1
DET1
14
OUT1
12
MUT
9
OUT2
7
DET2
3
GND

CG31793-2153
(GATE ARRAY)

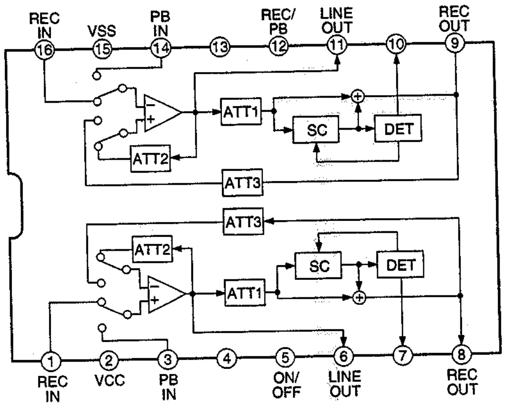


PIN ALIGNMENT

PIN NO.	I/O	PIN NAME	PIN NO.	I/O	PIN NAME	PIN NO.	I/O	PIN NAME	PIN NO.	I/O	PIN NAME
1	I/O	ADR1	53	I/O	BM OUT13	105	I	D IN7	157	I	SYSAD0
2	I/O	ADR2	54	I/O	BM OUT14	106	I	D IN8	158	I	SYSAD1
3	-	VSS	55	I/O	BM OUT15	107	-	VSS	159	I	SYSAD2
4	I/O	ADR3	56	I	JOGMWE	108	I	D IN9	160	I	SYSAD3
5	I/O	ADR4	57	I	VR IN2	109	I	D IN10	161	I	SYSAD4
6	I/O	ADR5	58	I/O	VR OUT2	110	I	D IN11	162	I	SYSAD5
7	I/O	ADR6	59	I	EEXP CLK	111	I	D IN12	163	I	BCK
8	I/O	ADR7	60	-	VSS	112	I	D IN13	164	-	VSS
9	I/O	ADR8	61	-	VDD	113	I	D IN14	165	-	VDD
10	-	VDD	62	I	EEXP REF	114	-	VDD	166	I	TEST5
11	I/O	ADR9	63	I	PRTY1	115	I	D IN15	167	I	TEST6
12	I/O	ADR10	64	I	PRTY2	116	I	IA DATA	168	I/O	BLKSYNC
13	I/O	ADR11	65	I	LRCK2	117	I	ID DATA	169	I	TEST RST
14	I/O	ADR12	66	-	N. C.	118	I	SG DATA	170	I	HIZ
15	-	VSS	67	I/O	ARECFRP	119	-	VSS	171	O	TDO
16	I/O	ADR13	68	I/O	RFRP ERR	120	I/O	REC DATA	172	I	TDI
17	I/O	ADR14	69	I/O	REC LEAP	121	I/O	CUE MIXD	173	I	TMS
18	I/O	DATA0	70	I/O	RFR GATE	122	I	PBDATA	174	I	TRS
19	I/O	DATA1	71	I	PB LEAP2	123	I	CUEMDATA	175	I	TCK
20	I/O	DATA2	72	-	VSS	124	I/O	MONIDATA	176	-	VSS
21	I/O	DATA3	73	I	MCK	125	-	N. C.	177	I	FS256
22	I/O	DATA4	74	I	TEST4	126	I	RXLRCK1	178	I	CLK REF2
23	I/O	DATA5	75	I	REC FRP	127	I	RXBCK1	179	I	CLK REF1
24	I/O	DATA6	76	I/O	T OUT1	128	I	RXLRCK2	180	I/O	FS64
25	I/O	DATA7	77	I/O	T OUT2	129	I	RXBCK2	181	I/O	FS
26	-	VSS	78	I/O	T OUT3	130	-	VSS	182	I/O	FS128
27	-	VDD	79	-	VDD	131	-	VDD	183	-	VDD
28	I/O	WE	80	I/O	T OUT4	132	I/O	RRST	184	-	N. C.
29	I/O	WRITE H	81	I	PBFRP	133	I/O	WRST1	185	I	CUEPP
30	I/O	M FAST	82	I	FEND	134	I/O	WRST2	186	I	SSD
31	I/O	M SLOW	83	I	APF18	135	I/O	WRST3	187	I	TTD
32	I/O	BUFERROR	84	I	CLK18	136	I/O	FIF GATE	188	I	VCO24M
33	I/O	JOGMCK	85	-	VSS	137	I	VR IN	189	-	VSS
34	I/O	FIELD	86	I	PB LEAP1	138	I/O	VR OUT	190	I	VCO9M
35	I/O	VALID	87	I	TEST3	139	I	PONRST	191	I	HALF L
36	I/O	LEAP	88	I	FR	140	I	PALH	192	I/O	COMPFH
37	I/O	BM OUT0	89	I/O	NOM OUT	141	I	LRCK	193	I/O	REF12K
38	-	VSS	90	I	NOM IN	142	-	VSS	194	I/O	COMP12K
39	I/O	BM OUT1	91	I	LR2	143	I	PB LRCK	195	-	N. C.
40	I/O	BMOUT2	92	I/O	DOUT	144	I	SYSCS	196	-	N. C.
41	I/O	BM OUT3	93	I	MUT	145	I	SYSRD	197	I	TEST1
42	I/O	BM OUT4	94	I	NDOWR	146	I	SYSWE	198	I	TEST2
43	-	VDD	95	I	PB LRCK2	147	-	VDD	199	I	PB BCK
44	I/O	BM OUT5	96	-	VSS	148	I/O	SYSDA0	200	-	VSS
45	I/O	BM OUT6	97	-	VDD	149	I/O	SYSDA1	201	-	VDD
46	I/O	BM OUT7	98	I	D IN0	150	I/O	SYSDA2	202	I	DIR
47	I/O	BM OUT8	99	I	D IN1	151	I/O	SYSDA3	203	I	TP0
48	I/O	BM OUT9	100	I	D IN2	152	I/O	SYSDA4	204	I	TP1
49	I/O	BM OUT10	101	I	D IN3	153	I/O	SYSDA5	205	I	TP2
50	-	VSS	102	I	D IN4	154	-	VSS	206	I	BM IN
51	I/O	BM OUT11	103	I	D IN5	155	I/O	SYSDA6	207	I/O	INIT
52	I/O	BM OUT12	104	I	D IN6	156	I/O	SYSDA7	208	I/O	ADR0

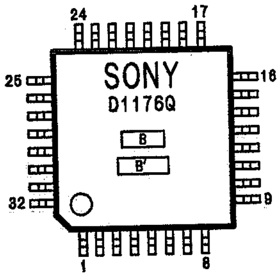
CXA1102M

BLOCK DIAGRAM

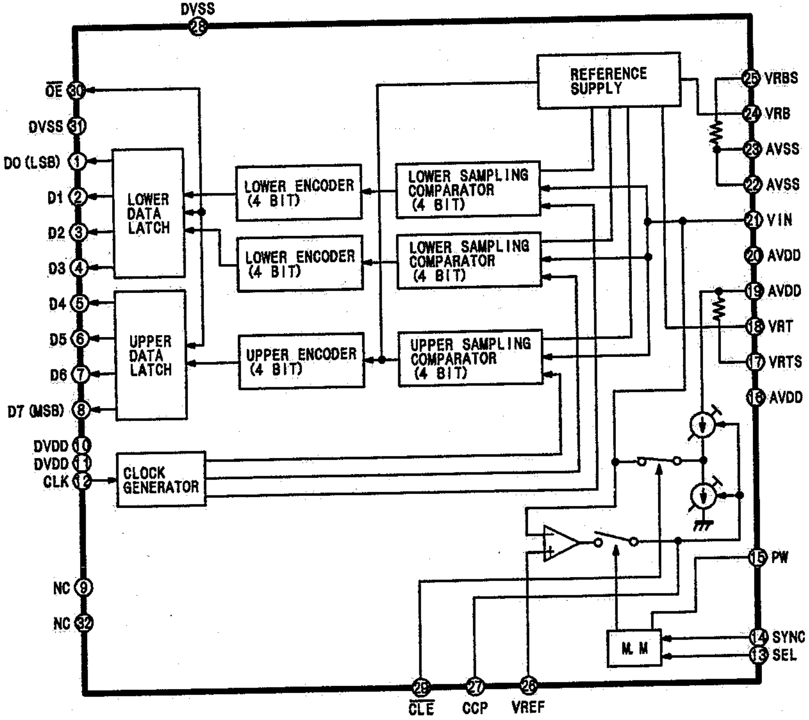

REC IN
VSS
PB IN
REC/PB
LINE OUT
REC OUT
16
15
14
13
12
11
10
9
ATT1
ATT2
ATT3
SC
DET
1
2
3
4
5
6
7
8
REC IN
VCC
PB IN
ON/OFF
LINE OUT
REC OUT

CXD1176Q

(8 BITS 20 MSPS VIDEO A/D CONVERTER WITH CLAMP FUNCTION)

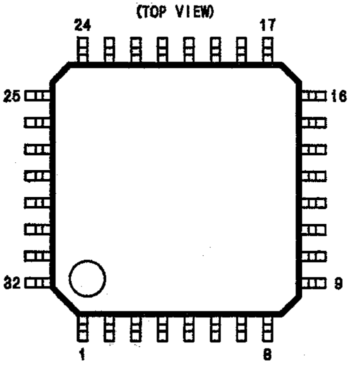

24
17
25
16
SONY
D1176Q
B
B'
32
9
1
8

BLOCK DIAGRAM

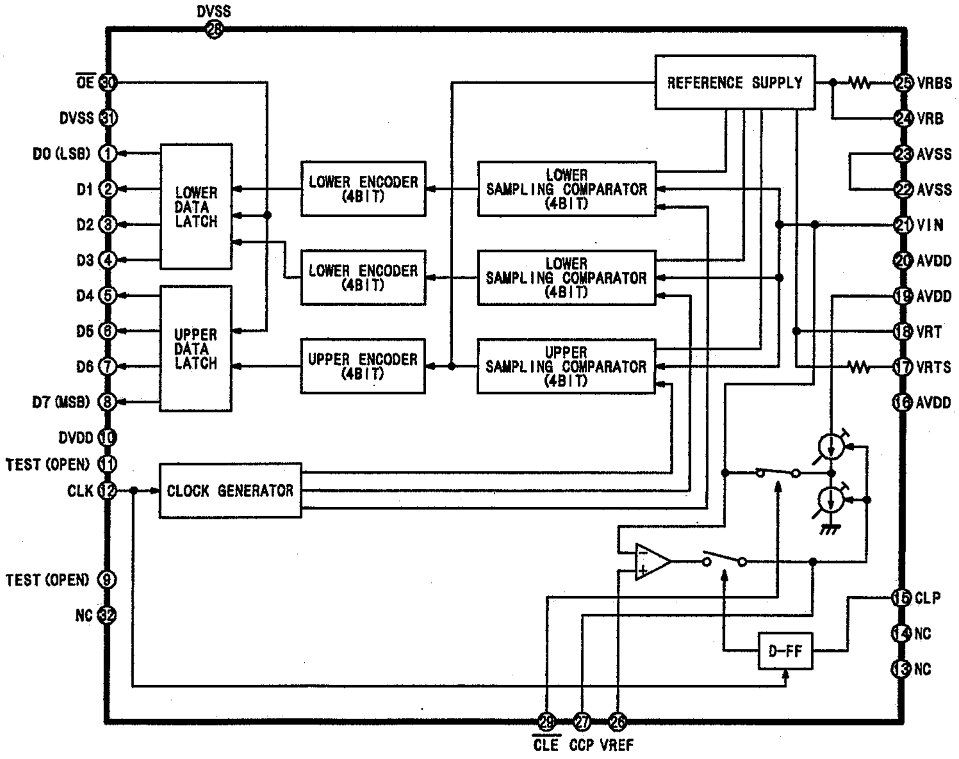

DVSS 28
OE 30
DVSS 31
D0 (LSB) 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
D7 (MSB) 8
DVDD 10
DVDD 11
CLK 12
NC 9
NC 32
LOWER DATA LATCH
UPPER DATA LATCH
LOWER ENCODER (4 BIT)
LOWER ENCODER (4 BIT)
UPPER ENCODER (4 BIT)
LOWER SAMPLING COMPARATOR (4 BIT)
LOWER SAMPLING COMPARATOR (4 BIT)
UPPER SAMPLING COMPARATOR (4 BIT)
REFERENCE SUPPLY
CLOCK GENERATOR
M. M
25 VRBS
24 VRB
23 AVSS
22 AVSS
21 VIN
20 AVDD
19 AVDD
18 VRT
17 VRTS
16 AVDD
15 PW
14 SYNC
13 SEL
29 CLE
27 CCP
26 VREF

CXD2302Q

(8 BITS 50MSPS VIDEO A/D CONVERTER WITH CLAMP OPERATION)

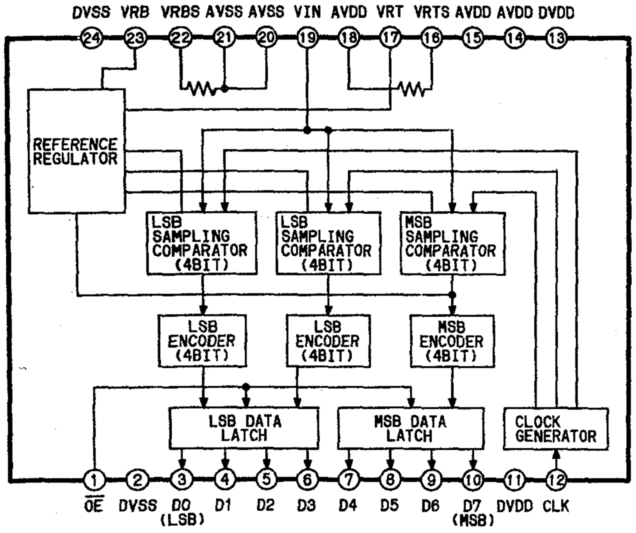

(TOP VIEW)
24
17
25
16
32
9
1
8

BLOCK DIAGRAM


DVSS 28
OE 30
DVSS 31
D0 (LSB) 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
D7 (MSB) 8
DVDD 10
TEST (OPEN) 11
CLK 12
TEST (OPEN) 9
NC 32
LOWER DATA LATCH
UPPER DATA LATCH
LOWER ENCODER (4BIT)
LOWER ENCODER (4BIT)
UPPER ENCODER (4BIT)
LOWER SAMPLING COMPARATOR (4BIT)
LOWER SAMPLING COMPARATOR (4BIT)
UPPER SAMPLING COMPARATOR (4BIT)
REFERENCE SUPPLY
CLOCK GENERATOR
D-FF
25 VRBS
24 VRB
23 AVSS
22 AVSS
21 VIN
20 AVDD
19 AVDD
18 VRT
17 VRTS
16 AVDD
15 CLP
14 NC
13 NC
29 CLE
27 CCP
26 VREF

CXD1175AM

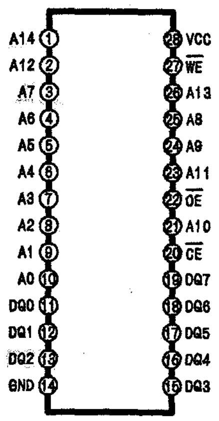
(8BIT 20MSPS VIDEO A/D CONVERTER)


DVSS
VRB
VRBS
AVSS
AVSS
VIN
AVDD
VRT
VRTS
AVDD
AVDD
DVDD
24
23
22
21
20
19
18
17
16
15
14
13
REFERENCE REGULATOR
LSB SAMPLING COMPARATOR (4BIT)
LSB SAMPLING COMPARATOR (4BIT)
MSB SAMPLING COMPARATOR (4BIT)
LSB ENCODER (4BIT)
LSB ENCODER (4BIT)
MSB ENCODER (4BIT)
LSB DATA LATCH
MSB DATA LATCH
CLOCK GENERATOR
1
2
3
4
5
6
7
8
9
10
11
12
OE
DVSS
D0 (LSB)
D1
D2
D3
D4
D5
D6
D7 (MSB)
DVDD
CLK

DS1230Y100

(256K NONVOLATILE SRAM)

PIN ASSIGNMENT


A14 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ0 11
DQ1 12
DQ2 13
GND 14
28 VCC
27 WE
26 A13
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 DQ7
18 DQ6
17 DQ5
16 DQ4
15 DQ3

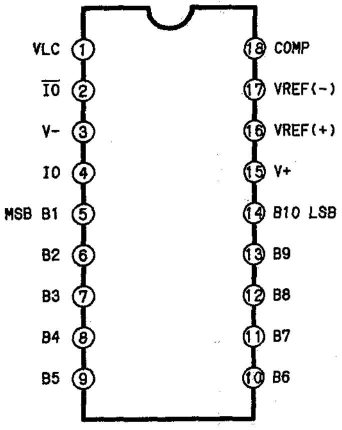
PIN DESCRIPTION

A0-A14	- ADDRESS INPUTS
$\overline{CE}$	- CHIP ENABLE
GND	- GROUND
DQ0-DQ7	- DATA IN/DATA OUT
VCC	- POWER (+5V)
$\overline{WE}$	- WRITE ENABLE
$\overline{OE}$	- OUTPUT ENABLE

DAC10-GX (10-BIT D/A CONVERTER)

(18PIN HERMETIC DIP)

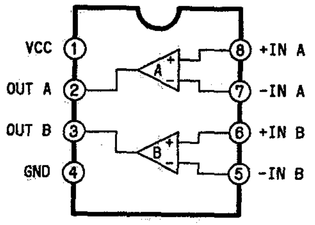
(TOP VIEW)

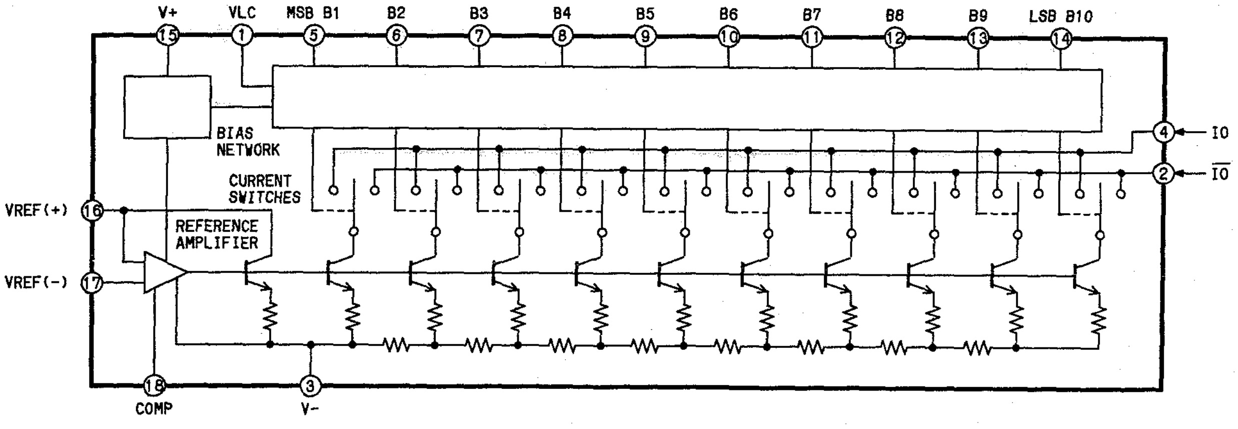

VLC 1
IO 2
V- 3
IO 4
MSB B1 5
B2 6
B3 7
B4 8
B5 9
18 COMP
17 VREF(-)
16 VREF(+)
15 V+
14 B10 LSB
13 B9
12 B8
11 B7
10 B6

DS9637A

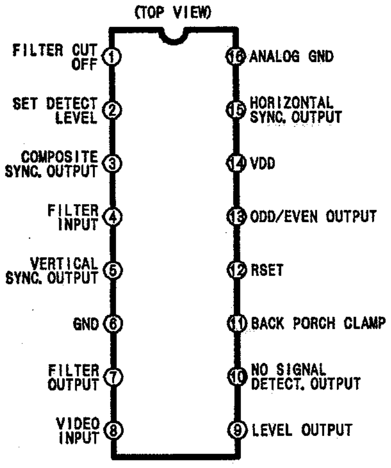
(DUAL DIFFERENTIAL LINE RECEIVER)

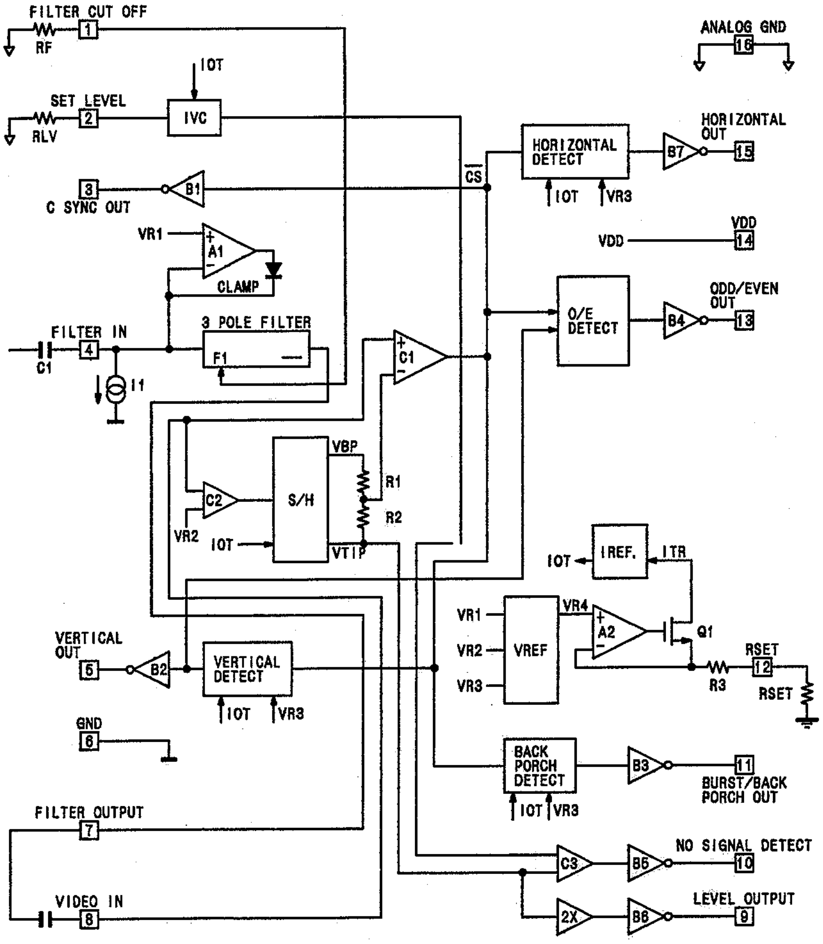
(TOP VIEW)


VCC 1
OUT A 2
OUT B 3
GND 4
8 +IN A
7 -IN A
6 +IN B
5 -IN B
A
B


V+
VLC
MSB B1
B2
B3
B4
B5
B6
B7
B8
B9
LSB B10
15
1
5
6
7
8
9
10
11
12
13
14
BIAS NETWORK
CURRENT SWITCHES
REFERENCE AMPLIFIER
VREF(+) 16
VREF(-) 17
4 IO
2 IO
18 COMP
3 V-

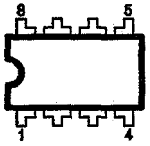
EL4583CS
(VIDEO SYNC SEPARATOR)


(TOP VIEW)
FILTER CUT OFF ①
SET DETECT LEVEL ②
COMPOSITE SYNC. OUTPUT ③
FILTER INPUT ④
VERTICAL SYNC. OUTPUT ⑤
GND ⑥
FILTER OUTPUT ⑦
VIDEO INPUT ⑧
⑯ ANALOG GND
⑮ HORIZONTAL SYNC. OUTPUT
⑭ VDD
⑬ ODD/EVEN OUTPUT
⑫ RSET
⑪ BACK PORCH CLAMP
⑩ NO SIGNAL DETECT. OUTPUT
⑨ LEVEL OUTPUT

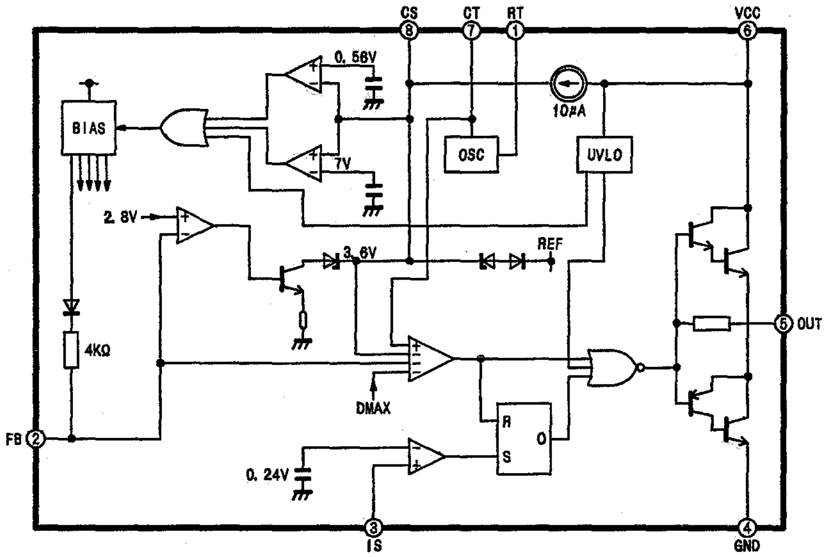

FILTER CUT OFF
RF
1
ANALOG GND
16
IOT
SET LEVEL
RLV
2
IVC
HORIZONTAL OUT
HORIZONTAL DETECT
B7
15
CS
3
B1
C SYNC OUT
IOT
VR3
VDD
VDD
14
VR1
A1
CLAMP
ODD/EVEN OUT
O/E DETECT
B4
13
FILTER IN
4
C1
3 POLE FILTER
F1
C1
I1
VBP
R1
R2
C2
S/H
VR2
IOT
VTIP
IOT
IREF.
ITR
VR4
VR1
A2
Q1
VR2
VREF
RSET
R3
12
VR3
RSET
VERTICAL OUT
5
B2
VERTICAL DETECT
IOT
VR3
GND
6
BACK PORCH DETECT
B3
11
BURST/BACK PORCH OUT
IOT
VR3
FILTER OUTPUT
7
NO SIGNAL DETECT
C3
B5
10
VIDEO IN
8
LEVEL OUTPUT
2X
B6
9

FA5311P
(PWM SWITCHING POWER CONTROL)

(TOP VIEW)

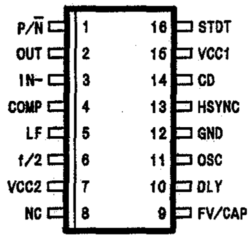


BLOCK DIAGRAM

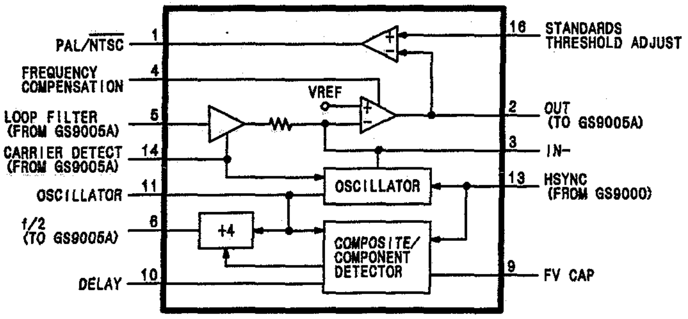

CS
8
CT
7
RT
1
VCC
6
0.56V
BIAS
10μA
OSC
UVLO
7V
2.8V
3.6V
REF
4KΩ
5 OUT
DMAX
FB 2
R
S
Q
0.24V
3
IS
4
GND

GS9010
(SERIAL DIGITAL AUTO TUNING SUB SYSTEM)

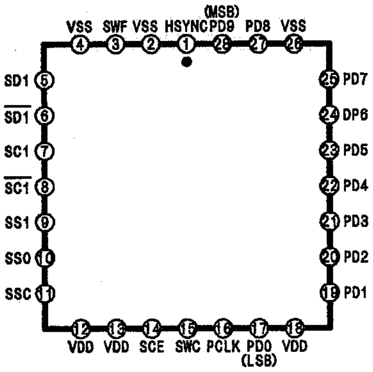
(TOP VIEW)


P/N̄ 1
OUT 2
IN− 3
COMP 4
LF 5
f/2 6
VCC2 7
NC 8
16 STDT
15 VCC1
14 CD
13 HSYNC
12 GND
11 OSC
10 DLY
9 FV/CAP

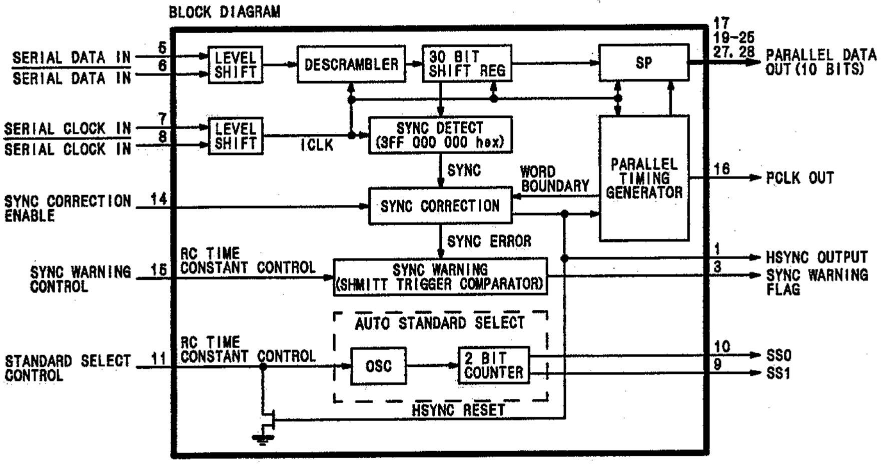
BLOCK DIAGRAM


PAL/$\overline{\text{NTSC}}$ 1
FREQUENCY COMPENSATION 4
LOOP FILTER (FROM GS9005A) 5
CARRIER DETECT (FROM GS9005A) 14
OSCILLATOR 11
f/2 (TO GS9005A) 6
DELAY 10
16 STANDARDS THRESHOLD ADJUST
2 OUT (TO GS9005A)
3 IN−
13 HSYNC (FROM GS9000)
9 FV CAP
VREF
OSCILLATOR
÷4
COMPOSITE/ COMPONENT DETECTOR

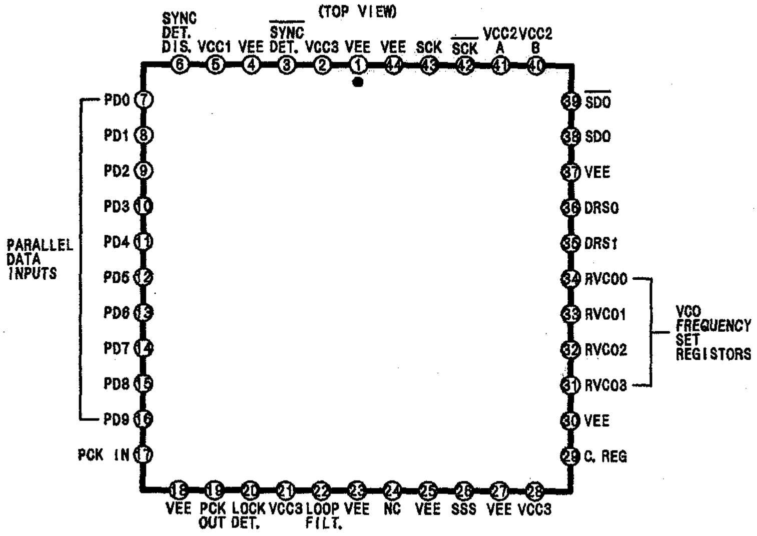
GS9000
(SERIAL DIGITAL DECODER)
(TOP VIEW)

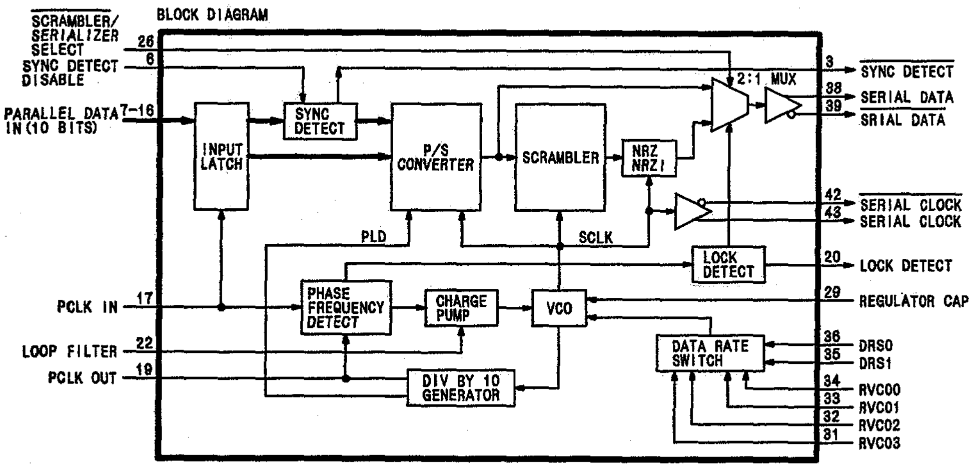

(MSB)
VSS ④
SWF ③
VSS ②
HSYNC ①
PD9 ㉘
PD8 ㉗
VSS ㉖
SD1 ⑤
$\overline{\text{SD1}}$ ⑥
SC1 ⑦
$\overline{\text{SC1}}$ ⑧
SS1 ⑨
SS0 ⑩
SSC ⑪
㉕ PD7
㉔ DP6
㉓ PD5
㉒ PD4
㉑ PD3
⑳ PD2
⑲ PD1
⑫ VDD
⑬ VDD
⑭ SCE
⑮ SWC
⑯ PCLK
⑰ PD0
⑱ VDD
(LSB)

BLOCK DIAGRAM

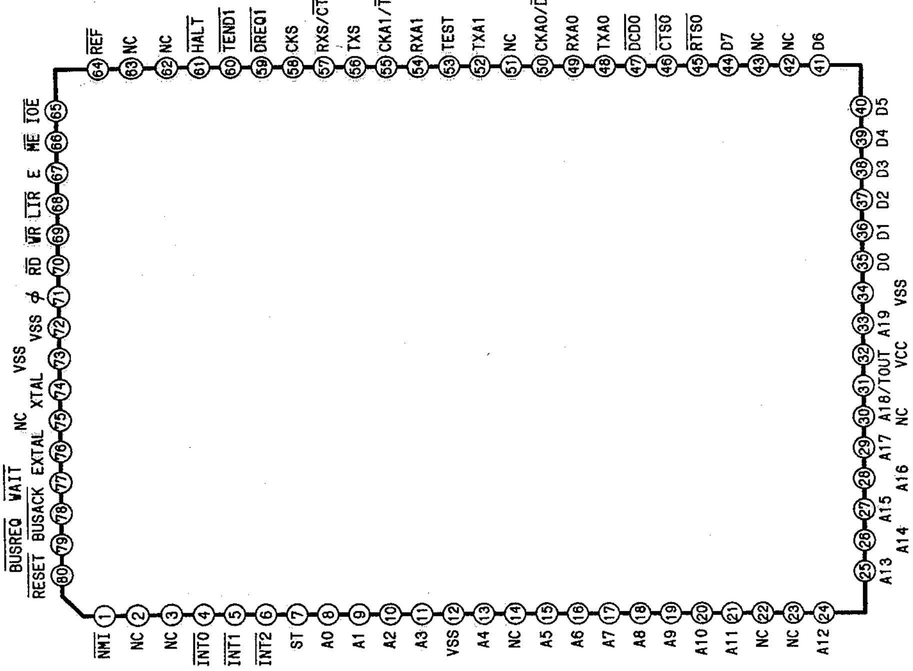

SERIAL DATA IN
$\overline{\text{SERIAL DATA IN}}$
5
6
LEVEL SHIFT
DESCRAMBLER
30 BIT SHIFT REG
SP
17
19-25
27, 28
PARALLEL DATA OUT (10 BITS)
SERIAL CLOCK IN
$\overline{\text{SERIAL CLOCK IN}}$
7
8
LEVEL SHIFT
ICLK
SYNC DETECT (3FF 000 000 hex)
PARALLEL TIMING GENERATOR
SYNC
WORD BOUNDARY
16
PCLK OUT
SYNC CORRECTION ENABLE
14
SYNC CORRECTION
SYNC ERROR
SYNC WARNING CONTROL
15
RC TIME CONSTANT CONTROL
SYNC WARNING (SHMITT TRIGGER COMPARATOR)
1
HSYNC OUTPUT
3
SYNC WARNING FLAG
AUTO STANDARD SELECT
STANDARD SELECT CONTROL
11
RC TIME CONSTANT CONTROL
OSC
2 BIT COUNTER
10
SS0
9
SS1
HSYNC RESET

GS9002
(SERIAL DIGITAL ENCODER)
(TOP VIEW)


SYNC DET. DIS. ⑥
VCC1 ⑤
VEE ④
SYNC DET. ③
VCC3 ②
VEE ①
VEE ㊹
SCK ㊸
SCK ㊷
VCC2 A ㊶
VCC2 B ㊵
PARALLEL DATA INPUTS
PD0 ⑦
PD1 ⑧
PD2 ⑨
PD3 ⑩
PD4 ⑪
PD5 ⑫
PD6 ⑬
PD7 ⑭
PD8 ⑮
PD9 ⑯
PCK IN ⑰
㊴ SDO
㊳ SDO
㊲ VEE
㊱ DRS0
㉟ DRS1
㉞ RVCO0
㉝ RVCO1
㉜ RVCO2
㉛ RVCO3
㉚ VEE
㉙ C. REG
VCO FREQUENCY SET REGISTORS
⑱ VEE
⑲ PCK OUT
⑳ LOCK DET.
㉑ VCC3
㉒ LOOP FILT.
㉓ VEE
㉔ NC
㉕ VEE
㉖ SSS
㉗ VEE
㉘ VCC3

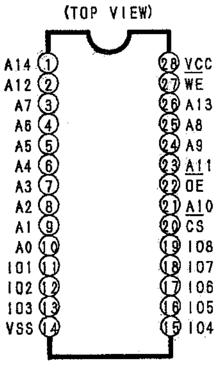

BLOCK DIAGRAM
SCRAMBLER/ SERIALIZER SELECT 26
SYNC DETECT DISABLE 6
PARALLEL DATA IN (10 BITS) 7–16
INPUT LATCH
SYNC DETECT
P/S CONVERTER
SCRAMBLER
NRZ NRZI
2:1 MUX
PLD
SCLK
LOCK DETECT
PHASE FREQUENCY DETECT
CHARGE PUMP
VCO
DIV BY 10 GENERATOR
DATA RATE SWITCH
PCLK IN 17
LOOP FILTER 22
PCLK OUT 19
3 SYNC DETECT
38 SERIAL DATA
39 SRIAL DATA
42 SERIAL CLOCK
43 SERIAL CLOCK
20 LOCK DETECT
29 REGULATOR CAP
36 DRS0
35 DRS1
34 RVCO0
33 RVCO1
32 RVCO2
31 RVCO3

HD64180
(8BIT MC)

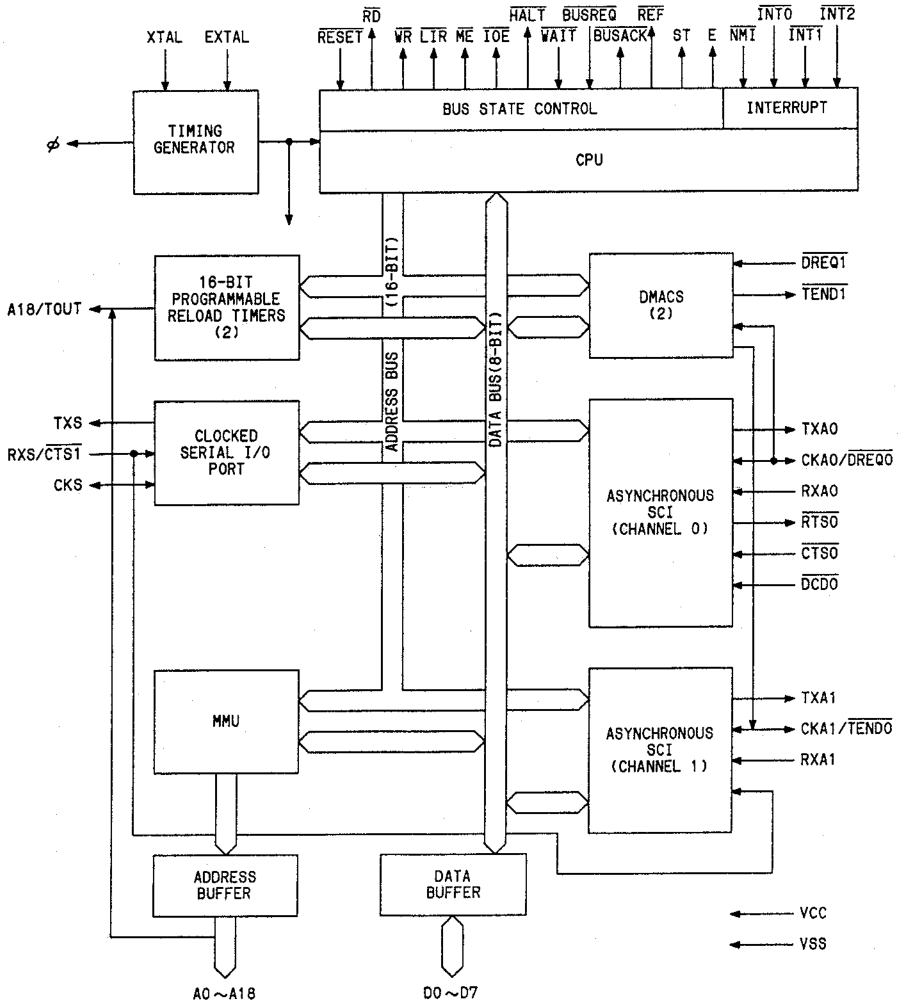


1 $\overline{NMI}$
2 NC
3 NC
4 $\overline{INT0}$
5 $\overline{INT1}$
6 $\overline{INT2}$
7 ST
8 A0
9 A1
10 A2
11 A3
12 VSS
13 A4
14 NC
15 A5
16 A6
17 A7
18 A8
19 A9
20 A10
21 A11
22 NC
23 NC
24 A12
25 A13
26 A14
27 A15
28 A16
29 A17
30 NC
31 A18/TOUT
32 VCC
33 A19
34 VSS
35 D0
36 D1
37 D2
38 D3
39 D4
40 D5
41 D6
42 NC
43 NC
44 D7
45 $\overline{RTS0}$
46 $\overline{CTS0}$
47 $\overline{DCD0}$
48 TXA0
49 RXA0
50 CKA0/$\overline{DREQ0}$
51 NC
52 TXA1
53 TEST
54 RXA1
55 CKA1/$\overline{TEND0}$
56 TXS
57 RXS/$\overline{CTS1}$
58 CKS
59 $\overline{DREQ1}$
60 $\overline{TEND1}$
61 $\overline{HALT}$
62 NC
63 NC
64 $\overline{REF}$
65 $\overline{IOE}$
66 $\overline{ME}$
67 E
68 $\overline{LIR}$
69 $\overline{WR}$
70 $\overline{RD}$
71 φ
72 VSS
73 VSS
74 XTAL
75 NC
76 EXTAL
77 $\overline{WAIT}$
78 $\overline{BUSACK}$
79 $\overline{BUSREQ}$
80 $\overline{RESET}$

K6256BLG7L
K6256CLG7L



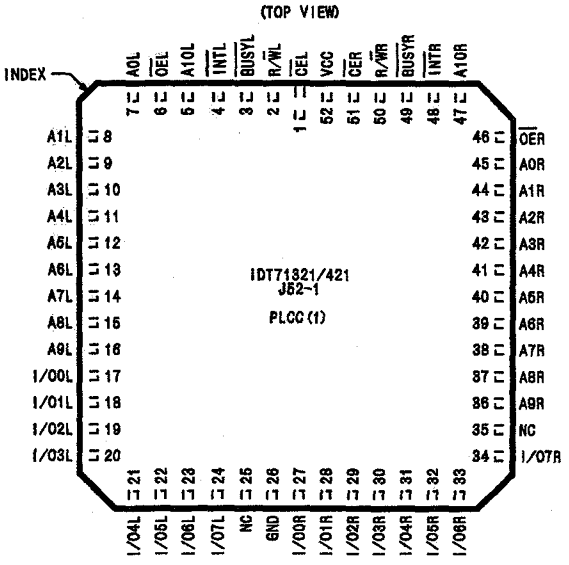
(TOP VIEW)
A14 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
IO1 11
IO2 12
IO3 13
VSS 14
IO4 15
IO5 16
IO6 17
IO7 18
IO8 19
$\overline{CS}$ 20
A10 21
$\overline{OE}$ 22
A11 23
A9 24
A8 25
A13 26
$\overline{WE}$ 27
VCC 28

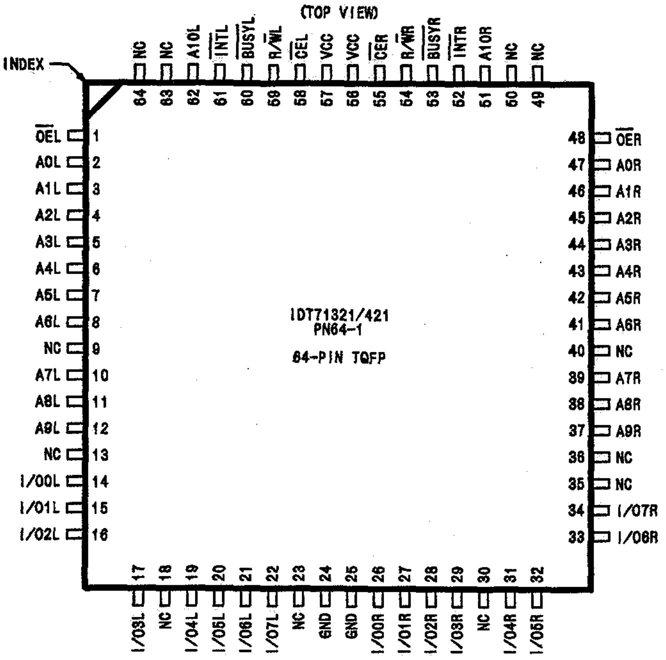


XTAL
EXTAL
$\overline{RESET}$
$\overline{RD}$
$\overline{WR}$
$\overline{LIR}$
$\overline{ME}$
$\overline{IOE}$
$\overline{HALT}$
$\overline{WAIT}$
$\overline{BUSREQ}$
$\overline{BUSACK}$
$\overline{REF}$
ST
E
$\overline{NMI}$
$\overline{INT0}$
$\overline{INT1}$
$\overline{INT2}$
TIMING GENERATOR
φ
BUS STATE CONTROL
INTERRUPT
CPU
16-BIT PROGRAMMABLE RELOAD TIMERS (2)
A18/TOUT
(16-BIT) ADDRESS BUS
DATA BUS(8-BIT)
DMACS (2)
$\overline{DREQ1}$
$\overline{TEND1}$
TXS
RXS/$\overline{CTS1}$
CKS
CLOCKED SERIAL I/O PORT
ASYNCHRONOUS SCI (CHANNEL 0)
TXA0
CKA0/$\overline{DREQ0}$
RXA0
$\overline{RTS0}$
$\overline{CTS0}$
$\overline{DCD0}$
MMU
ASYNCHRONOUS SCI (CHANNEL 1)
TXA1
CKA1/$\overline{TEND0}$
RXA1
ADDRESS BUFFER
DATA BUFFER
VCC
VSS
A0～A18
D0～D7

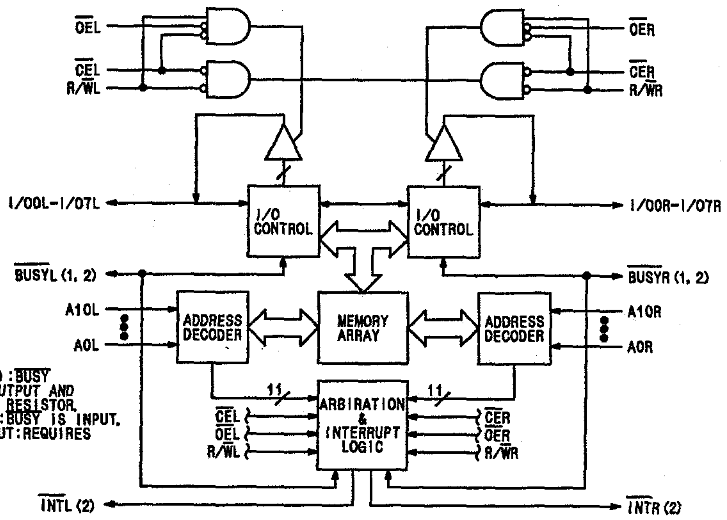
IDT71321A55T

(CMOS DUAL-PORT RAM 16K (2Kx8 BIT) WITH INTERRUPTS)


(TOP VIEW)
INDEX
A0L 7
OEL 6
A10L 5
INTL 4
BUSYL 3
R/WL 2
CEL 1
VCC 52
CER 51
R/WR 50
BUSYR 49
INTR 48
A10R 47
A1L 8
A2L 9
A3L 10
A4L 11
A5L 12
A6L 13
A7L 14
A8L 15
A9L 16
I/O0L 17
I/O1L 18
I/O2L 19
I/O3L 20
46 OER
45 A0R
44 A1R
43 A2R
42 A3R
41 A4R
40 A5R
39 A6R
38 A7R
37 A8R
36 A9R
35 NC
34 I/O7R
21 I/O4L
22 I/O5L
23 I/O6L
24 I/O7L
25 NC
26 GND
27 I/O0R
28 I/O1R
29 I/O2R
30 I/O3R
31 I/O4R
32 I/O5R
33 I/O6R
IDT71321/421
J52-1
PLCC (1)

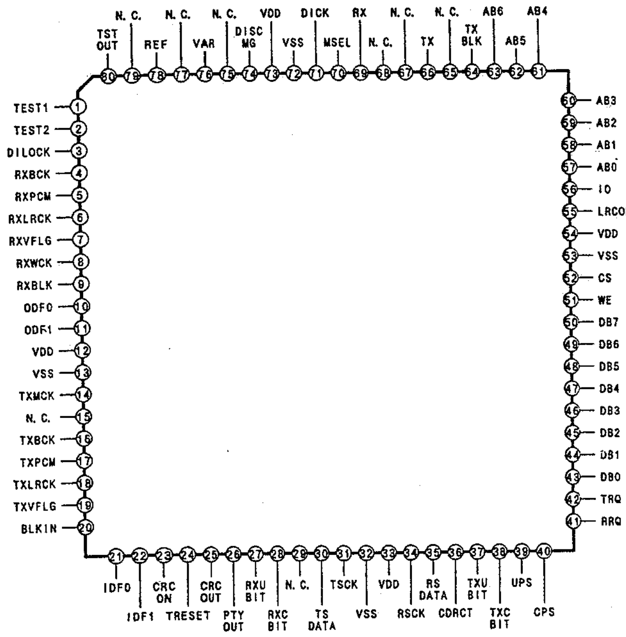

(TOP VIEW)
INDEX
NC 64
NC 63
A10L 62
INTL 61
BUSYL 60
R/WL 59
CEL 58
VCC 57
VCC 56
CER 55
R/WR 54
BUSYR 53
INTR 52
A10R 51
NC 50
NC 49
OEL 1
A0L 2
A1L 3
A2L 4
A3L 5
A4L 6
A5L 7
A6L 8
NC 9
A7L 10
A8L 11
A9L 12
NC 13
I/O0L 14
I/O1L 15
I/O2L 16
48 OER
47 A0R
46 A1R
45 A2R
44 A3R
43 A4R
42 A5R
41 A6R
40 NC
39 A7R
38 A8R
37 A9R
36 NC
35 NC
34 I/O7R
33 I/O6R
17 I/O3L
18 NC
19 I/O4L
20 I/O5L
21 I/O6L
22 I/O7L
23 NC
24 GND
25 GND
26 I/O0R
27 I/O1R
28 I/O2R
29 I/O3R
30 NC
31 I/O4R
32 I/O5R
IDT71321/421
PN64-1
64-PIN TQFP

BLOCK DIAGRAM

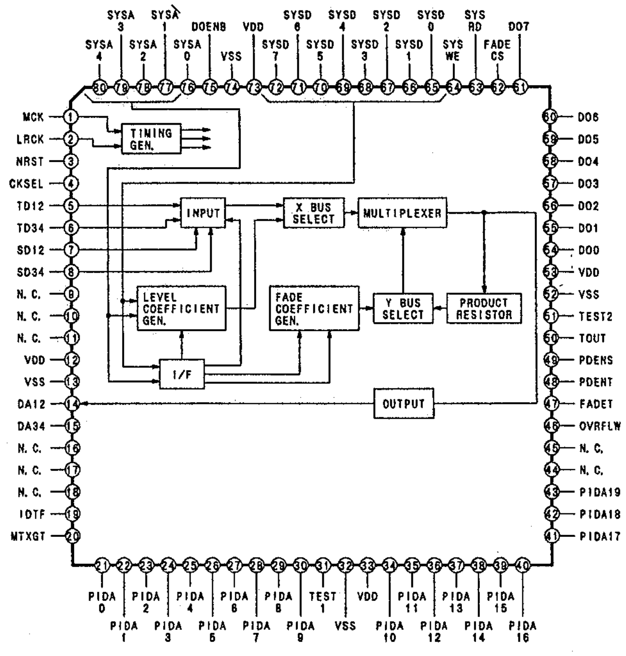

OEL
CEL
R/WL
OER
CER
R/WR
I/O0L-I/O7L
I/O CONTROL
I/O CONTROL
I/O0R-I/O7R
BUSYL (1, 2)
BUSYR (1, 2)
A10L
A0L
ADDRESS DECODER
MEMORY ARRAY
ADDRESS DECODER
A10R
A0R
11
11
ARBIRATION & INTERRUPT LOGIC
CEL
OEL
R/WL
CER
OER
R/WR
INTL (2)
INTR (2)

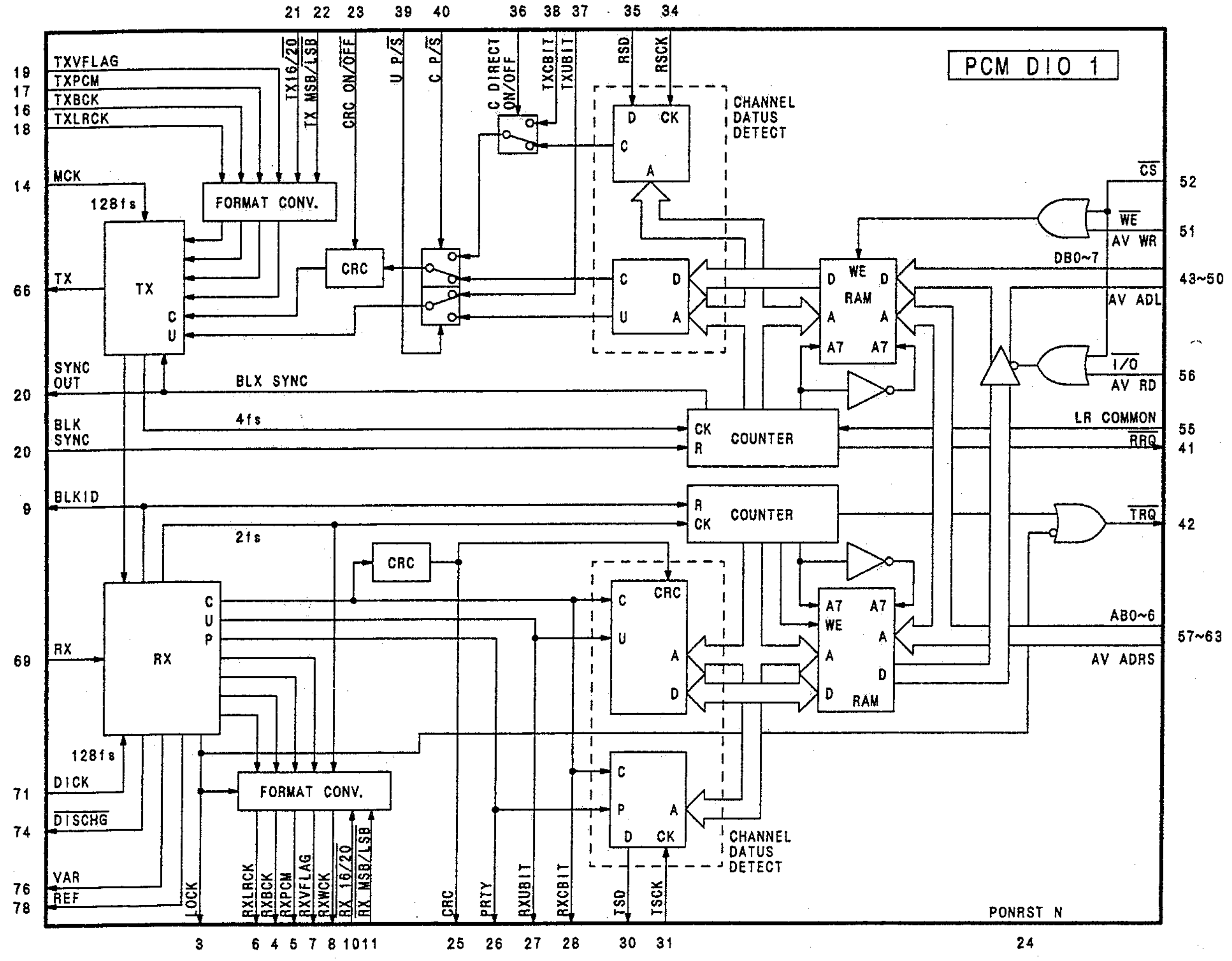
NOTES:
1. IDT71321 (MASTER) : BUSY IS OPEN DRAIN OUTPUT AND REQUIRES PULLUP RESISTOR.
IDT71421 (SLAVE) : BUSY IS INPUT.
2. OPEN DRAIN OUTPUT: REQUIRES PULLUP RESISTOR.

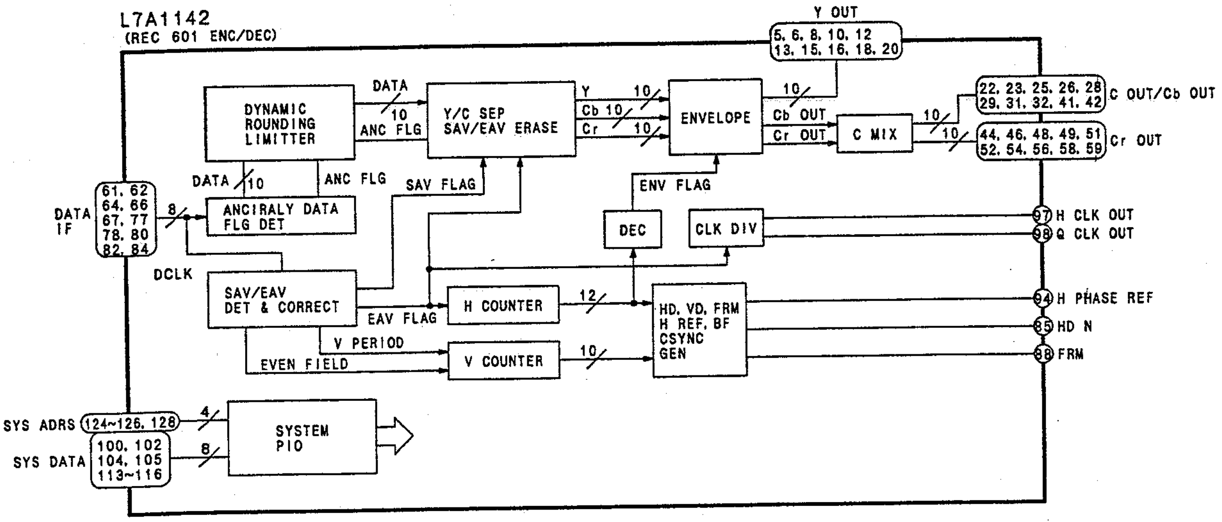
L7A0541
(DIGITAL AUDIO I/F)
(TOP VIEW)


TEST1 1
TEST2 2
DILOCK 3
RXBCK 4
RXPCM 5
RXLRCK 6
RXVFLG 7
RXWCK 8
RXBLK 9
ODF0 10
ODF1 11
VDD 12
VSS 13
TXMCK 14
N. C. 15
TXBCK 16
TXPCM 17
TXLRCK 18
TXVFLG 19
BLKIN 20
IDF0 21
IDF1 22
CRC ON 23
TRESET 24
CRC OUT 25
PTY OUT 26
RXU BIT 27
RXC BIT 28
N. C. 29
TS DATA 30
TSCK 31
VSS 32
VDD 33
RSCK 34
RS DATA 35
CDRCT 36
TXU BIT 37
TXC BIT 38
UPS 39
CPS 40
RRQ 41
TRQ 42
DB0 43
DB1 44
DB2 45
DB3 46
DB4 47
DB5 48
DB6 49
DB7 50
WE 51
CS 52
VSS 53
VDD 54
LRCON 55
IO 56
AB0 57
AB1 58
AB2 59
AB3 60
AB4 61
AB5 62
AB6 63
TX BLK 64
N. C. 65
TX 66
N. C. 67
N. C. 68
RX 69
MSEL 70
DICK 71
VSS 72
VDD 73
DISC MG 74
N. C. 75
VAR 76
N. C. 77
REF 78
N. C. 79
TST OUT 80

L7A0651
(AUDIO FADE)
(TOP VIEW)


MCK 1
LRCK 2
NRST 3
CKSEL 4
TD12 5
TD34 6
SD12 7
SD34 8
N. C. 9
N. C. 10
N. C. 11
VDD 12
VSS 13
DA12 14
DA34 15
N. C. 16
N. C. 17
N. C. 18
IDTF 19
MTXGT 20
PIDA 0 21
PIDA 1 22
PIDA 2 23
PIDA 3 24
PIDA 4 25
PIDA 5 26
PIDA 6 27
PIDA 7 28
PIDA 8 29
PIDA 9 30
TEST 1 31
VSS 32
VDD 33
PIDA 10 34
PIDA 11 35
PIDA 12 36
PIDA 13 37
PIDA 14 38
PIDA 15 39
PIDA 16 40
PIDA17 41
PIDA18 42
PIDA19 43
N. C. 44
N. C. 45
OVRFLW 46
FADET 47
PDENT 48
PDENS 49
TOUT 50
TEST2 51
VSS 52
VDD 53
DO0 54
DO1 55
DO2 56
DO3 57
DO4 58
DO5 59
DO6 60
DO7 61
FADE CS 62
SYS RD 63
SYS WE 64
SYSD 0 65
SYSD 1 66
SYSD 2 67
SYSD 3 68
SYSD 4 69
SYSD 5 70
SYSD 6 71
SYSD 7 72
VSS 73
VDD 74
DOENB 75
SYSA 0 76
SYSA 1 77
SYSA 2 78
SYSA 3 79
SYSA 4 80
TIMING GEN.
INPUT
X BUS SELECT
MULTIPLEXER
LEVEL COEFFICIENT GEN.
FADE COEFFICIENT GEN.
Y BUS SELECT
PRODUCT RESISTOR
I/F
OUTPUT

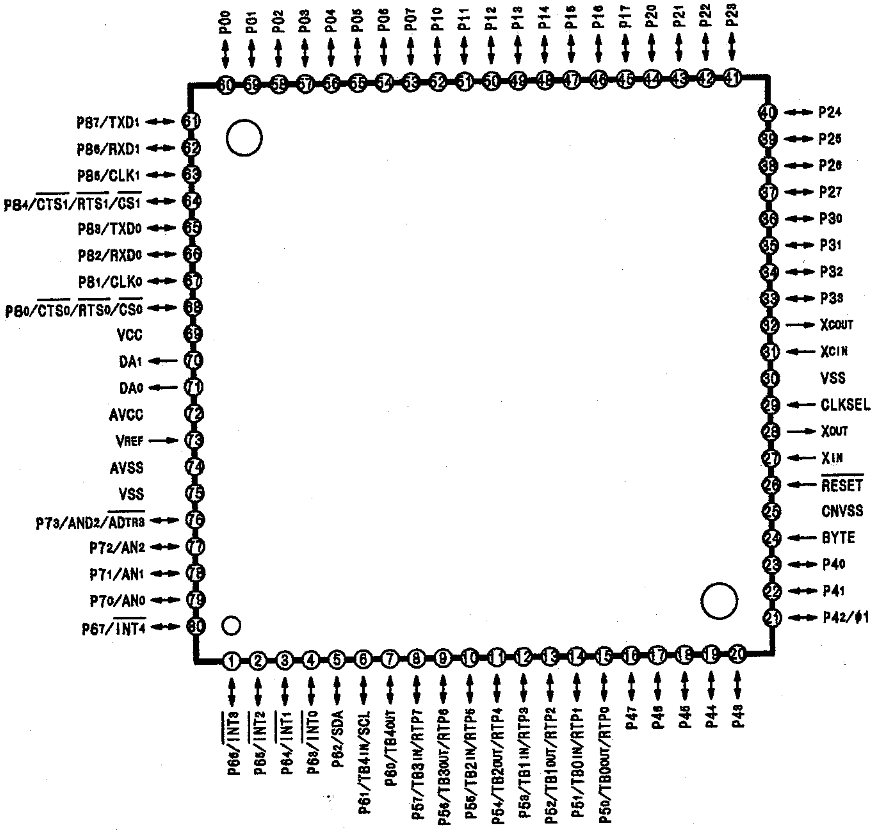

PCM DIO 1
21 22 23 39 40 36 38 37 35 34
TX16/20
TX MSB/LSB
CRC ON/OFF
U P/S
C P/S
C DIRECT ON/OFF
TXCBIT
TXUBIT
RSD
RSCK
19 TXVFLAG
17 TXPCM
16 TXBCK
18 TXLRCK
14 MCK
128fs
FORMAT CONV.
66 TX
TX
C
U
CRC
CHANNEL DATUS DETECT
D CK
C
A
C D
U A
52 CS
51 WE
AV WR
DB0~7
43~50
WE
D D
RAM
A A
A7 A7
AV ADL
56 I/O
AV RD
SYNC OUT
20
BLX SYNC
4fs
CK
R
COUNTER
LR COMMON 55
RRQ 41
BLK SYNC
20
9 BLKID
R
CK
COUNTER
TRQ 42
21fs
CRC
CRC
C
U
A
D
A7 A7
WE
A
A
D
D RAM
AB0~6
57~63
AV ADRS
69 RX
RX
C
U
P
128fs
71 DICK
74 DISCHG
76 VAR
78 REF
FORMAT CONV.
C
P A
D CK
CHANNEL DATUS DETECT
LOCK
RXLRCK
RXBCK
RXPCM
RXVFLAG
RXWCK
RX 16/20
RX MSB/LSB
CRC
PRTY
RXUBIT
RXCBIT
TSD
TSCK
PONRST N
3 6 4 5 7 8 10 11 25 26 27 28 30 31 24



L7A1142
(REC 601 ENC/DEC)

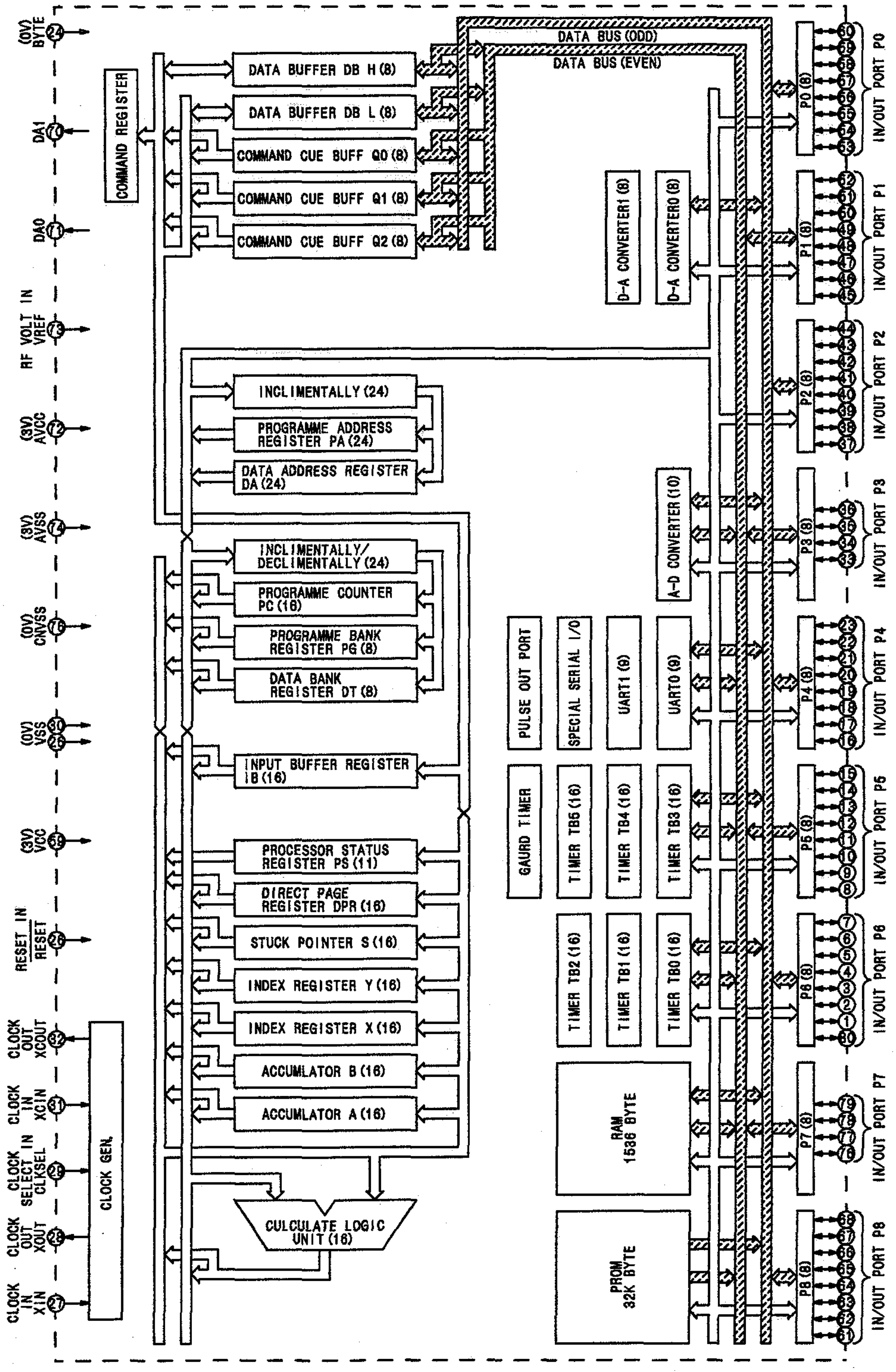
Y OUT
5, 6, 8, 10, 12
13, 15, 16, 18, 20
DYNAMIC
ROUNDING
LIMITTER
DATA
10
ANC FLG
Y/C SEP
SAV/EAV ERASE
Y
Cb
Cr
10
10
10
ENVELOPE
10
Cb OUT
Cr OUT
C MIX
10
10
22, 23, 25, 26, 28
29, 31, 32, 41, 42
C OUT/Cb OUT
44, 46, 48, 49, 51
52, 54, 56, 58, 59
Cr OUT
DATA
10
ANC FLG
SAV FLAG
ENV FLAG
DATA
IF
61, 62
64, 66
67, 77
78, 80
82, 84
8
ANCIRALY DATA
FLG DET
DEC
CLK DIV
97 H CLK OUT
98 Q CLK OUT
DCLK
SAV/EAV
DET & CORRECT
EAV FLAG
H COUNTER
12
HD, VD, FRM
H REF, BF
CSYNC
GEN
94 H PHASE REF
85 HD N
88 FRM
V PERIOD
EVEN FIELD
V COUNTER
10
SYS ADRS
124~126, 128
4
SYSTEM
PIO
SYS DATA
100, 102
104, 105
113~116
8

M37709E4LGP
(SINGLE CHIP 16 BITS MICROCOMPUTOR)
(TOP VIEW)



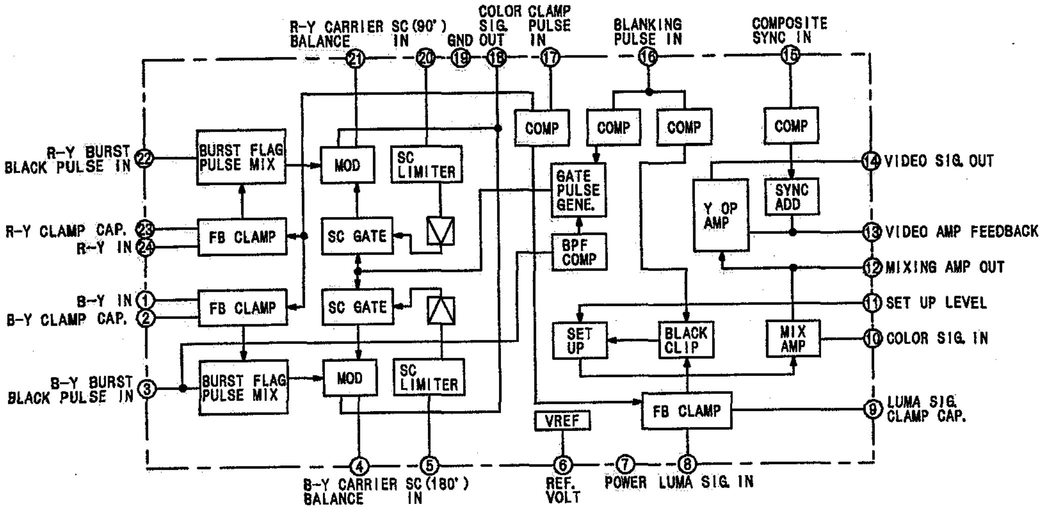
P00 60
P01 59
P02 58
P03 57
P04 56
P05 55
P06 54
P07 53
P10 52
P11 51
P12 50
P13 49
P14 48
P15 47
P16 46
P17 45
P20 44
P21 43
P22 42
P23 41
P87/TXD1 61
P86/RXD1 62
P85/CLK1 63
P84/CTS1/RTS1/CS1 64
P83/TXD0 65
P82/RXD0 66
P81/CLK0 67
P80/CTS0/RTS0/CS0 68
VCC 69
DA1 70
DA0 71
AVCC 72
VREF 73
AVSS 74
VSS 75
P73/AND2/ADTRG 76
P72/AN2 77
P71/AN1 78
P70/AN0 79
P67/INT4 80
40 P24
39 P25
38 P26
37 P27
36 P30
35 P31
34 P32
33 P33
32 XCOUT
31 XCIN
30 VSS
29 CLKSEL
28 XOUT
27 XIN
26 RESET
25 CNVSS
24 BYTE
23 P40
22 P41
21 P42/φ1
1 P66/INT3
2 P65/INT2
3 P64/INT1
4 P63/INT0
5 P62/SDA
6 P61/TB4IN/SCL
7 P60/TB4OUT
8 P57/TB3IN/RTP7
9 P56/TB3OUT/RTP6
10 P55/TB2IN/RTP5
11 P54/TB2OUT/RTP4
12 P53/TB1IN/RTP3
13 P52/TB1OUT/RTP2
14 P51/TB0IN/RTP1
15 P50/TB0OUT/RTP0
16 P47
17 P46
18 P45
19 P44
20 P43

BLOCK DIAGRAM M37709E4LGP


(0V) BYTE ㉔
DA1 70
DA0 71
RF VOLT IN VREF 73
(3V) AVCC 72
(3V) AVSS 74
(0V) CNVSS 76
(0V) VSS 30 26
(3V) VCC 59
RESET IN RESET 26
CLOCK OUT XCOUT 32
CLOCK IN XCIN 31
CLOCK SELECT IN CLKSEL 29
CLOCK OUT XOUT 28
CLOCK IN XIN 27
CLOCK GEN.
COMMAND REGISTER
DATA BUFFER DB H (8)
DATA BUFFER DB L (8)
COMMAND CUE BUFF Q0 (8)
COMMAND CUE BUFF Q1 (8)
COMMAND CUE BUFF Q2 (8)
DATA BUS (ODD)
DATA BUS (EVEN)
INCLIMENTALLY (24)
PROGRAMME ADDRESS REGISTER PA (24)
DATA ADDRESS REGISTER DA (24)
INCLIMENTALLY/ DECLIMENTALLY (24)
PROGRAMME COUNTER PC (16)
PROGRAMME BANK REGISTER PG (8)
DATA BANK REGISTER DT (8)
INPUT BUFFER REGISTER IB (16)
PROCESSOR STATUS REGISTER PS (11)
DIRECT PAGE REGISTER DPR (16)
STUCK POINTER S (16)
INDEX REGISTER Y (16)
INDEX REGISTER X (16)
ACCUMLATOR B (16)
ACCUMLATOR A (16)
CULCULATE LOGIC UNIT (16)
D-A CONVERTER1 (8)
D-A CONVERTER0 (8)
A-D CONVERTER (10)
PULSE OUT PORT
SPECIAL SERIAL I/O
UART1 (9)
UART0 (9)
GAURD TIMER
TIMER TB5 (16)
TIMER TB4 (16)
TIMER TB3 (16)
TIMER TB2 (16)
TIMER TB1 (16)
TIMER TB0 (16)
RAM 1536 BYTE
PROM 32K BYTE
P0 (8)
P1 (8)
P2 (8)
P3 (8)
P4 (8)
P5 (8)
P6 (8)
P7 (8)
P8 (8)
60 59 58 57 56 55 54 53
52 51 50 49 48 47 46 45
44 43 42 41 40 39 38 37
36 35 34 33
23 22 21 20 19 18 17 16
15 14 13 12 11 10 9 8
7 6 5 4 3 2 1 80
79 78 77 76
68 67 66 65 64 63 62 61
IN/OUT PORT P0
IN/OUT PORT P1
IN/OUT PORT P2
IN/OUT PORT P3
IN/OUT PORT P4
IN/OUT PORT P5
IN/OUT PORT P6
IN/OUT PORT P7
IN/OUT PORT P8

M51272P
(COLOR DIFFERENCE SIGNAL (R-Y, B-Y) ENCODER)

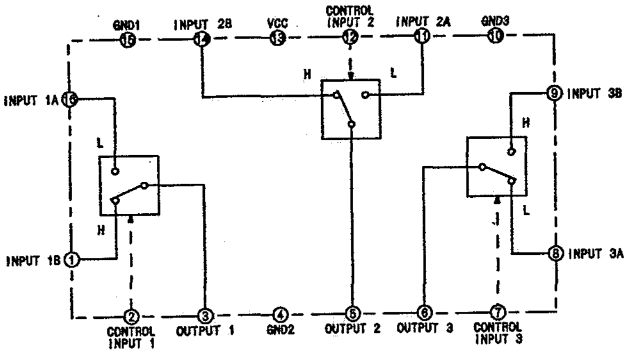
BLOCK DIAGRAM



R-Y CARRIER BALANCE ㉑
SC (90°) IN ⑳
GND ⑲
COLOR SIG. OUT ⑱
CLAMP PULSE IN ⑰
BLANKING PULSE IN ⑯
COMPOSITE SYNC IN ⑮
R-Y BURST BLACK PULSE IN ㉒
R-Y CLAMP CAP. ㉓
R-Y IN ㉔
B-Y IN ①
B-Y CLAMP CAP. ②
B-Y BURST BLACK PULSE IN ③
B-Y CARRIER BALANCE ④
SC (180°) IN ⑤
REF. VOLT ⑥
POWER ⑦
LUMA SIG. IN ⑧
⑭ VIDEO SIG. OUT
⑬ VIDEO AMP FEEDBACK
⑫ MIXING AMP OUT
⑪ SET UP LEVEL
⑩ COLOR SIG. IN
⑨ LUMA SIG. CLAMP CAP.
BURST FLAG PULSE MIX
FB CLAMP
MOD
SC LIMITER
SC GATE
COMP
GATE PULSE GENE.
BPF COMP
Y OP AMP
SYNC ADD
SET UP
BLACK CLIP
MIX AMP
VREF

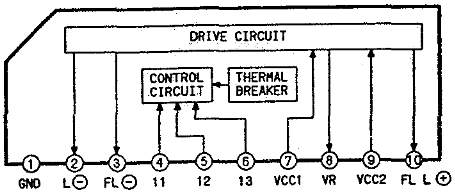
M52055P
(3 CH ANALOG SWITCH)

BLOCK DIAGRAM



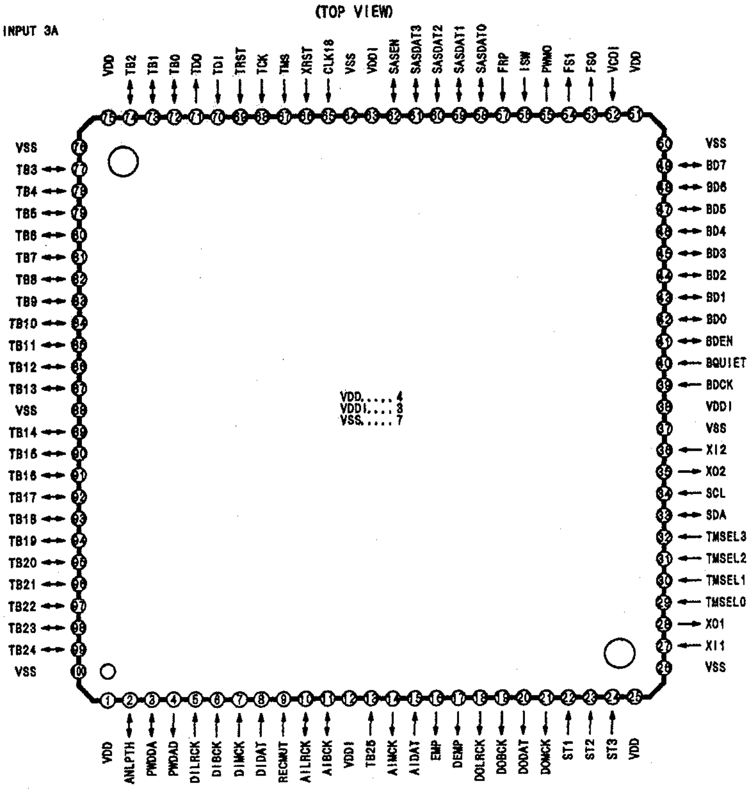
GND1 ⑯
INPUT 2B ⑭
VCC ⑬
CONTROL INPUT 2 ⑫
INPUT 2A ⑪
GND3 ⑩
INPUT 1A ⑮
INPUT 1B ①
⑨ INPUT 3B
⑧ INPUT 3A
H
L
CONTROL INPUT 1 ②
OUTPUT 1 ③
GND2 ④
OUTPUT 2 ⑤
OUTPUT 3 ⑥
CONTROL INPUT 3 ⑦

M54649L



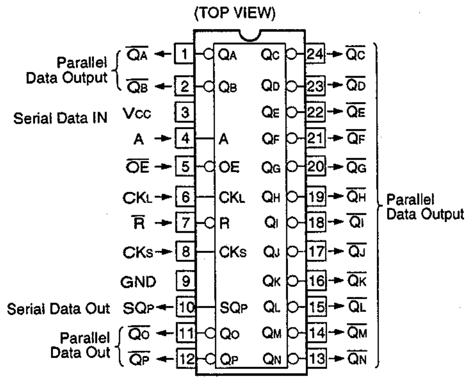
DRIVE CIRCUIT
CONTROL CIRCUIT
THERMAL BREAKER
① GND
② L⊖
③ FL⊖
④ 11
⑤ 12
⑥ 13
⑦ VCC1
⑧ VR
⑨ VCC2
⑩ FL L⊕

M65401FP
(DIGITAL AUDIO SIGNAL PROCESSOR)

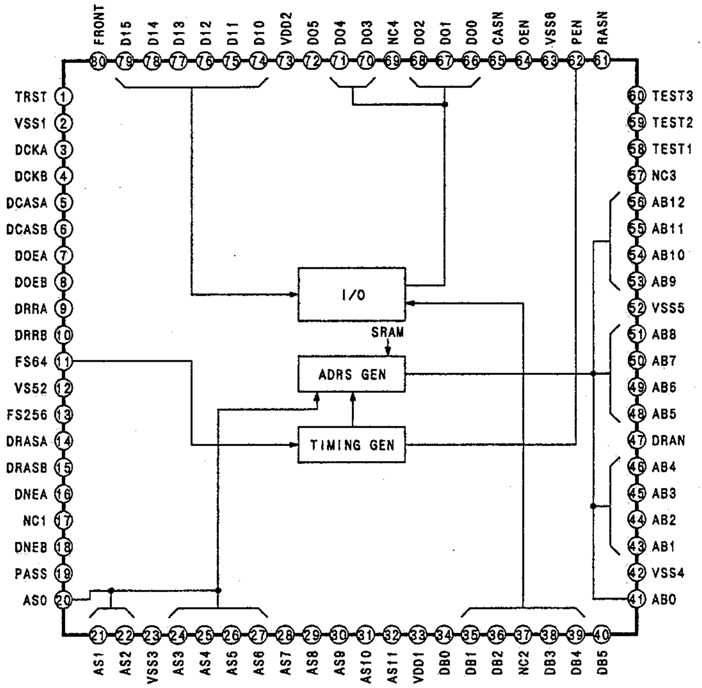


(TOP VIEW)
75 VDD
74 TB2
73 TB1
72 TB0
71 TDO
70 TDI
69 TRST
68 TCK
67 TMS
66 XRST
65 CLK18
64 VSS
63 VDDI
62 SASEN
61 SASDAT3
60 SASDAT2
59 SASDAT1
58 SASDAT0
57 FRP
56 ISW
55 PWMO
54 FS1
53 FS0
52 VCOI
51 VDD
76 VSS
77 TB3
78 TB4
79 TB5
80 TB6
81 TB7
82 TB8
83 TB9
84 TB10
85 TB11
86 TB12
87 TB13
88 VSS
89 TB14
90 TB15
91 TB16
92 TB17
93 TB18
94 TB19
95 TB20
96 TB21
97 TB22
98 TB23
99 TB24
100 VSS
50 VSS
49 BD7
48 BD6
47 BD5
46 BD4
45 BD3
44 BD2
43 BD1
42 BD0
41 BDEN
40 BQUIET
39 BDCK
38 VDDI
37 VSS
36 XI2
35 XO2
34 SCL
33 SDA
32 TMSEL3
31 TMSEL2
30 TMSEL1
29 TMSEL0
28 XO1
27 XI1
26 VSS
VDD.....4
VDDI....3
VSS.....7
1 VDD
2 ANLPTH
3 PWODA
4 PWOAD
5 DILRCK
6 DIBCK
7 DIMCK
8 DIDAT
9 RECMUT
10 AILRCK
11 AIBCK
12 VDDI
13 TB25
14 AIMCK
15 AIDAT
16 EMP
17 DEMP
18 DOLRCK
19 DOBCK
20 DODAT
21 DOMCK
22 ST1
23 ST2
24 ST3
25 VDD

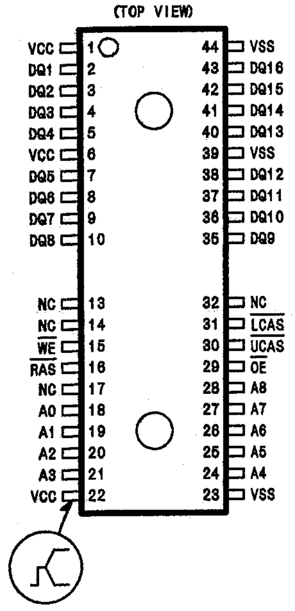
M66311FP
(16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH)


(TOP VIEW)
Parallel Data Output
$\overline{Q_A}$ 1 QA
$\overline{Q_B}$ 2 QB
Serial Data IN
Vcc 3
A 4 A
$\overline{OE}$ 5 OE
CKL 6 CKL
$\overline{R}$ 7 R
CKs 8 CKs
GND 9
Serial Data Out
SQP 10 SQP
Parallel Data Out
$\overline{Q_O}$ 11 QO
$\overline{Q_P}$ 12 QP
24 QC $\overline{Q_C}$
23 QD $\overline{Q_D}$
22 QE $\overline{Q_E}$
21 QF $\overline{Q_F}$
20 QG $\overline{Q_G}$
19 QH $\overline{Q_H}$
18 QI $\overline{Q_I}$
17 QJ $\overline{Q_J}$
16 QK $\overline{Q_K}$
15 QL $\overline{Q_L}$
14 QM $\overline{Q_M}$
13 QN $\overline{Q_N}$
Parallel Data Output

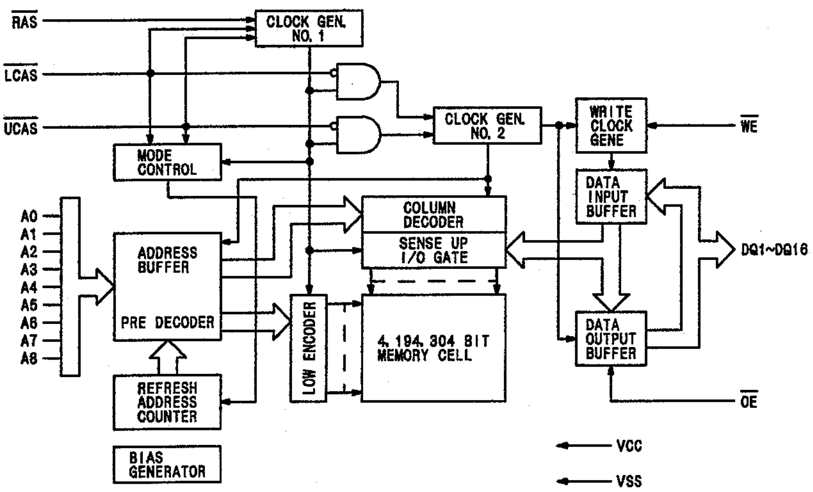
MB621926
(DELAY FOR DIGITAL AUDIO)

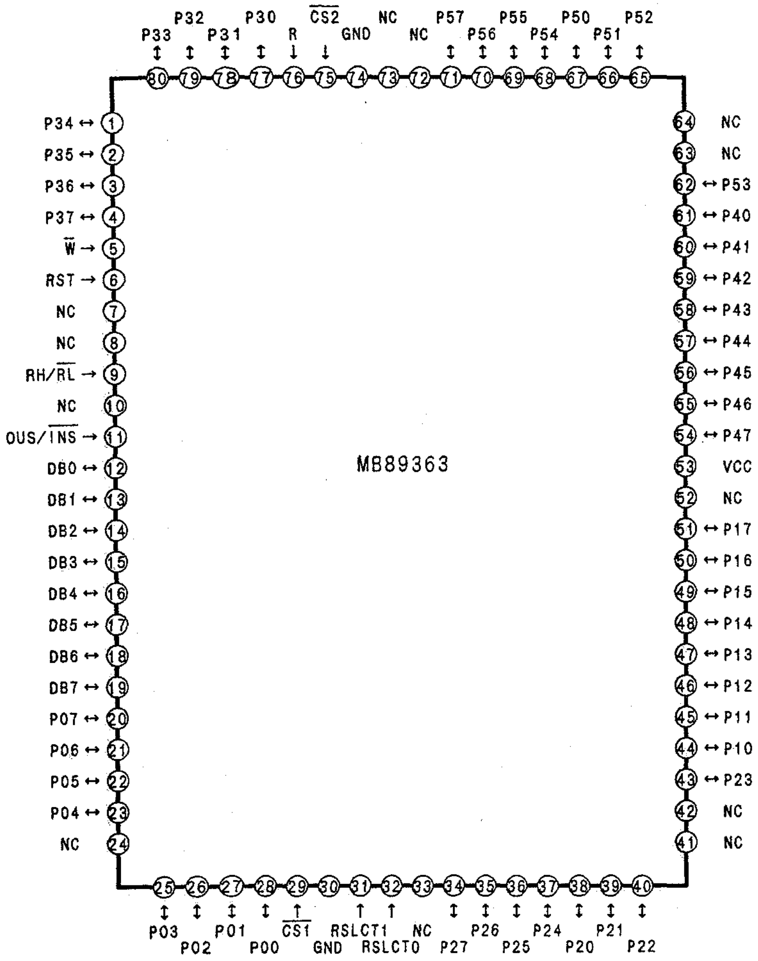

80 FRONT
79 D15
78 D14
77 D13
76 D12
75 D11
74 D10
73 VDD2
72 DO5
71 DO4
70 DO3
69 NC4
68 DO2
67 DO1
66 DO0
65 CASN
64 OEN
63 VSS6
62 PEN
61 RASN
1 TRST
2 VSS1
3 DCKA
4 DCKB
5 DCASA
6 DCASB
7 DOEA
8 DOEB
9 DRRA
10 DRRB
11 FS64
12 VS52
13 FS256
14 DRASA
15 DRASB
16 DNEA
17 NC1
18 DNEB
19 PASS
20 ASO
60 TEST3
59 TEST2
58 TEST1
57 NC3
56 AB12
55 AB11
54 AB10
53 AB9
52 VSS5
51 AB8
50 AB7
49 AB6
48 AB5
47 DRAN
46 AB4
45 AB3
44 AB2
43 AB1
42 VSS4
41 AB0
21 AS1
22 AS2
23 VSS3
24 AS3
25 AS4
26 AS5
27 AS6
28 AS7
29 AS8
30 AS9
31 AS10
32 AS11
33 VDD1
34 DB0
35 DB1
36 DB2
37 NC2
38 DB3
39 DB4
40 DB5
I/O
SRAM
ADRS GEN
TIMING GEN

MB81V4260S7
(4M BIT DRAM)


(TOP VIEW)
VCC 1
DQ1 2
DQ2 3
DQ3 4
DQ4 5
VCC 6
DQ5 7
DQ6 8
DQ7 9
DQ8 10
NC 13
NC 14
$\overline{WE}$ 15
$\overline{RAS}$ 16
NC 17
A0 18
A1 19
A2 20
A3 21
VCC 22
44 VSS
43 DQ16
42 DQ15
41 DQ14
40 DQ13
39 VSS
38 DQ12
37 DQ11
36 DQ10
35 DQ9
32 NC
31 $\overline{LCAS}$
30 $\overline{UCAS}$
29 $\overline{OE}$
28 A8
27 A7
26 A6
25 A5
24 A4
23 VSS

BLOCK DIAGRAM

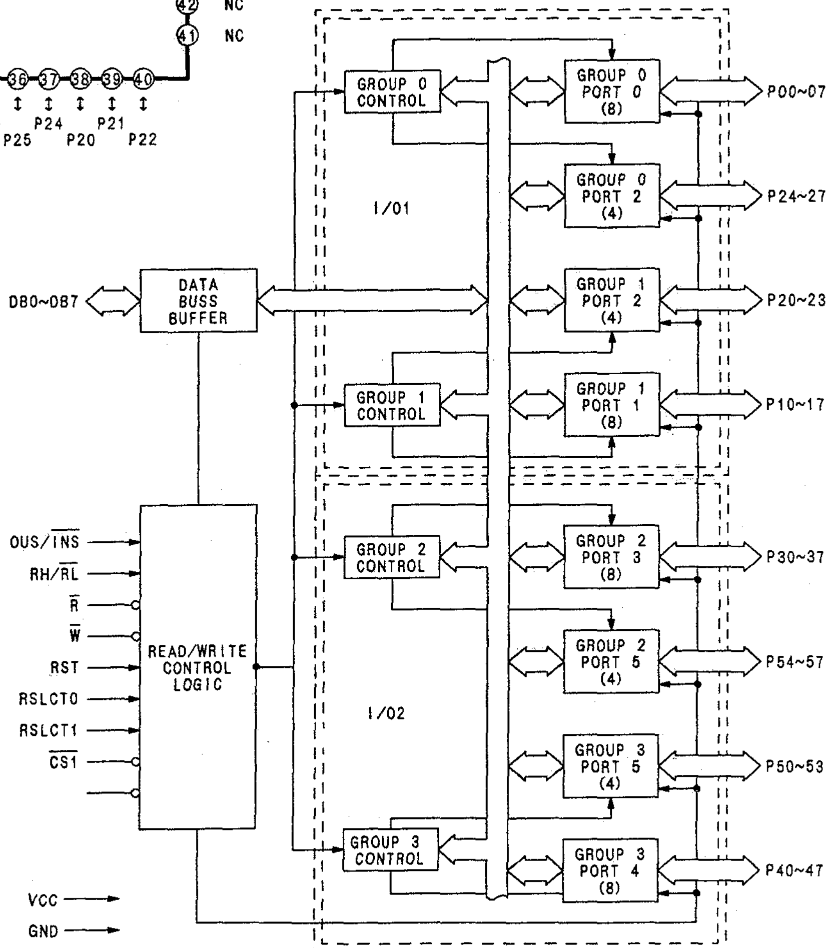

$\overline{RAS}$
$\overline{LCAS}$
$\overline{UCAS}$
CLOCK GEN. NO. 1
CLOCK GEN. NO. 2
MODE CONTROL
WRITE CLOCK GENE
$\overline{WE}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
ADDRESS BUFFER
PRE DECODER
COLUMN DECODER
SENSE UP I/O GATE
DATA INPUT BUFFER
DQ1~DQ16
LOW ENCODER
4,194,304 BIT MEMORY CELL
DATA OUTPUT BUFFER
REFRESH ADDRESS COUNTER
BIAS GENERATOR
$\overline{OE}$
VCC
VSS



P32
P30
CS2
NC
P57
P55
P50
P52
P33
P31
R
GND
NC
P56
P54
P51
80
79
78
77
76
75
74
73
72
71
70
69
68
67
66
65
P34 ↔ 1
P35 ↔ 2
P36 ↔ 3
P37 ↔ 4
W → 5
RST → 6
NC 7
NC 8
RH/RL → 9
NC 10
OUS/INS → 11
DB0 ↔ 12
DB1 ↔ 13
DB2 ↔ 14
DB3 ↔ 15
DB4 ↔ 16
DB5 ↔ 17
DB6 ↔ 18
DB7 ↔ 19
P07 ↔ 20
P06 ↔ 21
P05 ↔ 22
P04 ↔ 23
NC 24
MB89363
64 NC
63 NC
62 ↔ P53
61 ↔ P40
60 ↔ P41
59 ↔ P42
58 ↔ P43
57 ↔ P44
56 ↔ P45
55 ↔ P46
54 ↔ P47
53 VCC
52 NC
51 ↔ P17
50 ↔ P16
49 ↔ P15
48 ↔ P14
47 ↔ P13
46 ↔ P12
45 ↔ P11
44 ↔ P10
43 ↔ P23
42 NC
41 NC
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
P03
P02
P01
P00
CS1
GND
RSLCT1
RSLCT0
NC
P27
P26
P25
P24
P20
P21
P22

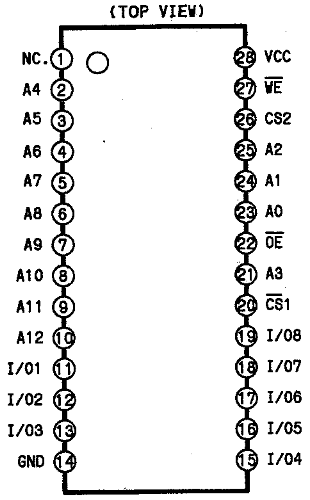
MB89363
(PROGRAMMABLE PERIPHERAL INTERFACE)
(TOP VIEW)

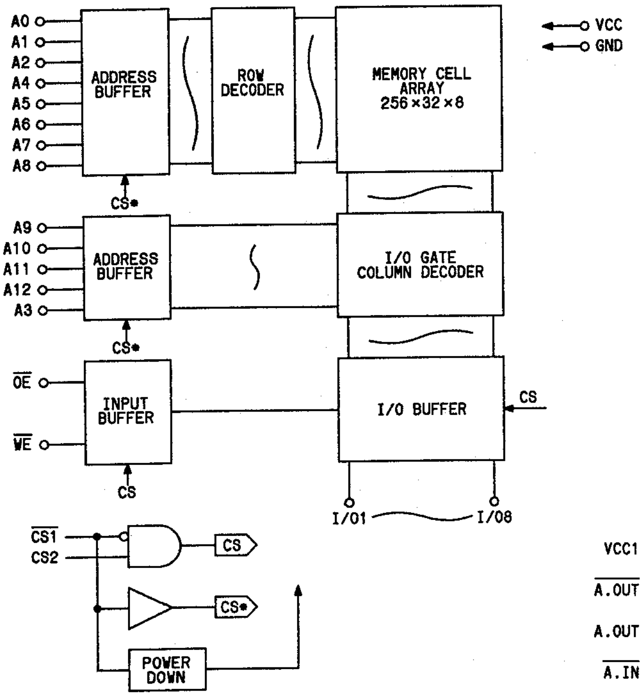
BLOCK DIAGRAM



GROUP 0 CONTROL
GROUP 0 PORT 0 (8)
P00~07
GROUP 0 PORT 2 (4)
P24~27
I/01
DB0~DB7
DATA BUSS BUFFER
GROUP 1 PORT 2 (4)
P20~23
GROUP 1 CONTROL
GROUP 1 PORT 1 (8)
P10~17
GROUP 2 CONTROL
GROUP 2 PORT 3 (8)
P30~37
OUS/INS
RH/RL
R
W
RST
RSLCT0
RSLCT1
CS1
READ/WRITE CONTROL LOGIC
GROUP 2 PORT 5 (4)
P54~57
I/02
GROUP 3 PORT 5 (4)
P50~53
GROUP 3 CONTROL
GROUP 3 PORT 4 (8)
P40~47
VCC
GND

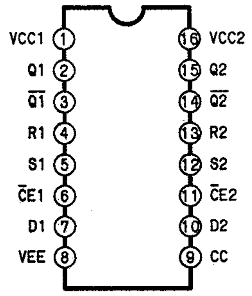
MB81C78A35PF (8K MEMORY)


(TOP VIEW)
NC. 1
A4 2
A5 3
A6 4
A7 5
A8 6
A9 7
A10 8
A11 9
A12 10
I/01 11
I/02 12
I/03 13
GND 14
28 VCC
27 $\overline{WE}$
26 CS2
25 A2
24 A1
23 A0
22 $\overline{OE}$
21 A3
20 $\overline{CS1}$
19 I/08
18 I/07
17 I/06
16 I/05
15 I/04


A0
A1
A2
A4
A5
A6
A7
A8
ADDRESS BUFFER
ROW DECODER
MEMORY CELL ARRAY 256×32×8
VCC
GND
CS*
A9
A10
A11
A12
A3
ADDRESS BUFFER
I/O GATE COLUMN DECODER
CS*
$\overline{OE}$
$\overline{WE}$
INPUT BUFFER
I/O BUFFER
CS
CS
I/01
I/08
$\overline{CS1}$
CS2
CS
CS*
POWER DOWN

MC10131

(DUAL TYPED MASTER-SLAVE FLIP-FLOP)


VCC1 1
Q1 2
$\overline{Q1}$ 3
R1 4
S1 5
$\overline{CE1}$ 6
D1 7
VEE 8
16 VCC2
15 Q2
14 $\overline{Q2}$
13 R2
12 S2
11 $\overline{CE2}$
10 D2
9 CC

CLOCKED TRUTH TABLE

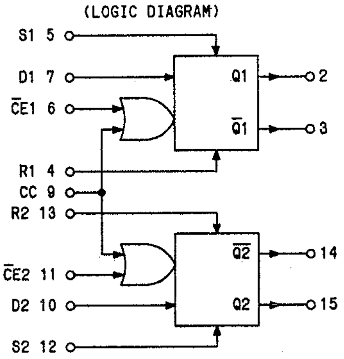
C	D	QN-1
L	ϕ	QN
H	L	L
H	H	H

ϕ-DON'T CARE
C -CE+CC
A CLOCK H IS A CLOCK TRANSITION FROM A LOW TO A HIGH STATE.

R-S TRUTH TABLE

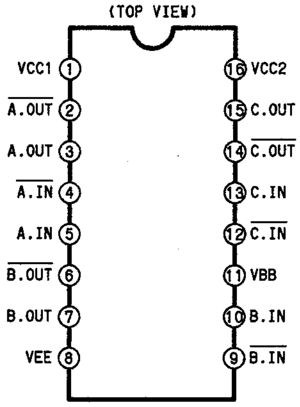
R	S	QN-1
L	L	QN
L	H	H
H	L	L
H	H	N.D.

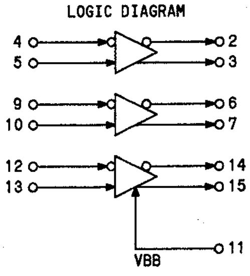
N.D.-NOT DEFINED


(LOGIC DIAGRAM)
S1 5
D1 7
$\overline{CE1}$ 6
R1 4
CC 9
R2 13
$\overline{CE2}$ 11
D2 10
S2 12
Q1
$\overline{Q1}$
2
3
$\overline{Q2}$
Q2
14
15

MC10H116

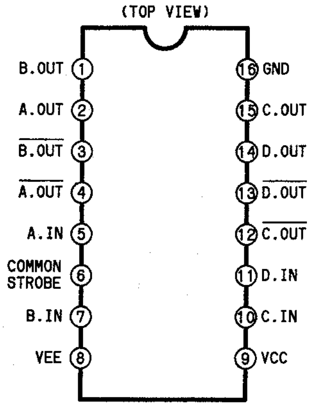
(TRIPLE LINE RECEIVER)

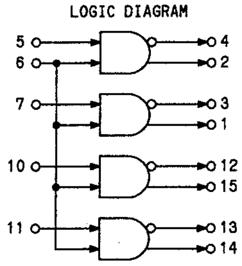

(TOP VIEW)
VCC1 1
$\overline{A.OUT}$ 2
A.OUT 3
$\overline{A.IN}$ 4
A.IN 5
$\overline{B.OUT}$ 6
B.OUT 7
VEE 8
16 VCC2
15 C.OUT
14 $\overline{C.OUT}$
13 C.IN
12 $\overline{C.IN}$
11 VBB
10 B.IN
9 $\overline{B.IN}$


LOGIC DIAGRAM
4
5
2
3
9
10
6
7
12
13
14
15
VBB
11

MC10124

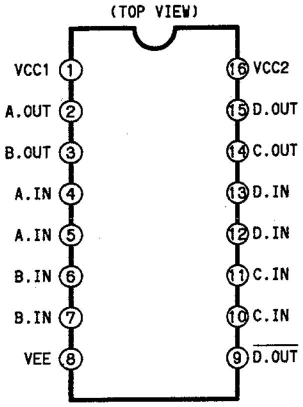
(QUAD TTL TO MECL TRANSLATOR)


(TOP VIEW)
B.OUT 1
A.OUT 2
$\overline{B.OUT}$ 3
$\overline{A.OUT}$ 4
A.IN 5
COMMON STROBE 6
B.IN 7
VEE 8
16 GND
15 C.OUT
14 D.OUT
13 $\overline{D.OUT}$
12 $\overline{C.OUT}$
11 D.IN
10 C.IN
9 VCC

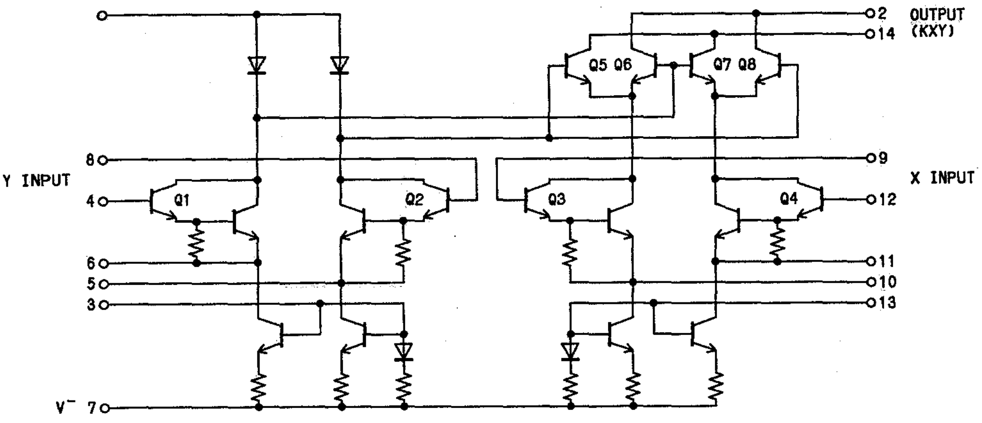

LOGIC DIAGRAM
5
6
4
2
7
3
1
10
12
15
11
13
14

MC10H102

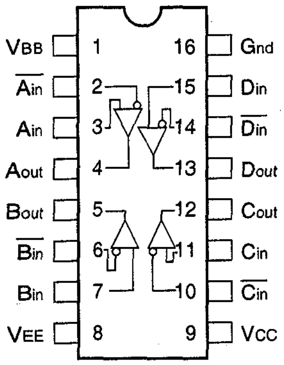
(QUAD 2-INPUT NOR GATE)


(TOP VIEW)
VCC1 1
A.OUT 2
B.OUT 3
A.IN 4
A.IN 5
B.IN 6
B.IN 7
VEE 8
16 VCC2
15 D.OUT
14 C.OUT
13 D.IN
12 D.IN
11 C.IN
10 C.IN
9 $\overline{D.OUT}$

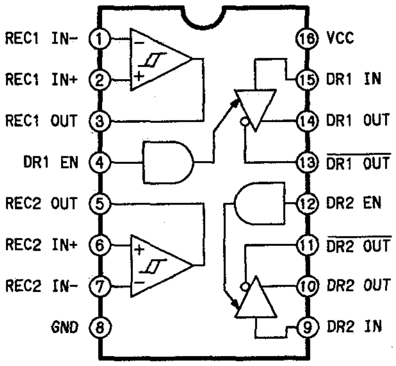
MC1495L
(ANALYSIS AND BASIC OPERATION)


2 OUTPUT
14 (KXY)
Q5 Q6
Q7 Q8
8
Y INPUT
4
Q1
Q2
Q3
Q4
9
X INPUT
12
6
5
3
11
10
13
V⁻ 7

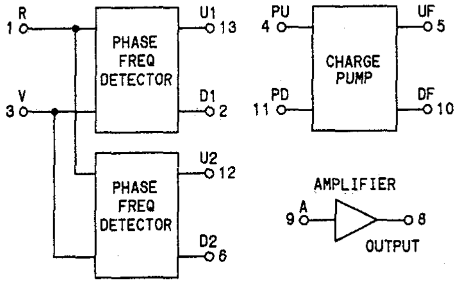
MC10H125(QUAD MECL-TO-TTL TRANSLATOR)


VBB 1
$\overline{\text{Ain}}$ 2
Ain 3
Aout 4
Bout 5
$\overline{\text{Bin}}$ 6
Bin 7
VEE 8
16 Gnd
15 Din
14 $\overline{\text{Din}}$
13 Dout
12 Cout
11 Cin
10 $\overline{\text{Cin}}$
9 Vcc

MC34051
(DUAL RS-422/423 TRANSCEIVER)


REC1 IN- 1
REC1 IN+ 2
REC1 OUT 3
DR1 EN 4
REC2 OUT 5
REC2 IN+ 6
REC2 IN- 7
GND 8
16 VCC
15 DR1 IN
14 DR1 OUT
13 $\overline{\text{DR1 OUT}}$
12 DR2 EN
11 $\overline{\text{DR2 OUT}}$
10 DR2 OUT
9 DR2 IN

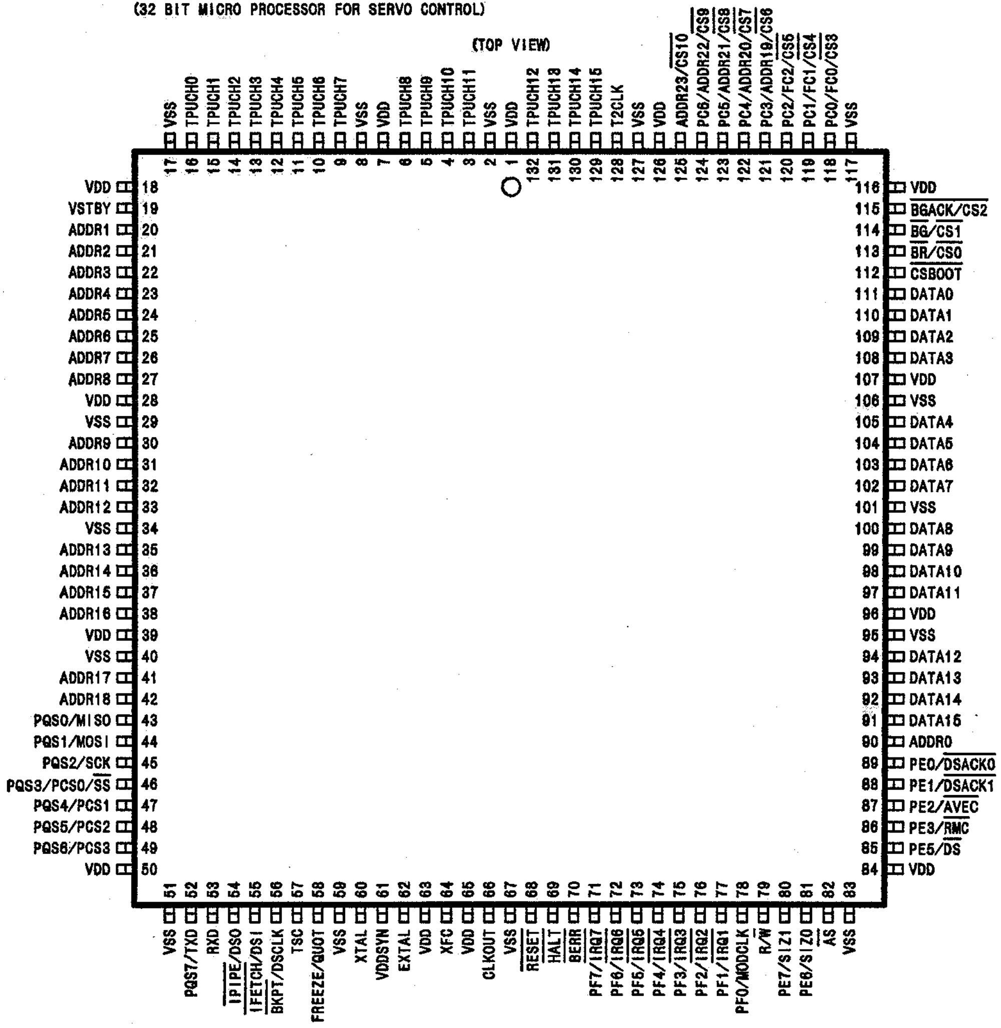
MC4044


R
1
V
3
PHASE FREQ DETECTOR
U1
13
D1
2
PHASE FREQ DETECTOR
U2
12
D2
6
PU
4
PD
11
CHARGE PUMP
UF
5
DF
10
AMPLIFIER
A
9
8
OUTPUT

TRUTH TABLE

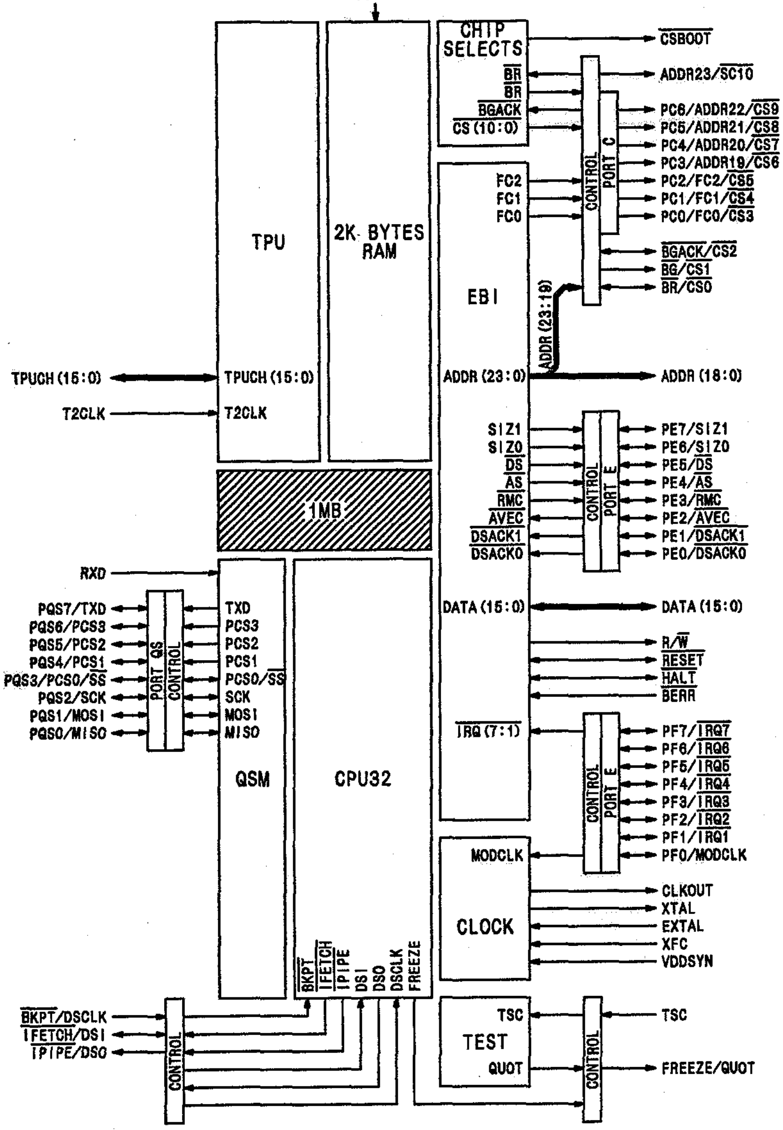
INPUT STATE	INPUT		OUTPUT			
	R	V	U1	D1	U2	D2
1	0	0	×	×	1	1
2	1	0	×	×	0	1
3	1	1	×	×	1	0
4	1	0	×	×	0	1
5	0	0	×	×	1	1
6	1	0	×	×	0	1
7	0	0	×	×	1	1
8	1	0	×	×	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

MC68332A
(32 BIT MICRO PROCESSOR FOR SERVO CONTROL)


(TOP VIEW)
17 VSS
16 TPUCH0
15 TPUCH1
14 TPUCH2
13 TPUCH3
12 TPUCH4
11 TPUCH5
10 TPUCH6
9 TPUCH7
8 VSS
7 VDD
6 TPUCH8
5 TPUCH9
4 TPUCH10
3 TPUCH11
2 VSS
1 VDD
132 TPUCH12
131 TPUCH13
130 TPUCH14
129 TPUCH15
128 T2CLK
127 VSS
126 VDD
125 ADDR23/CS10
124 PC6/ADDR22/CS9
123 PC5/ADDR21/CS8
122 PC4/ADDR20/CS7
121 PC3/ADDR19/CS6
120 PC2/FC2/CS5
119 PC1/FC1/CS4
118 PC0/FC0/CS3
117 VSS
VDD 18
VSTBY 19
ADDR1 20
ADDR2 21
ADDR3 22
ADDR4 23
ADDR5 24
ADDR6 25
ADDR7 26
ADDR8 27
VDD 28
VSS 29
ADDR9 30
ADDR10 31
ADDR11 32
ADDR12 33
VSS 34
ADDR13 35
ADDR14 36
ADDR15 37
ADDR16 38
VDD 39
VSS 40
ADDR17 41
ADDR18 42
PQS0/MISO 43
PQS1/MOSI 44
PQS2/SCK 45
PQS3/PCS0/SS 46
PQS4/PCS1 47
PQS5/PCS2 48
PQS6/PCS3 49
VDD 50
51 VSS
52 PQS7/TXD
53 RXD
54 IPIPE/DSO
55 IFETCH/DSI
56 BKPT/DSCLK
57 TSC
58 FREEZE/QUOT
59 VSS
60 XTAL
61 VDDSYN
62 EXTAL
63 VDD
64 XFC
65 VDD
66 CLKOUT
67 VSS
68 RESET
69 HALT
70 BERR
71 PF7/IRQ7
72 PF6/IRQ6
73 PF5/IRQ5
74 PF4/IRQ4
75 PF3/IRQ3
76 PF2/IRQ2
77 PF1/IRQ1
78 PF0/MODCLK
79 R/W
80 PE7/SIZ1
81 PE6/SIZ0
82 AS
83 VSS
116 VDD
115 BGACK/CS2
114 BG/CS1
113 BR/CS0
112 CSBOOT
111 DATA0
110 DATA1
109 DATA2
108 DATA3
107 VDD
106 VSS
105 DATA4
104 DATA5
103 DATA6
102 DATA7
101 VSS
100 DATA8
99 DATA9
98 DATA10
97 DATA11
96 VDD
95 VSS
94 DATA12
93 DATA13
92 DATA14
91 DATA15
90 ADDR0
89 PE0/DSACK0
88 PE1/DSACK1
87 PE2/AVEC
86 PE3/RMC
85 PE5/DS
84 VDD

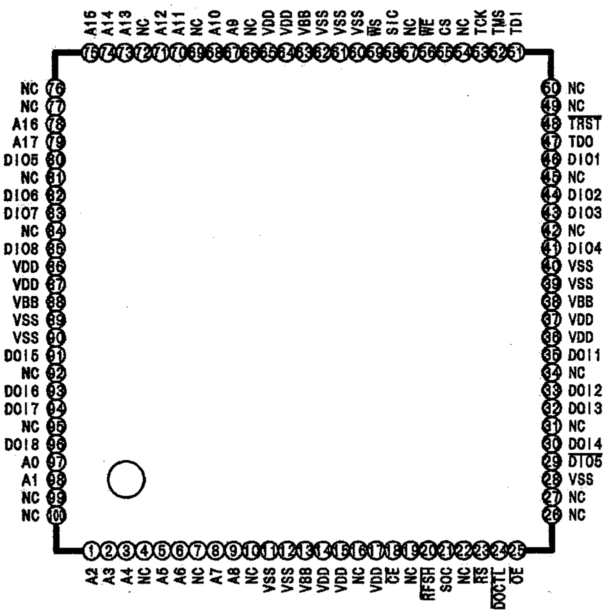
BLOCK DIAGRAM

MC68332A

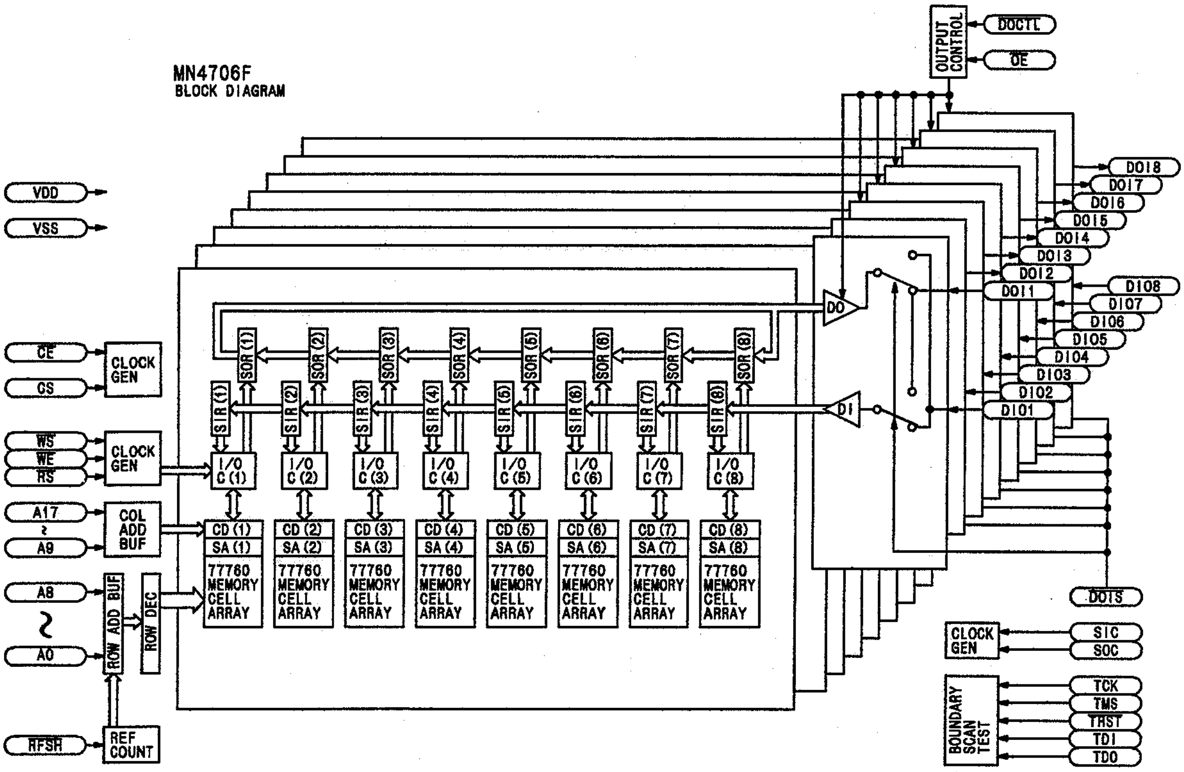

VSTBY
TPU
2K BYTES RAM
CHIP SELECTS
BR
BR
BGACK
CS (10:0)
CSBOOT
ADDR23/CS10
CONTROL
PORT C
PC6/ADDR22/CS9
PC5/ADDR21/CS8
PC4/ADDR20/CS7
PC3/ADDR19/CS6
PC2/FC2/CS5
PC1/FC1/CS4
PC0/FC0/CS3
BGACK/CS2
BG/CS1
BR/CS0
FC2
FC1
FC0
EBI
ADDR (23:19)
ADDR (23:0)
ADDR (18:0)
TPUCH (15:0)
TPUCH (15:0)
T2CLK
T2CLK
SIZ1
SIZ0
DS
AS
RMC
AVEC
DSACK1
DSACK0
CONTROL
PORT E
PE7/SIZ1
PE6/SIZ0
PE5/DS
PE4/AS
PE3/RMC
PE2/AVEC
PE1/DSACK1
PE0/DSACK0
1MB
RXD
PQS7/TXD
PQS6/PCS3
PQS5/PCS2
PQS4/PCS1
PQS3/PCS0/SS
PQS2/SCK
PQS1/MOSI
PQS0/MISO
PORT QS
CONTROL
TXD
PCS3
PCS2
PCS1
PCS0/SS
SCK
MOSI
MISO
QSM
CPU32
DATA (15:0)
DATA (15:0)
R/W
RESET
HALT
BERR
IRQ (7:1)
CONTROL
PORT F
PF7/IRQ7
PF6/IRQ6
PF5/IRQ5
PF4/IRQ4
PF3/IRQ3
PF2/IRQ2
PF1/IRQ1
PF0/MODCLK
MODCLK
CLOCK
CLKOUT
XTAL
EXTAL
XFC
VDDSYN
BKPT
IFETCH
IPIPE
DSI
DSO
DSCLK
FREEZE
BKPT/DSCLK
IFETCH/DSI
IPIPE/DSO
CONTROL
TEST
TSC
QUOT
CONTROL
TSC
FREEZE/QUOT

MN4706F
(4.75M BITS VIDEO MEMORY)

(TOP VIEW)


A15 75
A14 74
A13 73
NC 72
A12 71
A11 70
NC 69
A10 68
A9 67
NC 66
VDD 65
VDD 64
VBB 63
VSS 62
VSS 61
VSS 60
WS 59
SIC 58
NC 57
WE 56
CS 55
NC 54
TCK 53
TMS 52
TDI 51
NC 76
NC 77
A16 78
A17 79
DIO5 80
NC 81
DIO6 82
DIO7 83
NC 84
DIO8 85
VDD 86
VDD 87
VBB 88
VSS 89
VSS 90
DOI5 91
NC 92
DOI6 93
DOI7 94
NC 95
DOI8 96
A0 97
A1 98
NC 99
NC 100
60 NC
49 NC
48 TRST
47 TDO
46 DIO1
45 NC
44 DIO2
43 DIO3
42 NC
41 DIO4
40 VSS
39 VSS
38 VBB
37 VDD
36 VDD
35 DOI1
34 NC
33 DOI2
32 DOI3
31 NC
30 DOI4
29 DTO5
28 VSS
27 NC
26 NC
1 A2
2 A3
3 A4
4 NC
5 A5
6 A6
7 NC
8 A7
9 A8
10 NC
11 VSS
12 VSS
13 VBB
14 VDD
15 VDD
16 NC
17 VDD
18 CE
19 NC
20 RFSH
21 SOC
22 NC
23 RS
24 DOCTL
25 OE

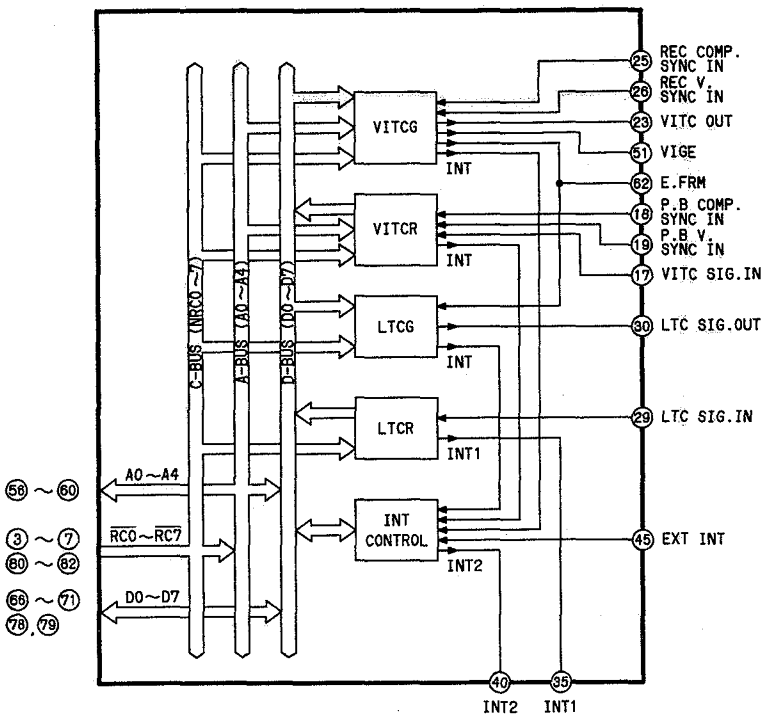
MN4706F
BLOCK DIAGRAM


VDD
VSS
CE
CS
CLOCK GEN
WS
WE
RS
CLOCK GEN
A17
A9
COL ADD BUF
A8
A0
ROW ADD BUF
ROW DEC
RFSH
REF COUNT
SOR (1)
SOR (2)
SOR (3)
SOR (4)
SOR (5)
SOR (6)
SOR (7)
SOR (8)
SIR (1)
SIR (2)
SIR (3)
SIR (4)
SIR (5)
SIR (6)
SIR (7)
SIR (8)
I/O C (1)
I/O C (2)
I/O C (3)
I/O C (4)
I/O C (5)
I/O C (6)
I/O C (7)
I/O C (8)
CD (1)
SA (1)
CD (2)
SA (2)
CD (3)
SA (3)
CD (4)
SA (4)
CD (5)
SA (5)
CD (6)
SA (6)
CD (7)
SA (7)
CD (8)
SA (8)
77760 MEMORY CELL ARRAY
DO
DI
OUTPUT CONTROL
DOCTL
OE
DOI8
DOI7
DOI6
DOI5
DOI4
DOI3
DOI2
DOI1
DIO8
DIO7
DIO6
DIO5
DIO4
DIO3
DIO2
DIO1
DOTS
CLOCK GEN
SIC
SOC
BOUNDARY SCAN TEST
TCK
TMS
TRST
TDI
TDO

SIR :SHIFT IN REGISTER
SOR :SHIFT OUT REGISTER
I/O C:I/O CONTROLLER
CD :COLUMN DECODER
SA :SENSE AMPLIFIER
DI :DATA IN BUFFER
DO :DATA OUT BUFFER

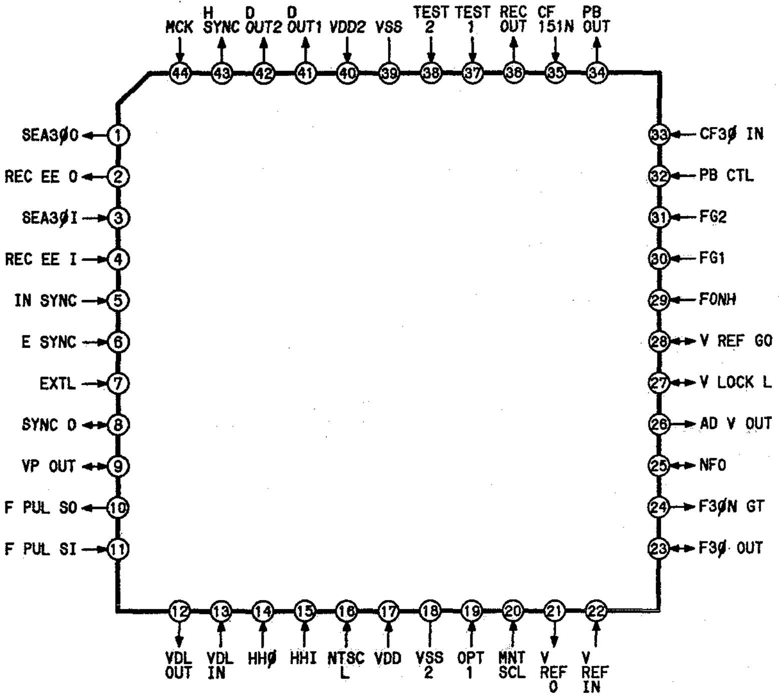
CLOCK GEN :CLOCK GENERATOR
COL ADD BUF:COLUMN ADDRESS BUFFER
ROW ADD BUF:ROW ADDRESS BUFFER
ROW DEC :ROW DECODER
REF COUNT :REFRESH COUNTER

MN51040
(TIME CODE GENERATOR/READER)



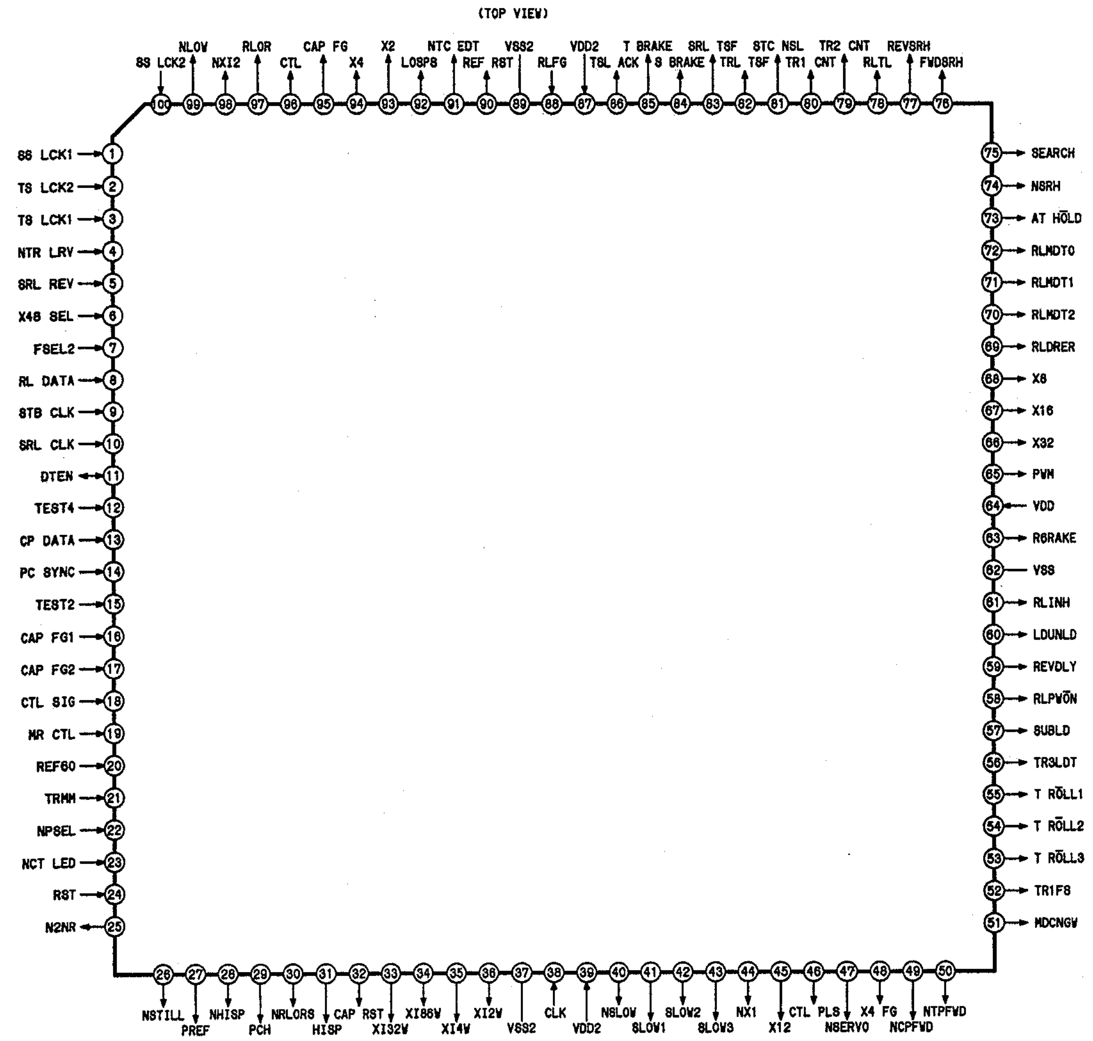
VITCG
INT
VITCR
INT
LTCG
INT
LTCR
INT1
INT CONTROL
INT2
C-BUS (NRC0~7)
A-BUS (A0~A4)
D-BUS (D0~D7)
㉕ REC COMP. SYNC IN
㉖ REC V. SYNC IN
㉓ VITC OUT
(51) VIGE
(62) E.FRM
⑱ P.B COMP. SYNC IN
⑲ P.B V. SYNC IN
⑰ VITC SIG.IN
㉚ LTC SIG.OUT
㉙ LTC SIG.IN
㊺ EXT INT
(56) ~ (60)
A0~A4
③ ~ ⑦
(80) ~ (82)
RC0~RC7
(66) ~ (71)
(78), (79)
D0~D7
㊵ INT2
㉟ INT1

MN53015VZW
(1500 GATES C-MOS GATE ARRAY)

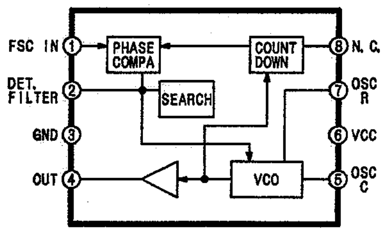


MCK ㊹
H SYNC ㊸
D OUT2 ㊷
D OUT1 ㊶
VDD2 ㊵
VSS ㊴
TEST 2 ㊳
TEST 1 ㊲
REC OUT ㊱
CF 151N ㉟
PB OUT ㉞
SEA30O ①
REC EE O ②
SEA30I ③
REC EE I ④
IN SYNC ⑤
E SYNC ⑥
EXTL ⑦
SYNC O ⑧
VP OUT ⑨
F PUL SO ⑩
F PUL SI ⑪
㉝ CF30 IN
㉜ PB CTL
㉛ FG2
㉚ FG1
㉙ FONH
㉘ V REF GO
㉗ V LOCK L
㉖ AD V OUT
㉕ NFO
㉔ F30N GT
㉓ F30 OUT
⑫ VDL OUT
⑬ VDL IN
⑭ HH0
⑮ HHI
⑯ NTSC L
⑰ VDD
⑱ VSS 2
⑲ OPT 1
⑳ MNT SCL
㉑ V REF O
㉒ V REF IN

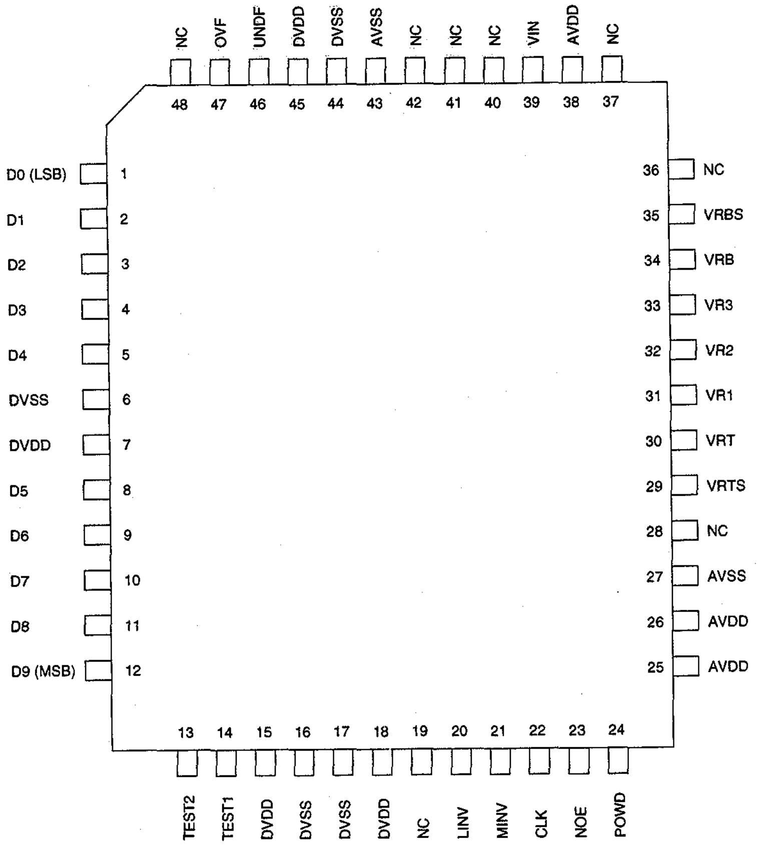
MN53030VYA (CONTROL FOR JOG)


(TOP VIEW)
1 SS LCK1
2 TS LCK2
3 TS LCK1
4 NTR LRV
5 SRL REV
6 X48 SEL
7 FSEL2
8 RL DATA
9 STB CLK
10 SRL CLK
11 DTEN
12 TEST4
13 CP DATA
14 PC SYNC
15 TEST2
16 CAP FG1
17 CAP FG2
18 CTL SIG
19 MR CTL
20 REF60
21 TRMM
22 NPSEL
23 NCT LED
24 RST
25 N2NR
26 NSTILL
27 PREF
28 NHISP
29 PCH
30 NRLORS
31 HISP
32 CAP RST
33 XI32W
34 XI86W
35 XI4W
36 XI2W
37 VSS2
38 CLK
39 VDD2
40 NSLOW
41 SLOW1
42 SLOW2
43 SLOW3
44 NX1
45 X12
46 CTL PLS
47 NSERVO
48 X4 FG
49 NCPFWD
50 NTPFWD
51 MDCNGW
52 TR1FS
53 T ROLL3
54 T ROLL2
55 T ROLL1
56 TRSLDT
57 SUBLD
58 RLPWON
59 REVDLY
60 LDUNLD
61 RLINH
62 VSS
63 RBRAKE
64 VDD
65 PWM
66 X32
67 X16
68 X8
69 RLDRER
70 RLMDT2
71 RLMDT1
72 RLMDT0
73 AT HOLD
74 NSRH
75 SEARCH
76 FWDSRH
77 REVSRH
78 RLTL
79 TR2 CNT
80 TR1 CNT
81 STC NSL
82 TRL TSF
83 SRL TSF
84 S BRAKE
85 T BRAKE
86 TSL ACK
87 VDD2
88 RLFG
89 VSS2
90 REF RST
91 NTC EDT
92 LOSPS
93 X2
94 X4
95 CAP FG
96 CTL
97 RLOR
98 NXI2
99 NLOW
100 SS LCK2

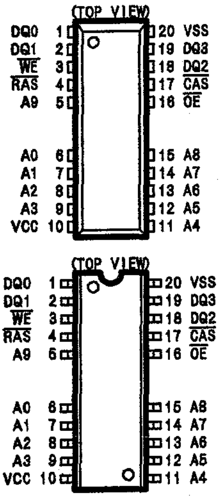
MST003MS
(NTSC/PAL 4FSC·MULTIPLEXER)


FSC IN 1
DET. FILTER 2
GND 3
OUT 4
5 OSC C
6 VCC
7 OSC R
8 N. C.
PHASE COMPA
COUNT DOWN
SEARCH
VCO

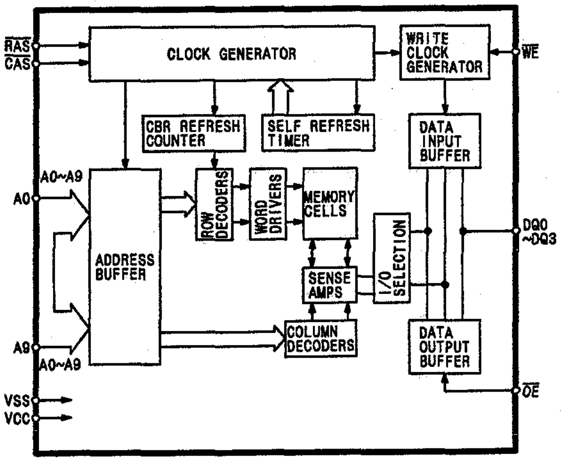
MN6577H


48 NC
47 OVF
46 UNDF
45 DVDD
44 DVSS
43 AVSS
42 NC
41 NC
40 NC
39 VIN
38 AVDD
37 NC
1 D0 (LSB)
2 D1
3 D2
4 D3
5 D4
6 DVSS
7 DVDD
8 D5
9 D6
10 D7
11 D8
12 D9 (MSB)
36 NC
35 VRBS
34 VRB
33 VR3
32 VR2
31 VR1
30 VRT
29 VRTS
28 NC
27 AVSS
26 AVDD
25 AVDD
13 TEST2
14 TEST1
15 DVDD
16 DVSS
17 DVSS
18 DVDD
19 NC
20 LINV
21 MINV
22 CLK
23 NOE
24 POWD

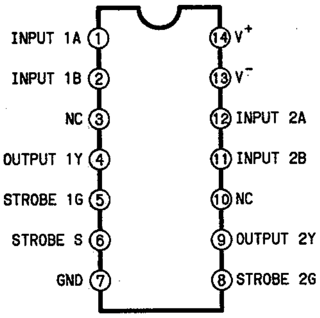
MNS4400CJ7

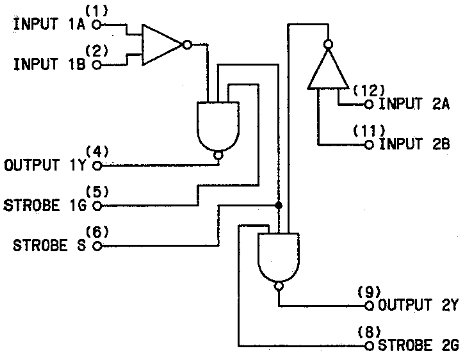

(TOP VIEW)
DQ0 1
DQ1 2
WE 3
RAS 4
A9 5
A0 6
A1 7
A2 8
A3 9
VCC 10
20 VSS
19 DQ3
18 DQ2
17 CAS
16 OE
15 A8
14 A7
13 A6
12 A5
11 A4
(TOP VIEW)
DQ0 1
DQ1 2
WE 3
RAS 4
A9 5
A0 6
A1 7
A2 8
A3 9
VCC 10
20 VSS
19 DQ3
18 DQ2
17 CAS
16 OE
15 A8
14 A7
13 A6
12 A5
11 A4

BLOCK DIAGRAM

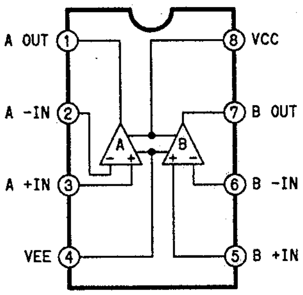

RAS
CAS
CLOCK GENERATOR
WRITE CLOCK GENERATOR
WE
CBR REFRESH COUNTER
SELF REFRESH TIMER
DATA INPUT BUFFER
A0~A9
A0
ADDRESS BUFFER
ROW DECODERS
WORD DRIVERS
MEMORY CELLS
I/O SELECTION
DQ0 ~DQ3
SENSE AMPS
COLUMN DECODERS
DATA OUTPUT BUFFER
A9
A0~A9
OE
VSS
VCC

NE521
(HIGH SPEED DUAL DIFFERENTIAL COMPARATOR)


INPUT 1A ①
INPUT 1B ②
NC ③
OUTPUT 1Y ④
STROBE 1G ⑤
STROBE S ⑥
GND ⑦
⑭ V+
⑬ V-
⑫ INPUT 2A
⑪ INPUT 2B
⑩ NC
⑨ OUTPUT 2Y
⑧ STROBE 2G

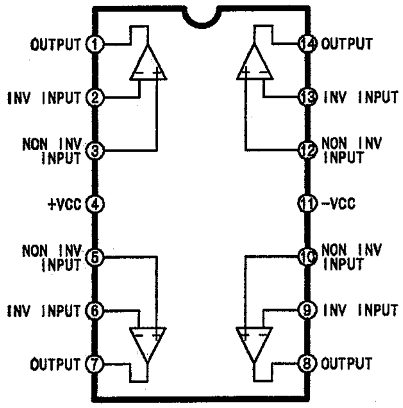

(1) INPUT 1A
(2) INPUT 1B
(4) OUTPUT 1Y
(5) STROBE 1G
(6) STROBE S
(12) INPUT 2A
(11) INPUT 2B
(9) OUTPUT 2Y
(8) STROBE 2G

NJM062M
(OPERATIONAL AMPLIFIER)
(TOP VIEW)

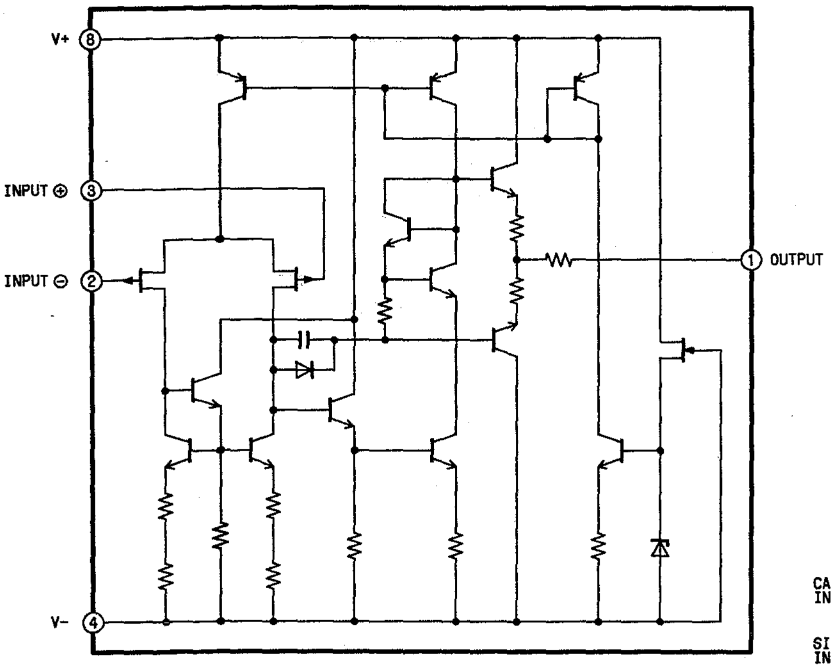

A OUT ①
A -IN ②
A +IN ③
VEE ④
⑧ VCC
⑦ B OUT
⑥ B -IN
⑤ B +IN
A
B
-
+

NJM064
(OP AMP, LOW POWER, JFET INPUT)

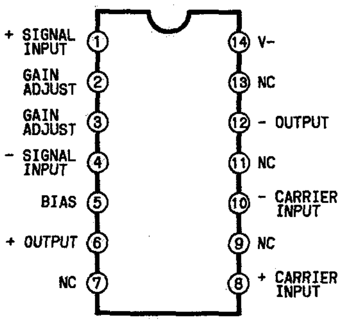
(TOP VIEW)

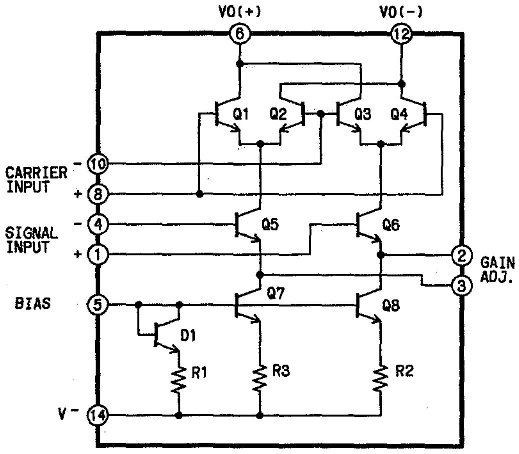

OUTPUT ①
INV INPUT ②
NON INV INPUT ③
+VCC ④
NON INV INPUT ⑤
INV INPUT ⑥
OUTPUT ⑦
⑭ OUTPUT
⑬ INV INPUT
⑫ NON INV INPUT
⑪ -VCC
⑩ NON INV INPUT
⑨ INV INPUT
⑧ OUTPUT

NJM082BM
(OPERATIONAL AMPLIFIER)

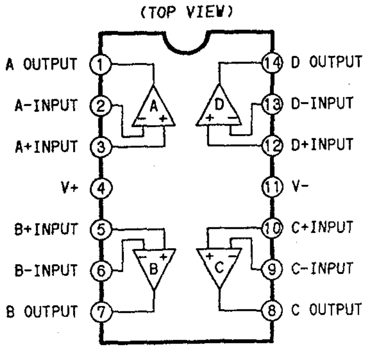

V+ ⑧
INPUT ⊕ ③
INPUT ⊖ ②
V- ④
① OUTPUT

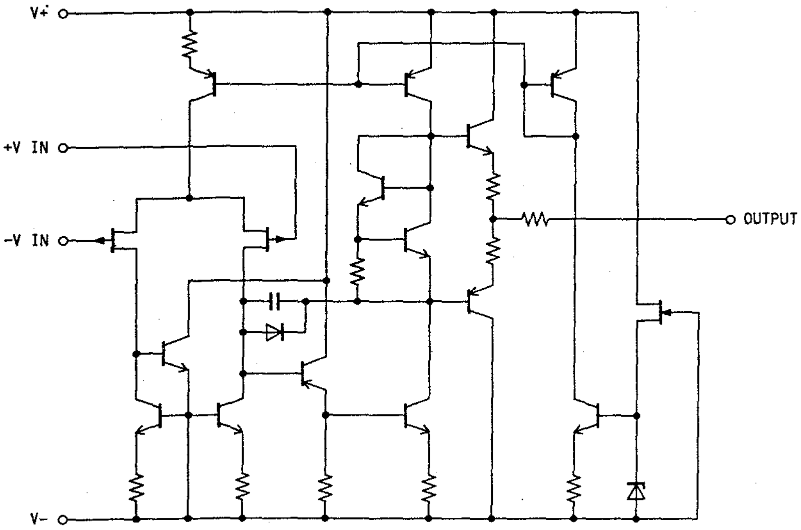
NJM1496
(BALANCED MODULATOR/DEMODULATOR)


+ SIGNAL INPUT ①
GAIN ADJUST ②
GAIN ADJUST ③
- SIGNAL INPUT ④
BIAS ⑤
+ OUTPUT ⑥
NC ⑦
⑭ V-
⑬ NC
⑫ - OUTPUT
⑪ NC
⑩ - CARRIER INPUT
⑨ NC
⑧ + CARRIER INPUT

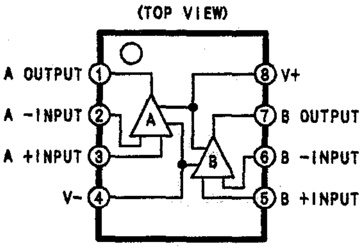

VO(+)
VO(-)
⑥
⑫
Q1
Q2
Q3
Q4
CARRIER INPUT
- ⑩
+ ⑧
SIGNAL INPUT
- ④
+ ①
Q5
Q6
② GAIN ADJ.
③
BIAS ⑤
Q7
Q8
D1
R1
R3
R2
V- ⑭

NJM084
(QUAD J-FET INPUT OPERATINAL AMPLIFIER)


(TOP VIEW)
A OUTPUT ①
A-INPUT ②
A+INPUT ③
V+ ④
B+INPUT ⑤
B-INPUT ⑥
B OUTPUT ⑦
⑭ D OUTPUT
⑬ D-INPUT
⑫ D+INPUT
⑪ V-
⑩ C+INPUT
⑨ C-INPUT
⑧ C OUTPUT
A
B
C
D


V+
+V IN
-V IN
V-
OUTPUT

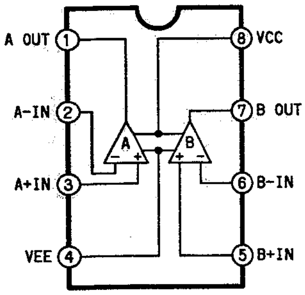
NJM2043MD
(OP AMP)

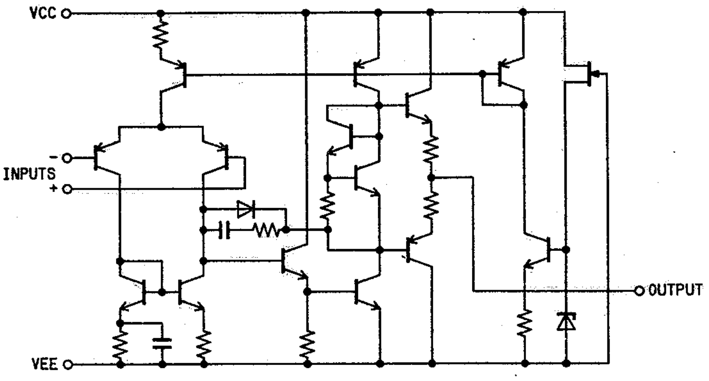

(TOP VIEW)
A OUTPUT ①
A -INPUT ②
A +INPUT ③
V- ④
⑧ V+
⑦ B OUTPUT
⑥ B -INPUT
⑤ B +INPUT
A
B

NJM2068MD

(OPERATIONAL AMPLIFIER)

(TOP VIEW)

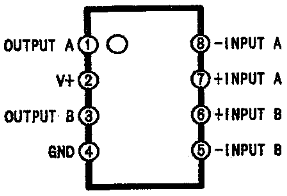

A OUT ①
A-IN ②
A+IN ③
VEE ④
⑧ VCC
⑦ B OUT
⑥ B-IN
⑤ B+IN
A
B
+
-


VCC
INPUTS
-
+
OUTPUT
VEE

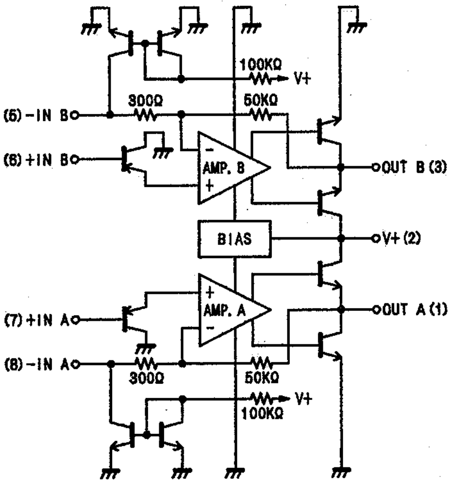
NJM2073M

(DUAL LOW POWER OPERATION POWER AMP)

(TOP VIEW)


OUTPUT A ①
V+ ②
OUTPUT B ③
GND ④
⑧ -INPUT A
⑦ +INPUT A
⑥ +INPUT B
⑤ -INPUT B

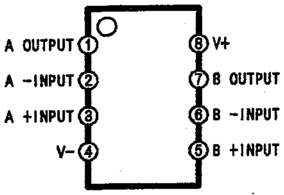
BLOCK DIAGRAM


100KΩ
V+
300Ω
50KΩ
(5) -IN B
(6) +IN B
AMP. B
OUT B (3)
BIAS
V+ (2)
(7) +IN A
AMP. A
OUT A (1)
(8) -IN A
300Ω
50KΩ
V+
100KΩ

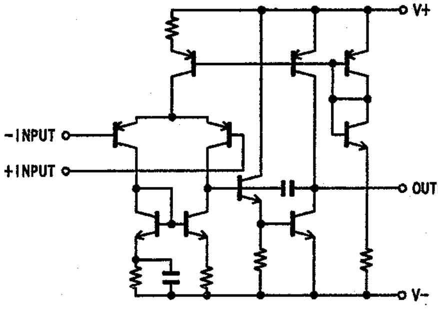
NJM2100MD

(OP AMP)

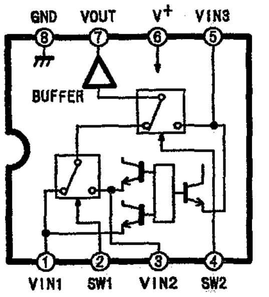
(TOP VIEW)


A OUTPUT ①
A -INPUT ②
A +INPUT ③
V- ④
⑧ V+
⑦ B OUTPUT
⑥ B -INPUT
⑤ B +INPUT

EQUIVALENT CIRCUIT

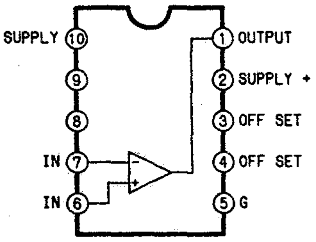

V+
-INPUT
+INPUT
OUTPUT
V-

NJM2535M
(3 INPUTS SINGLE VIDEO SWITCH)


GND
VOUT
V+
VIN3
8
7
6
5
BUFFER
1
2
3
4
VIN1
SW1
VIN2
SW2

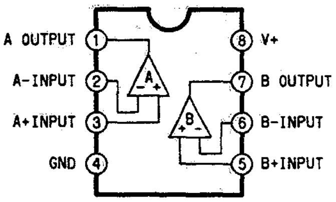
NJM2903M

(VOLTAGE CONPARATOR)
(TOP VIEW)

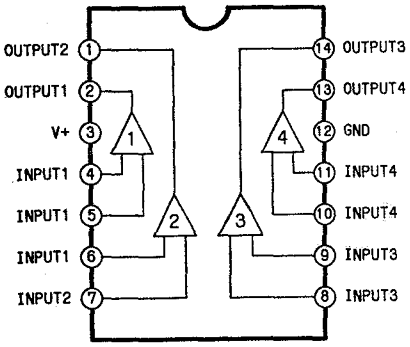

SUPPLY 10
9
8
IN 7
IN 6
1 OUTPUT
2 SUPPLY +
3 OFF SET
4 OFF SET
5 G
-
+

NJM2904M

(DUAL SIGNAL SUPPLY OPERATIONAL AMPLIFIER)
(TOP VIEW)

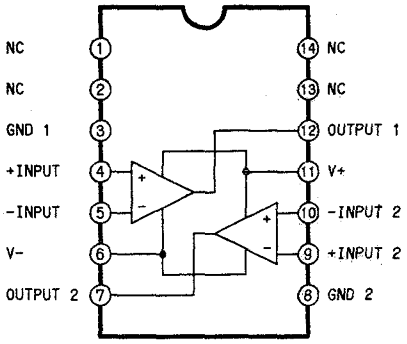

A OUTPUT 1
A-INPUT 2
A+INPUT 3
GND 4
8 V+
7 B OUTPUT
6 B-INPUT
5 B+INPUT
A
B
-
+

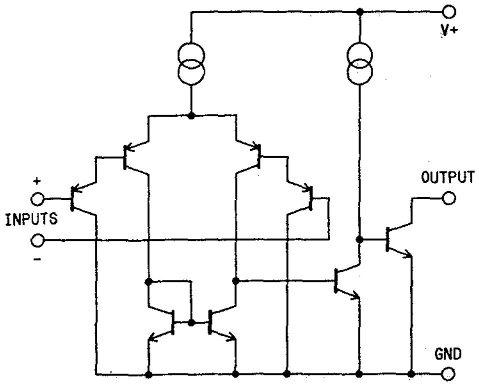
NJM2901
(QUAD VOLTAGE COMPARATOR)
(TOP VIEW)

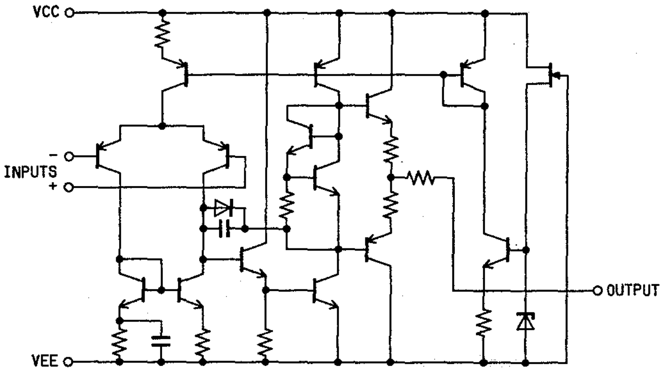

OUTPUT2 1
OUTPUT1 2
V+ 3
INPUT1 4
INPUT1 5
INPUT1 6
INPUT2 7
14 OUTPUT3
13 OUTPUT4
12 GND
11 INPUT4
10 INPUT4
9 INPUT3
8 INPUT3
1
2
3
4

NJM319M

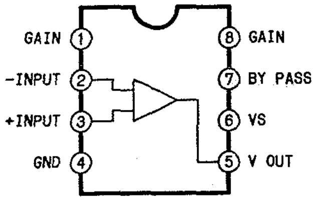
(DUAL VOLTAGE COMPARATOR)
(TOP VIEW)


NC 1
NC 2
GND 1 3
+INPUT 4
-INPUT 5
V- 6
OUTPUT 2 7
14 NC
13 NC
12 OUTPUT 1
11 V+
10 -INPUT 2
9 +INPUT 2
8 GND 2
+
-

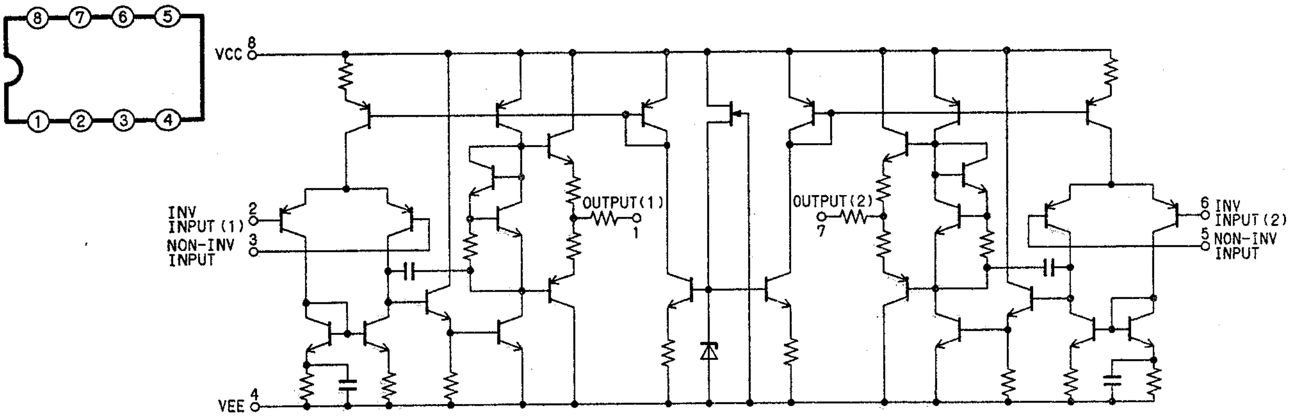

V+
+
INPUTS
-
OUTPUT
GND


VCC
-
INPUTS
+
OUTPUT
VEE

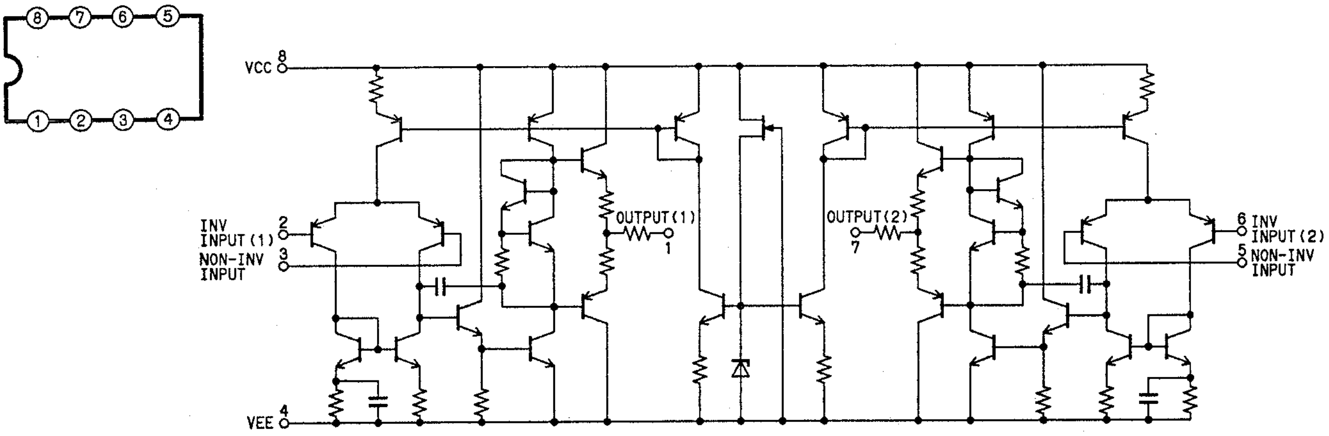
NJM386
(LOW FREQUENCY POWER AMPLIFIER)
(TOP VIEW)


GAIN 1
-INPUT 2
+INPUT 3
GND 4
8 GAIN
7 BY PASS
6 VS
5 V OUT

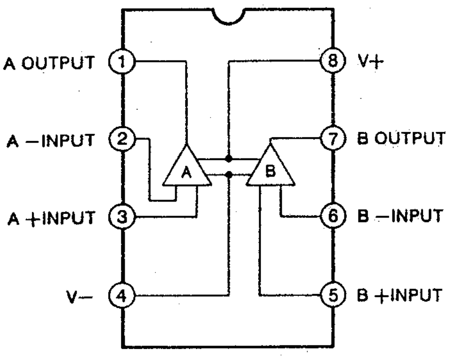
NJM4556MB
(OPERATIONAL AMPLIFIER)


8
7
6
5
1
2
3
4
VCC 8
INV INPUT (1) 2
NON-INV INPUT 3
OUTPUT(1)
1
OUTPUT(2)
7
6 INV INPUT (2)
5 NON-INV INPUT
VEE 4

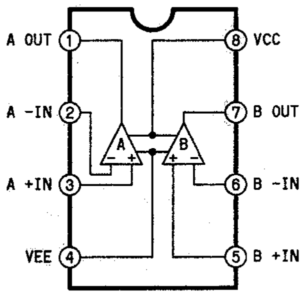
NJM4560
(OPERATIONAL AMPLIFIER)


8
7
6
5
1
2
3
4
VCC 8
INV INPUT (1) 2
NON-INV INPUT 3
OUTPUT(1)
1
OUTPUT(2)
7
6 INV INPUT (2)
5 NON-INV INPUT
VEE 4

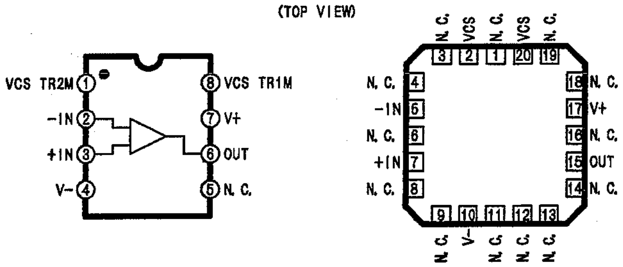
NJM4580ED
(DUAL OP AMP)


A OUTPUT 1
A −INPUT 2
A +INPUT 3
V− 4
8 V+
7 B OUTPUT
6 B −INPUT
5 B +INPUT
A
B

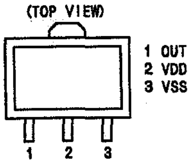
NJM4558
(OPERATIONAL AMPLIFIER)
(TOP VIEW)


A OUT 1
A -IN 2
A +IN 3
VEE 4
8 VCC
7 B OUT
6 B -IN
5 B +IN
A
B

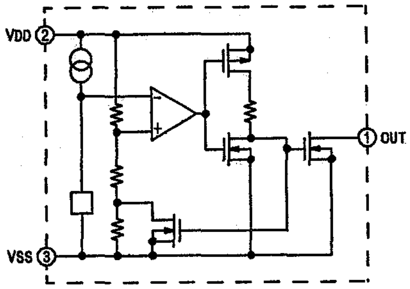
OP177GS
(OP AMP)


(TOP VIEW)
VCS TR2M 1
-IN 2
+IN 3
V- 4
8 VCS TR1M
7 V+
6 OUT
5 N. C.
3 N. C.
2 VCS
1 N. C.
20 VCS
19 N. C.
4 N. C.
5 -IN
6 N. C.
7 +IN
8 N. C.
18 N. C.
17 V+
16 N. C.
15 OUT
14 N. C.
9 N. C.
10 V-
11 N. C.
12 N. C.
13 N. C.

S80700AN


(TOP VIEW)
1 OUT
2 VDD
3 VSS
1
2
3

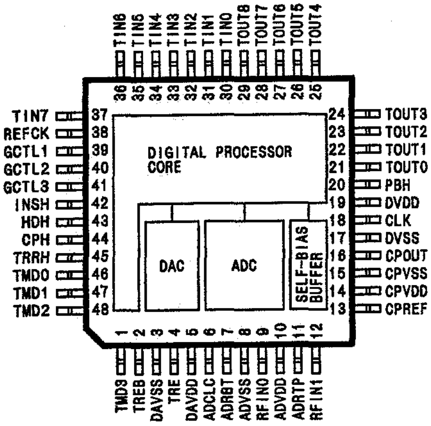
BLOCK DIAGRAM


VDD ②
VSS ③
① OUT

SC371025VFU

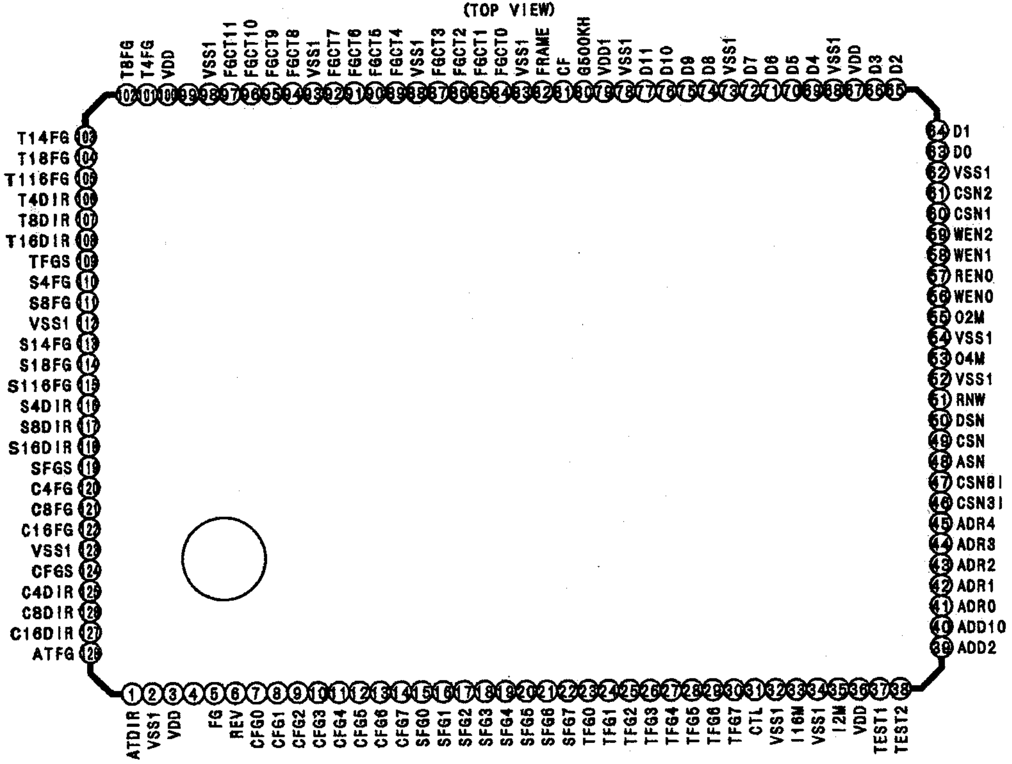
(FULL DIGITAL VTR SERVO INTERFACE)

(TOP VIEW)

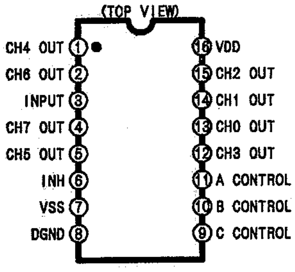

TIN6 36
TIN5 35
TIN4 34
TIN3 33
TIN2 32
TIN1 31
TIN0 30
TOUT8 29
TOUT7 28
TOUT6 27
TOUT5 26
TOUT4 25
TIN7 37
REFCK 38
GCTL1 39
GCTL2 40
GCTL3 41
INSH 42
HDH 43
CPH 44
TRRH 45
TMD0 46
TMD1 47
TMD2 48
24 TOUT3
23 TOUT2
22 TOUT1
21 TOUT0
20 PBH
19 DVDD
18 CLK
17 DVSS
16 CPOUT
15 CPVSS
14 CPVDD
13 CPREF
1 TMD3
2 TREB
3 DAVSS
4 TRE
5 DAVDD
6 ADCLC
7 ADRBT
8 ADVSS
9 RFIN0
10 ADVDD
11 ADRTP
12 RFIN1
DIGITAL PROCESSOR CORE
DAC
ADC
SELF-BIAS BUFFER

(1) TMD3 :TEST MODE SELECT INPUT
(2) TREB :DA CONV. BUFFER OUTPUT
(4) TRE :DA CONV. OUTPUT
(7) ADRBT :AD CONV. BOTTOM REFERENCE
(9) RFIN0 :AD CONV. INPUT
(11) ADRTP :AD CONV. TOP REFERENCE
(12) RFIN1 :SELF BIAS BUFFER INPUT
(13) CPREF :SELF BIAS BUFFER INVERTED OUTPUT (FEEDBACK)
(16) CP OUT :SELF BIAS BUFFER OUT
(18) CLK :CLOCK INPUT (41.85MHz)
(20) PBH :POWER DOWN CONTROL
L:POWER DOWN
(38) REFCK :72 COUNT DOWN CLOCK OUT
(39) GCTL 1 :GAIN SELECT 1
(40) GCTL 2 :GAIN SELECT 2
(41) GCTL 3 :GAIN SELECT 3
(42) INSH :FILTER RESPONSE TIME SELECT 1
(43) HDH :FILTER RESPONSE TIME SELECT 2
(44) CPH :ADC/SELF BIAS BUFFER SELECT SETTING INPUT
(45) TRRH :DA OUTPUT CODE SELECT

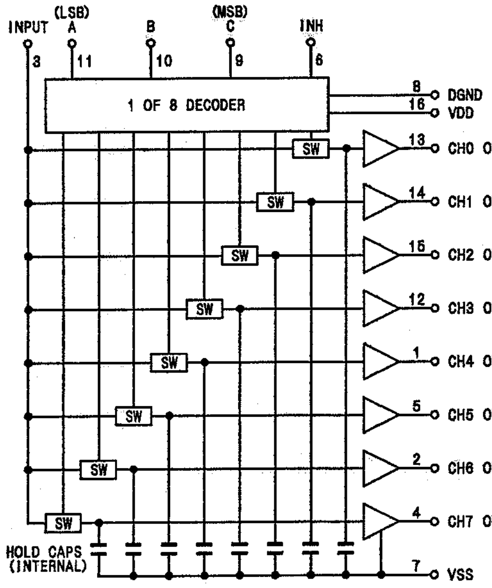
SLA909SF1G
(MOTOR CONTROL GATE ARRAY)


(TOP VIEW)
102 T8FG
101 T4FG
100 VDD
99
98 VSS1
97 FGCT11
96 FGCT10
95 FGCT9
94 FGCT8
93 VSS1
92 FGCT7
91 FGCT6
90 FGCT5
89 FGCT4
88 VSS1
87 FGCT3
86 FGCT2
85 FGCT1
84 FGCT0
83 VSS1
82 FRAME
81 CF
80 G500KH
79 VDD1
78 VSS1
77 D11
76 D10
75 D9
74 D8
73 VSS1
72 D7
71 D6
70 D5
69 D4
68 VSS1
67 VDD
66 D3
65 D2
T14FG 103
T18FG 104
T116FG 105
T4DIR 106
T8DIR 107
T16DIR 108
TFGS 109
S4FG 110
S8FG 111
VSS1 112
S14FG 113
S18FG 114
S116FG 115
S4DIR 116
S8DIR 117
S16DIR 118
SFGS 119
C4FG 120
C8FG 121
C16FG 122
VSS1 123
CFGS 124
C4DIR 125
C8DIR 126
C16DIR 127
ATFG 128
64 D1
63 D0
62 VSS1
61 CSN2
60 CSN1
59 WEN2
58 WEN1
57 RENO
56 WENO
55 02M
54 VSS1
53 04M
52 VSS1
51 RNW
50 DSN
49 CSN
48 ASN
47 CSN8I
46 CSN3I
45 ADR4
44 ADR3
43 ADR2
42 ADR1
41 ADR0
40 ADD10
39 ADD2
1 ATDIR
2 VSS1
3 VDD
4
5 FG
6 REV
7 CFG0
8 CFG1
9 CFG2
10 CFG3
11 CFG4
12 CFG5
13 CFG6
14 CFG7
15 SFG0
16 SFG1
17 SFG2
18 SFG3
19 SFG4
20 SFG5
21 SFG6
22 SFG7
23 TFG0
24 TFG1
25 TFG2
26 TFG3
27 TFG4
28 TFG5
29 TFG6
30 TFG7
31 CTL
32 VSS1
33 I16M
34 VSS1
35 I2M
36 VDD
37 TEST1
38 TEST2

SMP08FS
(SAMPLE/HOLD AMP)

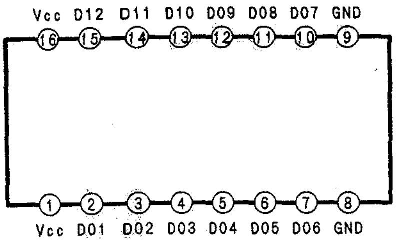

(TOP VIEW)
CH4 OUT 1
CH6 OUT 2
INPUT 3
CH7 OUT 4
CH5 OUT 5
INH 6
VSS 7
DGND 8
16 VDD
15 CH2 OUT
14 CH1 OUT
13 CH0 OUT
12 CH3 OUT
11 A CONTROL
10 B CONTROL
9 C CONTROL

BLOCK DIAGRAM

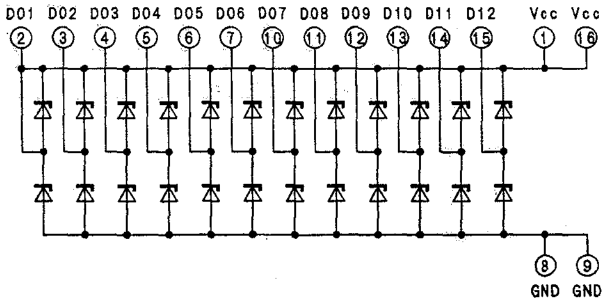

INPUT
(LSB)
A
B
(MSB)
C
INH
3
11
10
9
6
1 OF 8 DECODER
8 DGND
16 VDD
SW
13 CH0 OUT
14 CH1 OUT
15 CH2 OUT
12 CH3 OUT
1 CH4 OUT
5 CH5 OUT
2 CH6 OUT
4 CH7 OUT
HOLD CAPS
(INTERNAL)
7 VSS

SN74S1051NS
(DIODE ARRAY)

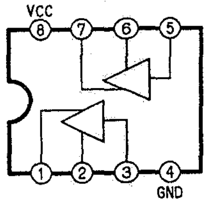
(TOP VIEW)


Vcc D12 D11 D10 D09 D08 D07 GND
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
Vcc D01 D02 D03 D04 D05 D06 GND

(BLOCK DIAGRAM)

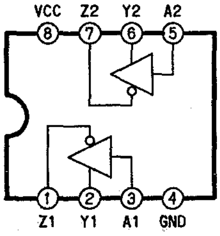

D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 Vcc Vcc
2 3 4 5 6 7 10 11 12 13 14 15 1 16
8 9
GND GND

SN75158PS
(40 MA.RS422)


VCC
8 7 6 5
1 2 3 4
GND

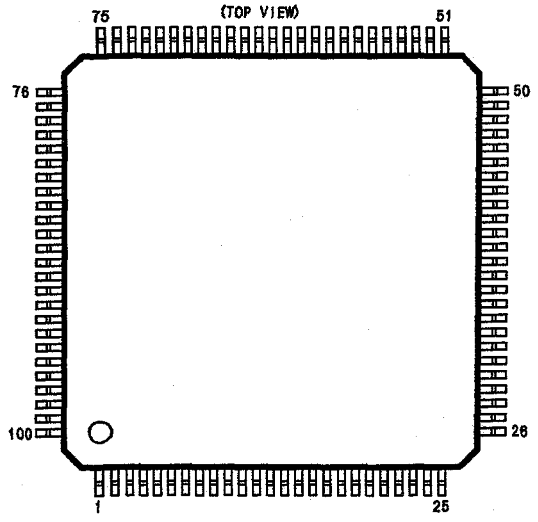
SN75158

(TOP VIEW)


VCC Z2 Y2 A2
8 7 6 5
1 2 3 4
Z1 Y1 A1 GND

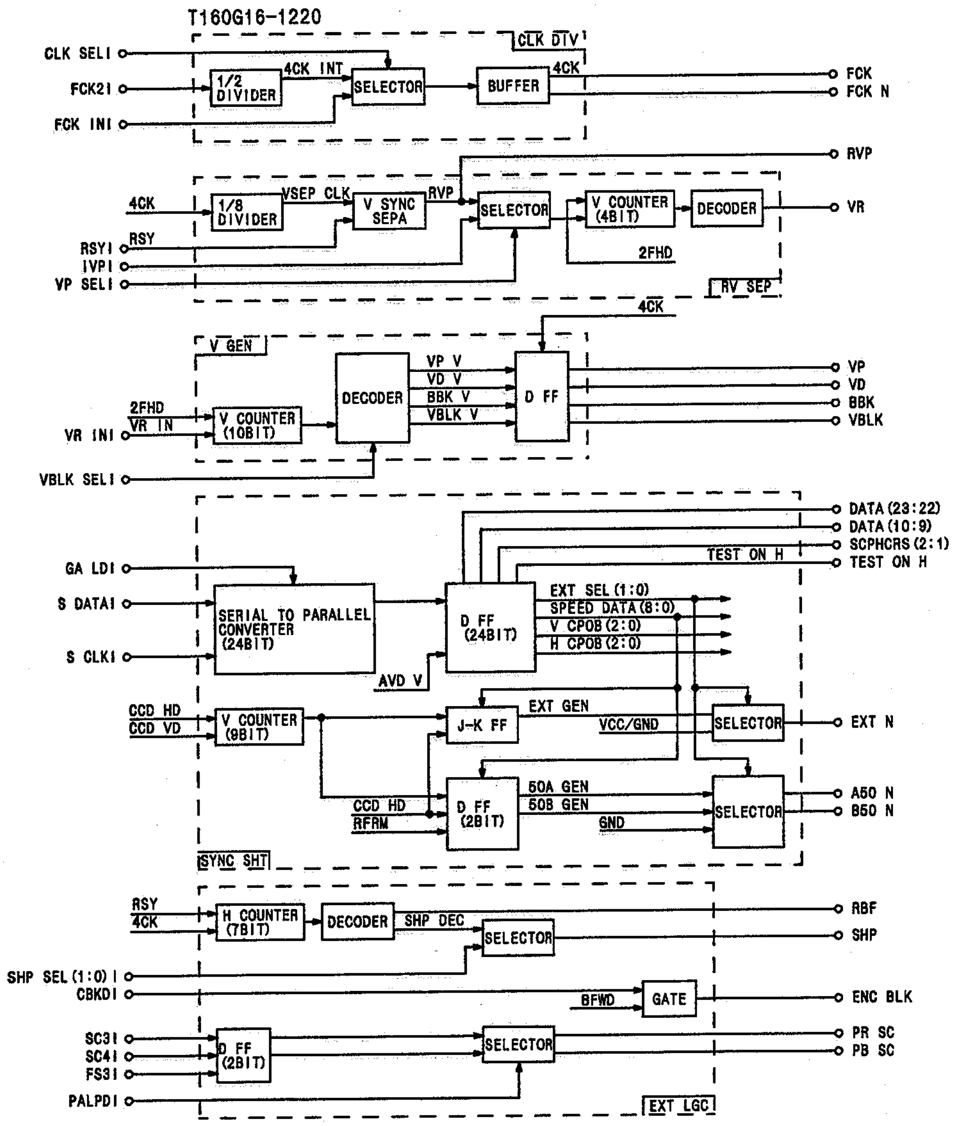
T160G16-1220
(GATE ARRAY-SYNC GENERATOR)

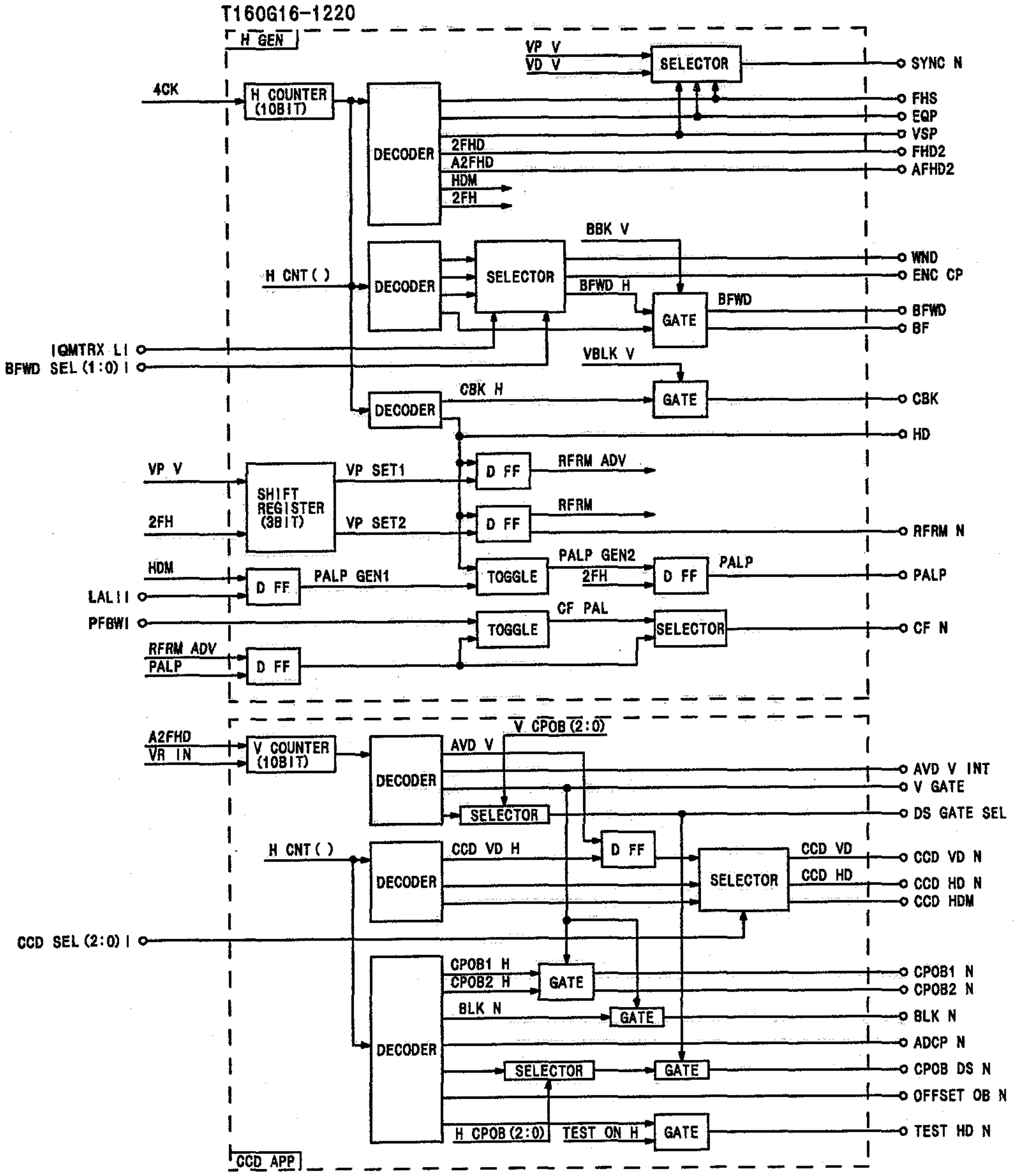
(TOP VIEW)


75
51
76
50
100
26
1
25

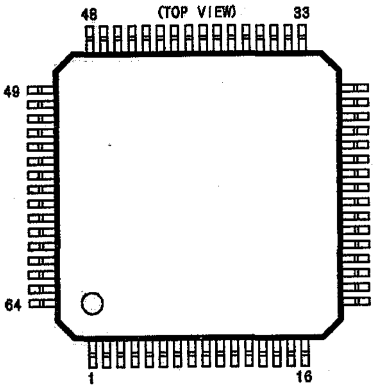
PIN ASSAINGMENT

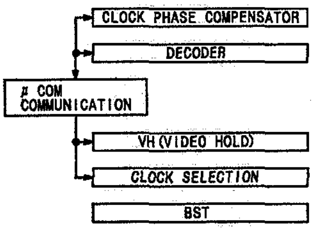
PIN NO.	PIN NAME	I/O	PIN NO.	PIN NAME	I/O
1	DATA9	OUT	51	DATA22	OUT
2	VSS	—	52	CPOB DS N	OUT
3	VDD	—	53	VDD	—
4	FHS	OUT	54	ADCP N	OUT
5	EQP	OUT	55	CPOB2 N	OUT
6	VSP	OUT	56	CPOB1 N	OUT
7	VR INI	IN	57	BLK N	OUT
8	VR	OUT	58	VSS	—
9	RVP	OUT	59	ENC BLK	OUT
10	DS GATE SEL	OUT	60	ENC CP	OUT
11	V GATE	OUT	61	GA LDI	IN
12	AVD V INT	OUT	62	S CLKI	IN
13	CCD HDM	OUT	63	S DATAI	IN
14	RBF	OUT	64	PR SC	OUT
15	VSS	—	65	VSS	—
16	SHP SEL0I	IN	66	PB SC	OUT
17	SHP SEL1I	IN	67	EXT N	OUT
18	SHP	OUT	68	B50 N	OUT
19	FCK INI	IN	69	A50 N	OUT
20	FCK2I	IN	70	RFRM N	OUT
21	CLK SELI	IN	71	PALPDI	IN
22	WND	OUT	72	PALP	OUT
23	TESTON H	OUT	73	CBKDI	IN
24	TEST HD N	OUT	74	VD	OUT
25	OFFSET OB N	OUT	75	HD	OUT
26	DATA10	OUT	76	DATA23	OUT
27	BFWD	OUT	77	FCK N	OUT
28	VDD	—	78	VDD	—
29	BFWD SEL0I	IN	79	FCK	OUT
30	BFWD SEL1I	IN	80	CBK	OUT
31	FHD2	OUT	81	BF	OUT
32	AFHD2	OUT	82	SYNC N	OUT
33	BBK	OUT	83	CCD VD N	OUT
34	VBLK	OUT	84	CCD HD N	OUT
35	VP	OUT	85	RSYI	IN
36	CF N	OUT	86	LALII	IN
37	TEST IN8I	IN	87	PFBWI	IN
38	TEST IN7I	IN	88	SCPHCRS1	OUT
39	TEST IN6I	IN	89	SCPHCRS2	OUT
40	VSS	—	90	VSS	—
41	TEST IN5I	IN	91	IVPI	IN
42	TEST IN4I	IN	92	VP SELI	IN
43	TEST IN3I	IN	93	CCD SEL0I	IN
44	TEST IN2I	IN	94	CCD SEL1I	IN
45	TEST IN1I	IN	95	CCD SEL2I	IN
46	TEST3I	IN	96	VBLK SELI	IN
47	TEST2I	IN	97	IQMTRX LI	IN
48	TEST1I	IN	98	SC4I	IN
49	NTSC LI	IN	99	SC3I	IN
50	MRST LI	IN	100	FS3I	IN


T160G16-1220
CLK DIV
CLK SELI
FCK2I
FCK INI
1/2 DIVIDER
4CK INT
SELECTOR
BUFFER
4CK
FCK
FCK N
RVP
4CK
1/8 DIVIDER
VSEP CLK
V SYNC SEPA
RVP
SELECTOR
V COUNTER (4BIT)
DECODER
VR
RSYI
RSY
IVPI
VP SELI
2FHD
RV SEP
4CK
V GEN
VP V
VD V
BBK V
VBLK V
DECODER
D FF
VP
VD
BBK
VBLK
2FHD
VR IN
VR INI
V COUNTER (10BIT)
VBLK SELI
DATA (23:22)
DATA (10:9)
SCPHCRS (2:1)
TEST ON H
TEST ON H
GA LDI
S DATAI
S CLKI
SERIAL TO PARALLEL CONVERTER (24BIT)
D FF (24BIT)
EXT SEL (1:0)
SPEED DATA (8:0)
V CPOB (2:0)
H CPOB (2:0)
AVD V
CCD HD
CCD VD
V COUNTER (9BIT)
J-K FF
EXT GEN
VCC/GND
SELECTOR
EXT N
CCD HD
RFRM
D FF (2BIT)
50A GEN
50B GEN
GND
SELECTOR
A50 N
B50 N
SYNC SHT
RSY
4CK
H COUNTER (7BIT)
DECODER
SHP DEC
SELECTOR
RBF
SHP
SHP SEL (1:0) I
CBKDI
BFWD
GATE
ENC BLK
SC3I
SC4I
FS3I
D FF (2BIT)
SELECTOR
PR SC
PB SC
PALPDI
EXT LGC


T160G16-1220
H GEN
4CK
H COUNTER (10BIT)
DECODER
VP V
VD V
SELECTOR
SYNC N
FHS
EQP
VSP
2FHD
FHD2
A2FHD
AFHD2
HDM
2FH
BBK V
H CNT( )
DECODER
SELECTOR
WND
ENC CP
BFWD H
BFWD
GATE
BFWD
BF
IQMTRX L I
BFWD SEL(1:0) I
VBLK V
CBK H
DECODER
GATE
CBK
HD
VP V
SHIFT REGISTER (3BIT)
VP SET1
D FF
RFRM ADV
2FH
VP SET2
D FF
RFRM
RFRM N
HDM
D FF
PALP GEN1
TOGGLE
PALP GEN2
2FH
D FF
PALP
PALP
LAL I I
PFBW I
TOGGLE
CF PAL
SELECTOR
CF N
RFRM ADV
PALP
D FF
A2FHD
VR IN
V COUNTER (10BIT)
V CPOB(2:0)
DECODER
AVD V
AVD V INT
V GATE
SELECTOR
DS GATE SEL
H CNT( )
CCD VD H
D FF
DECODER
SELECTOR
CCD VD
CCD VD N
CCD HD
CCD HD N
CCD HDM
CCD SEL(2:0) I
CPOB1 H
CPOB2 H
GATE
CPOB1 N
CPOB2 N
BLK N
GATE
BLK N
DECODER
ADCP N
SELECTOR
GATE
CPOB DS N
OFFSET OB N
H CPOB(2:0)
TEST ON H
GATE
TEST HD N
CCD APP

T160G22-1225
(GATE ARRAY)

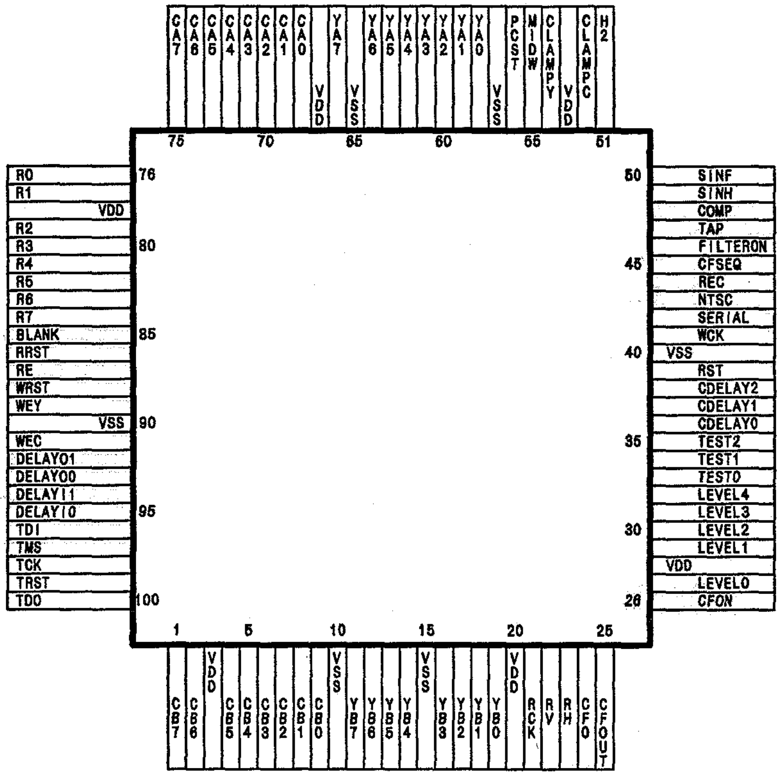

(TOP VIEW)
48
33
49
32
64
17
1
16


CLOCK PHASE COMPENSATOR
DECODER
μ COM
COMMUNICATION
VH (VIDEO HOLD)
CLOCK SELECTION
BST

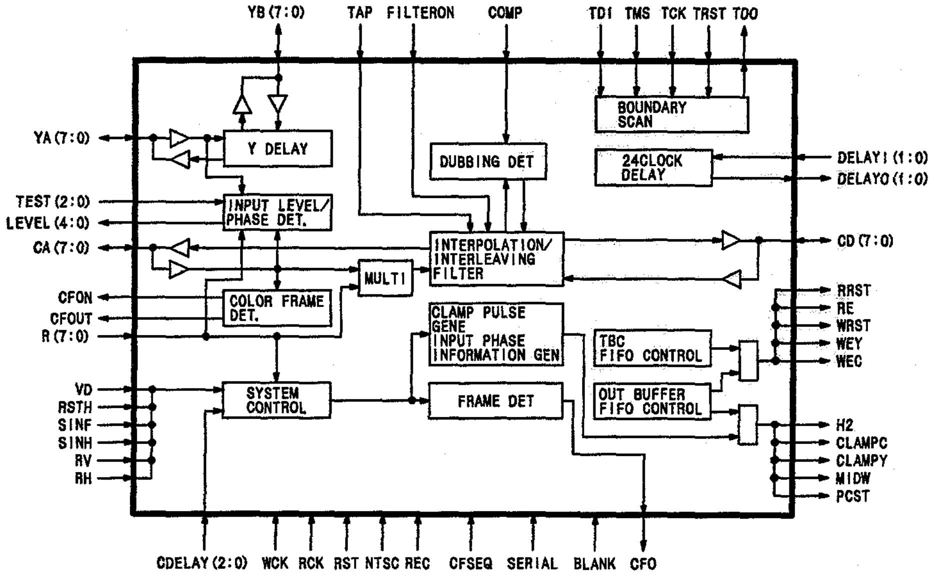
PIN ASSAINGMENT

PIN NO.	PIN NAME	I/O	PIN NO.	PIN NAME	I/O
1	VDD	—	33	VSS	—
2	AD0	IN	34	MON 00	OUT
3	AD1	IN	35	MON 01	OUT
4	AD2	IN	36	MON 02	OUT
5	AD3	IN	37	MON 03	OUT
6	AD4	IN	38	MON 04	OUT
7	AD5	IN	39	MON 05	OUT
8	AD6	IN	40	MON 06	OUT
9	CLKTST	IN	41	MON 07	OUT
10	VSS	—	42	VSS	—
11	M CLK	IN	43	TMS	IN
12	SEL CLK AD	OUT	44	TCK	IN
13	SEL CLK DCI	OUT	45	TDI	IN
14	VDD	—	46	TRST	IN
15	VSS	—	47	TDO	OUT
16	PBCLK	IN	48	RECSTR	IN
17	PBDAT I	IN	49	SBSTR	IN
18	PBDAT O	OUT	50	DEDR I0	IN
19	VSS	—	51	DEDR I1	IN
20	RST	IN	52	DEDR I2	IN
21	TEST	IN	53	DEDR I3	IN
22	RCA	IN	54	DEDR 00	OUT
23	RCB	IN	55	DEDR 01	OUT
24	HID	IN	56	DEDR 02	OUT
25	FRP	IN	57	DEDR 03	OUT
26	VDD	—	58	VDD	—
27	PBH	IN	59	S CS	IN
28	PWM	OUT	60	S CLK	IN
29	MON MD0	IN	61	S DATA	I/O
30	MON MD1	IN	62	CLK18	IN
31	MON MD2	IN	63	DREC	IN
32	MON MD3	IN	64	VSS	—

T160G41-1437
(GATE ARRAY (TBC)) (TOP VIEW)

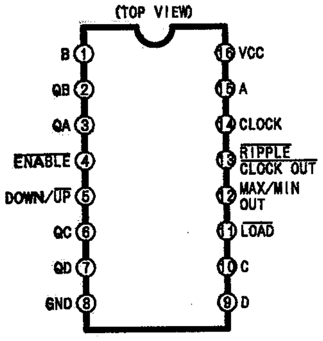

CA7
CA6
CA5
CA4
CA3
CA2
CA1
CA0
VDD
YA7
VSS
YA6
YA5
YA4
YA3
YA2
YA1
YA0
VSS
PCST
MIDW
CLAMPY
VDD
CLAMPC
H2
75
70
65
60
55
51
R0
R1
VDD
R2
R3
R4
R5
R6
R7
BLANK
RRST
RE
WRST
WEY
VSS
WEC
DELAYO1
DELAYO0
DELAYI1
DELAYI0
TDI
TMS
TCK
TRST
TDO
76
80
85
90
95
100
50
45
40
35
30
26
SINF
SINH
COMP
TAP
FILTERON
CFSEQ
REC
NTSC
SERIAL
WCK
VSS
RST
CDELAY2
CDELAY1
CDELAY0
TEST2
TEST1
TEST0
LEVEL4
LEVEL3
LEVEL2
LEVEL1
VDD
LEVEL0
CFON
1
5
10
15
20
25
CB7
CB6
VDD
CB5
CB4
CB3
CB2
CB1
CB0
VSS
YB7
YB6
YB5
YB4
VSS
YB3
YB2
YB1
YB0
VDD
RCK
RV
RH
CFO
CFOUT

BLOCK DIAGRAM

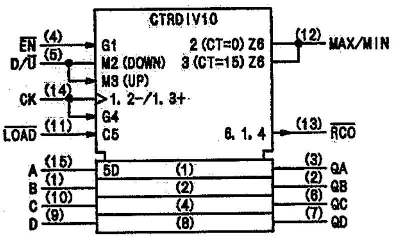

YB (7:0)
TAP
FILTERON
COMP
TDI
TMS
TCK
TRST
TDO
BOUNDARY SCAN
Y DELAY
DUBBING DET
24CLOCK DELAY
DELAYI (1:0)
DELAYO (1:0)
YA (7:0)
TEST (2:0)
LEVEL (4:0)
INPUT LEVEL/ PHASE DET.
CA (7:0)
INTERPOLATION/ INTERLEAVING FILTER
CD (7:0)
MULTI
CFON
CFOUT
R (7:0)
COLOR FRAME DET.
CLAMP PULSE GENE INPUT PHASE INFORMATION GEN
TBC FIFO CONTROL
RRST
RE
WRST
WEY
WEC
VD
RSTH
SINF
SINH
RV
RH
SYSTEM CONTROL
FRAME DET
OUT BUFFER FIFO CONTROL
H2
CLAMPC
CLAMPY
MIDW
PCST
CDELAY (2:0)
WCK
RCK
RST
NTSC
REC
CFSEQ
SERIAL
BLANK
CFO

T74HCT191A

(4 BIT BINARY UP/DOWN COUNTER)


(TOP VIEW)
B ①
QB ②
QA ③
$\overline{\text{ENABLE}}$ ④
DOWN/$\overline{\text{UP}}$ ⑤
QC ⑥
QD ⑦
GND ⑧
⑯ VCC
⑮ A
⑭ CLOCK
⑬ $\overline{\text{RIPPLE CLOCK OUT}}$
⑫ MAX/MIN OUT
⑪ $\overline{\text{LOAD}}$
⑩ C
⑨ D

LOGIC DIAGRAM

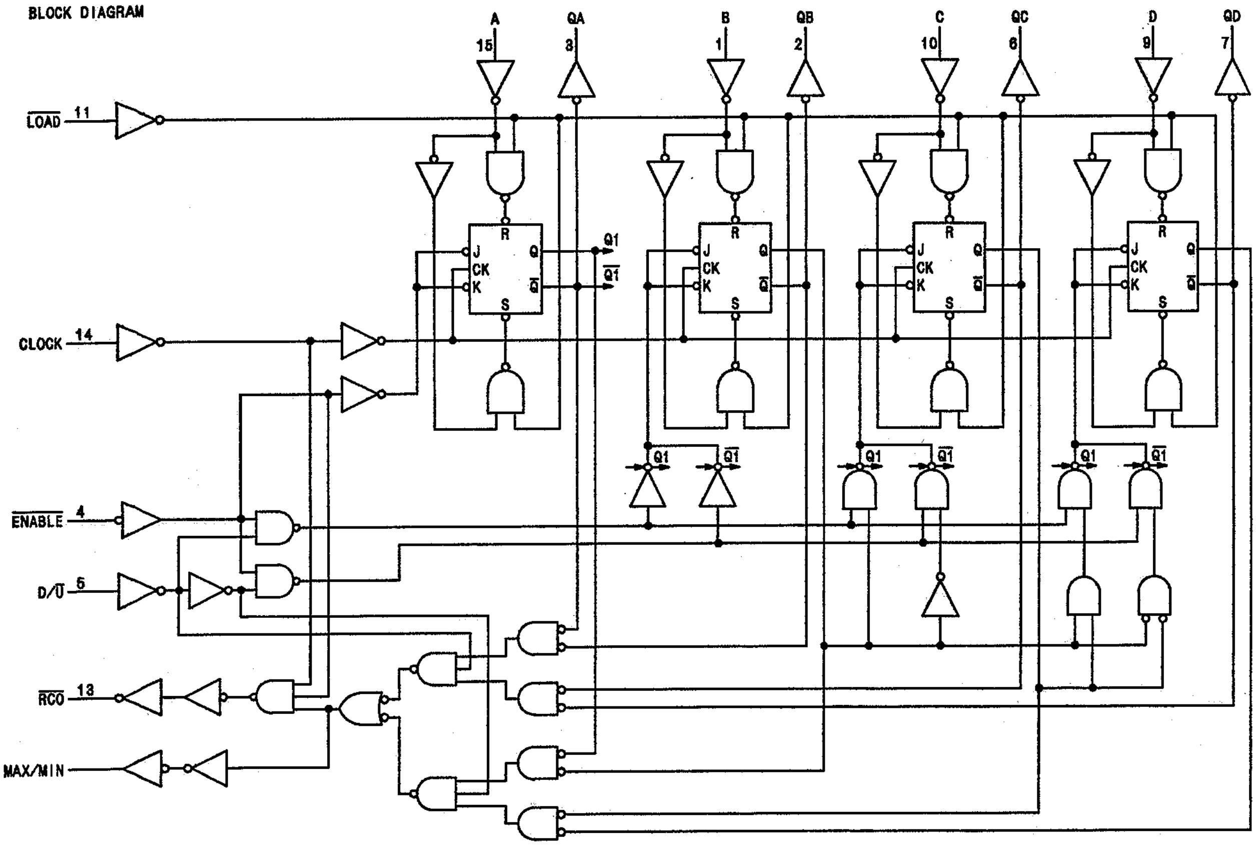

CTRDIV10
$\overline{\text{EN}}$ (4) G1
D/$\overline{\text{U}}$ (5) M2 (DOWN)
M3 (UP)
CK (14) >1, 2−/1, 3+
G4
$\overline{\text{LOAD}}$ (11) C5
2 (CT=0) Z6
3 (CT=15) Z6
(12) MAX/MIN
6, 1, 4
(13) $\overline{\text{RCO}}$
A (15) 5D (1) (3) QA
B (1) (2) (2) QB
C (10) (4) (6) QC
D (9) (8) (7) QD

TRUTH TABLE

INPUTS				OUTPUTS				FUNCTION
$\overline{\text{LOAD}}$	$\overline{\text{ENABLE}}$	D/$\overline{\text{U}}$	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	PRESET DATA
H	L	L	↑	UP COUNT				UP COUNT
H	L	H	↑	DOWN COUNT				DOWN COUNT
H	H	X	↑	NO CHANGE				NO COUNT
H	X	X	↓	NO CHANGE				NO COUNT

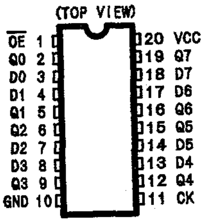
NOTE X:DON'T CARE
a~d: INPUT LEVEL INTO A~D

BLOCK DIAGRAM


A
15
QA
3
B
1
QB
2
C
10
QC
6
D
9
QD
7
$\overline{\text{LOAD}}$ 11
CLOCK 14
$\overline{\text{ENABLE}}$ 4
D/$\overline{\text{U}}$ 5
$\overline{\text{RCO}}$ 13
MAX/MIN
J
CK
K
R
S
Q
$\overline{\text{Q}}$
Q1
$\overline{\text{Q1}}$

T74HCT374A
(OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT)

(TOP VIEW)



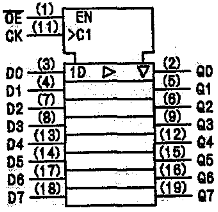
$\overline{OE}$ 1
Q0 2
D0 3
D1 4
Q1 5
Q2 6
D2 7
D3 8
Q3 9
GND 10
20 VCC
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 CK

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (T374A)	$\overline{Q}$ (T534A)
H	X	X	Z	Z
L	↓	X	Qn	$\overline{Qn}$
L	↑	L	L	H
L	↑	H	H	L

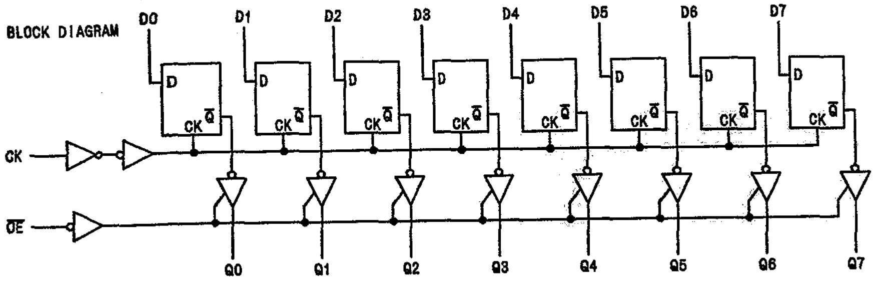
X:DON' T CARE
Z:HIGH IMPEDANCE
Qn ($\overline{Qn}$) :NOT VARIABLE

LOGIC DIAGRAM



$\overline{OE}$
(1)
CK
(11)
EN
>C1
1D
D0 (3)
D1 (4)
D2 (7)
D3 (8)
D4 (13)
D5 (14)
D6 (17)
D7 (18)
(2) Q0
(5) Q1
(6) Q2
(9) Q3
(12) Q4
(15) Q5
(16) Q6
(19) Q7

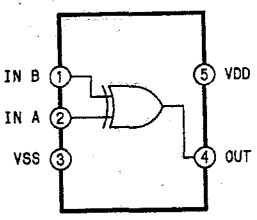
BLOCK DIAGRAM



D0
D1
D2
D3
D4
D5
D6
D7
D
CK
$\overline{Q}$
CK
$\overline{OE}$
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

TC4S30F
(EXCLUSIVE-OR GATE)

(TOP VIEW)



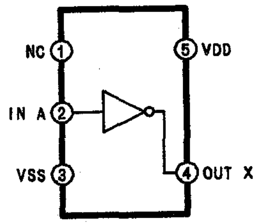
IN B ①
IN A ②
VSS ③
⑤ VDD
④ OUT X

TRUTH TABLE

INPUT		OUTPUT
A	B	X
L	L	L
L	H	H
H	L	H
H	H	L

TC4S69F
(INVETER GATE)

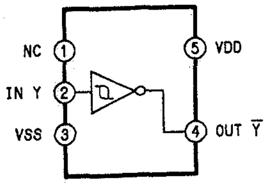
(TOP VIEW)



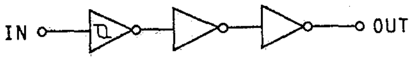
NC ①
IN A ②
VSS ③
⑤ VDD
④ OUT X

TC4S584F
(SCHMITT TRIGGER)

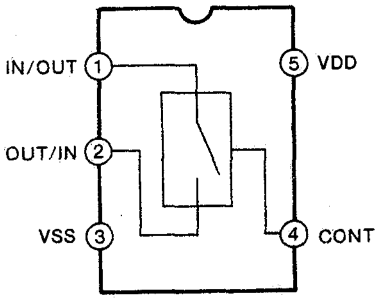
(TOP VIEW)



NC ①
IN Y ②
VSS ③
⑤ VDD
④ OUT $\overline{Y}$

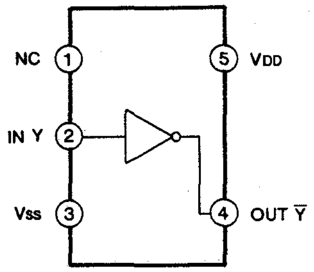


TC4S66F
(BILATERAL SWITCH)



IN/OUT ①
OUT/IN ②
VSS ③
⑤ VDD
④ CONT

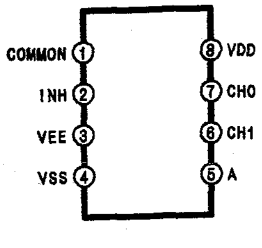
TC7S04F
(C-MOS INVERTER)



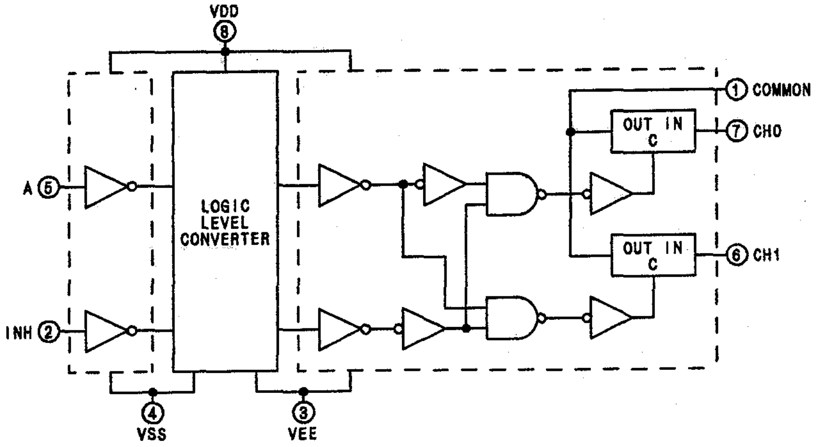
NC ①
IN Y ②
Vss ③
⑤ VDD
④ OUT $\overline{Y}$

TC4W53FU
(2-CHANNEL MULTIPLEXER/DEMULTIPLEXER)

(TOP VIEW)

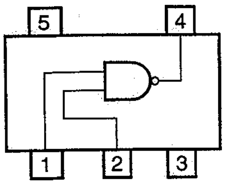


COMMON ①
INH ②
VEE ③
VSS ④
⑧ VDD
⑦ CH0
⑥ CH1
⑤ A



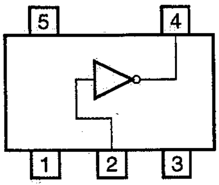
VDD
⑧
A ⑤
INH ②
LOGIC LEVEL CONVERTER
OUT IN
C
① COMMON
⑦ CH0
⑥ CH1
④
VSS
③
VEE

TC7S00F(2 INPUT NAND GATE)



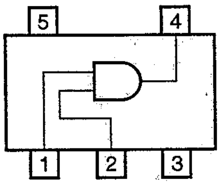
$Y = \overline{A \cdot B}$

TC7S04F(INVERTER)



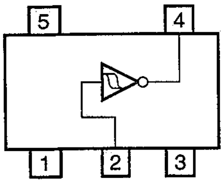
$Y = \overline{A}$

TC7S08F(2 INPUT AND GATE)



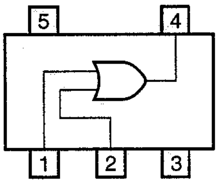
$Y = A \cdot B$

TC7S14F(SCHMITT INVERTER)



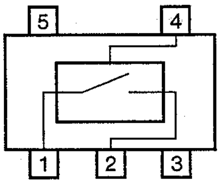
$Y = \overline{A}$

TC7S32F(2 INPUT OR GATE)

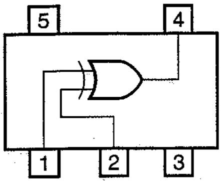


$Y = A + B$

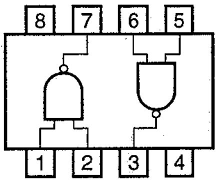
TC7S66F(ANALOG SWITCH)



TC7S86F(2 INPUT EXCLUSIVE OR GATE)

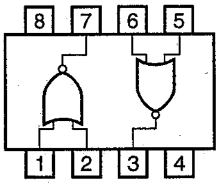


TC7W00F(DUAL 2 INPUT NAND GATE)



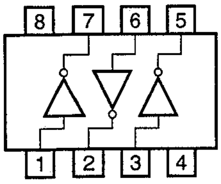
$Y = \overline{A \cdot B}$

TC7W02F(DUAL 2 INPUT NOR GATE)



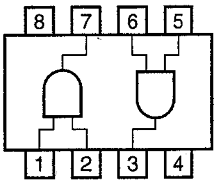
$Y = \overline{A + B}$

TC7W04F(TRIPLE INVERTER)



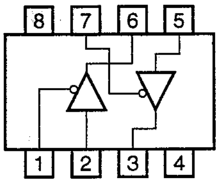
$Y = \overline{A}$

TC7W08F(DUAL 2 INPUT AND GATE)

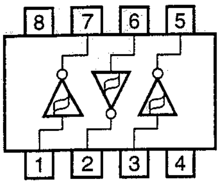


$Y = A \cdot B$

TC7W125FU(DUAL 3-STATE BUFFER)

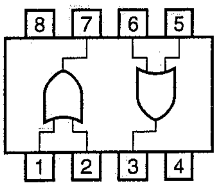


TC7W14F(TRIPLE SCHMITT INVERTER)



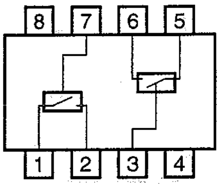
$Y = \overline{A}$

TC7W32F(DUAL 2 INPUT OR GATE)



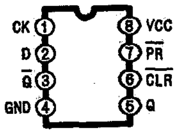
$Y = A + B$

TC4W66F(DUAL ANALOG SWITCH)

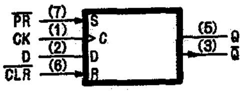


TC7W74F
(D TYPE FLIP FLOP WITH PRESET AND CLEAR)

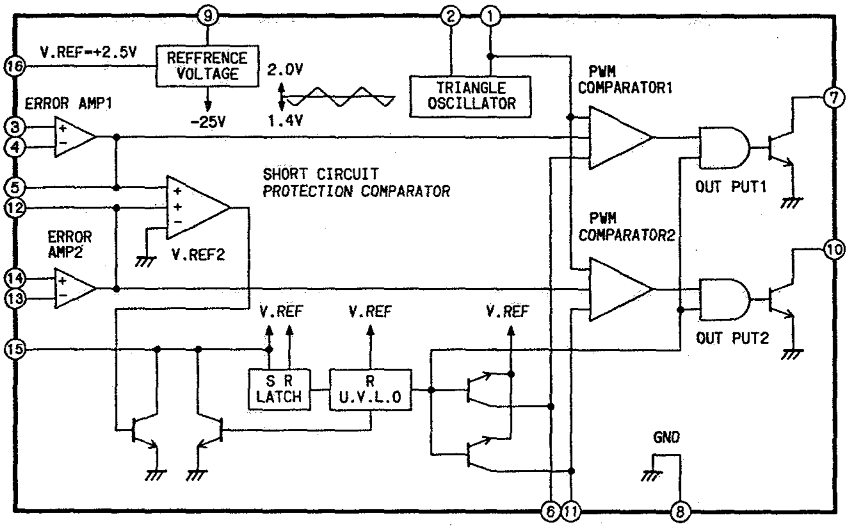
(TOP VIEW)


CK ①
D ②
Q̄ ③
GND ④
⑧ VCC
⑦ P̄R̄
⑥ C̄L̄R̄
⑤ Q

LOGIC BLOCK DIAGRAM

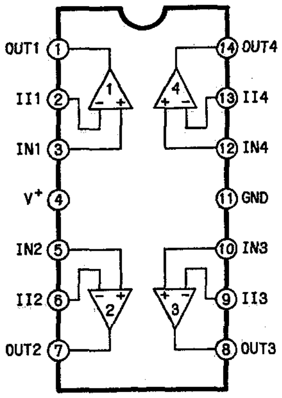

P̄R̄ (7)
CK (1)
D (2)
C̄L̄R̄ (6)
S
C
D
R
(5) Q
(3) Q̄

TL1451CNS
(DUAL SWITCHING REGULATOR CONTROLLER)

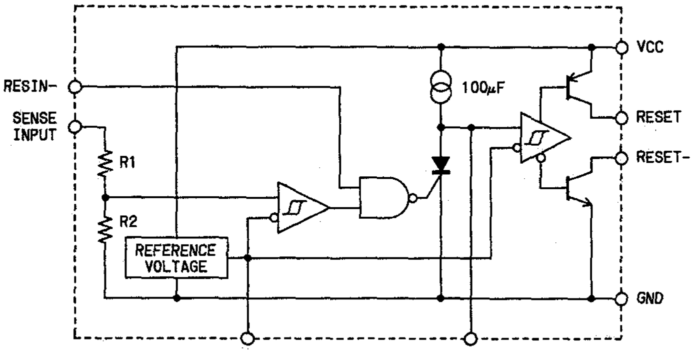

⑨
②
①
V.REF=+2.5V
REFFRENCE VOLTAGE
2.0V
1.4V
-25V
TRIANGLE OSCILLATOR
PWM COMPARATOR1
⑦
⑯
ERROR AMP1
③
④
⑤
⑫
SHORT CIRCUIT PROTECTION COMPARATOR
V.REF2
OUT PUT1
PWM COMPARATOR2
⑩
ERROR AMP2
⑭
⑬
V.REF
V.REF
V.REF
OUT PUT2
⑮
S R LATCH
R U.V.L.O
GND
⑥
⑪
⑧

TL084
(OPERATIONAL AMPLIFIER)

(TOP VIEW)

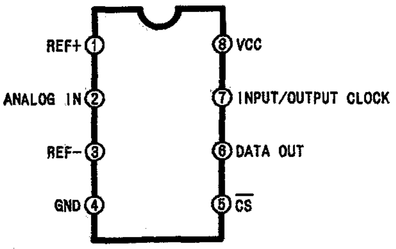

OUT1 ①
II1 ②
IN1 ③
V⁺ ④
IN2 ⑤
II2 ⑥
OUT2 ⑦
⑭ OUT4
⑬ II4
⑫ IN4
⑪ GND
⑩ IN3
⑨ II3
⑧ OUT3
1
2
3
4

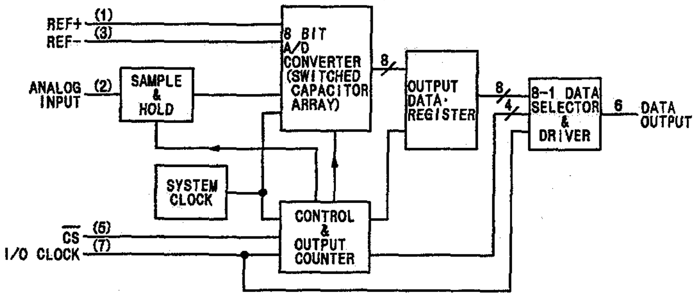
TL7705
(SUPPLY VOLTAGE SUPERVISOR CIRCUIT)


VCC
RESIN-
100μF
SENSE INPUT
RESET
RESET-
R1
R2
REFERENCE VOLTAGE
GND

TLC548C/549C
(8 BIT BINARY COMPATIBLE A/D CONVERTER)

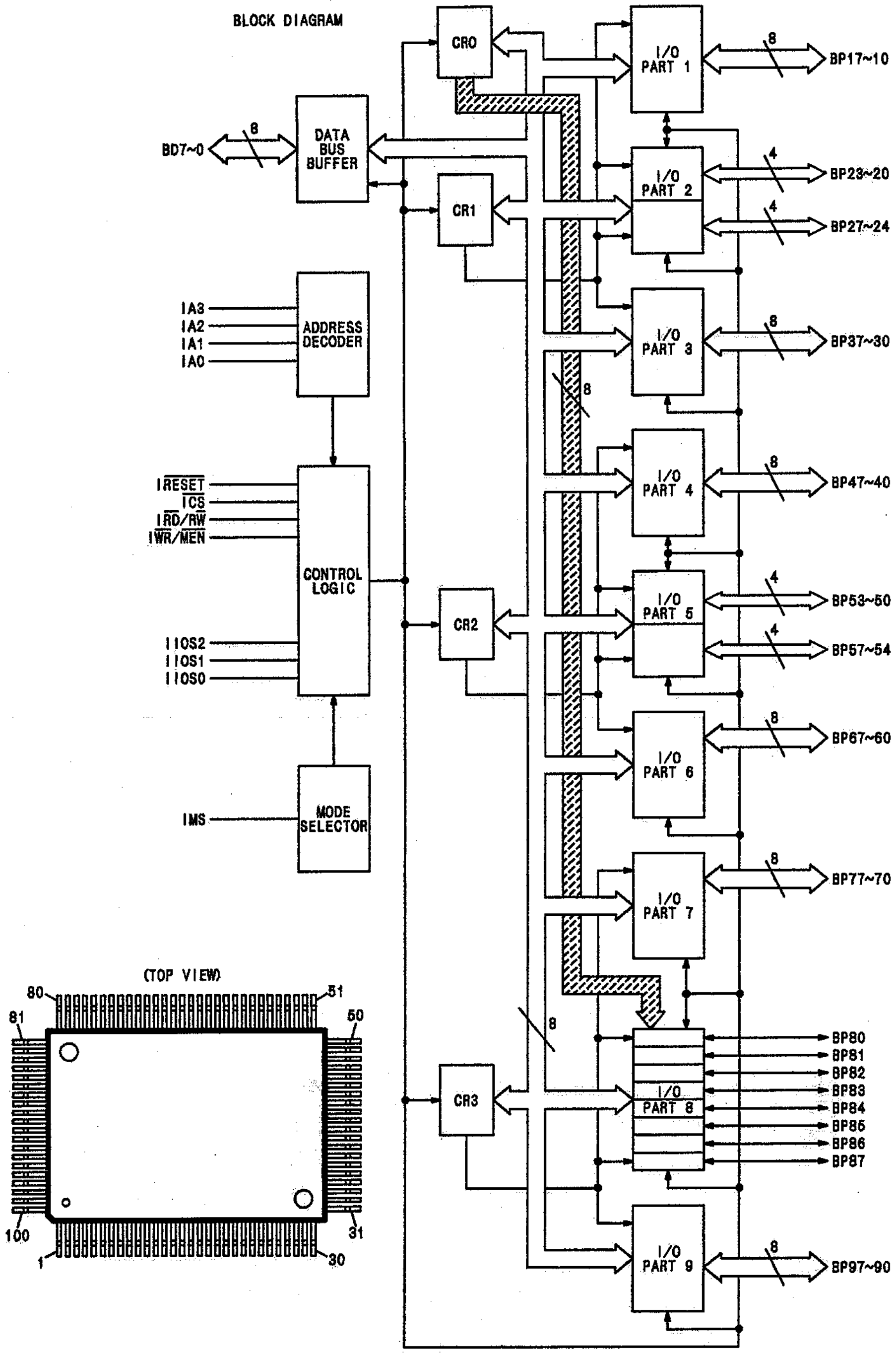
(TOP VIEW)


REF+ ①
ANALOG IN ②
REF- ③
GND ④
⑧ VCC
⑦ INPUT/OUTPUT CLOCK
⑥ DATA OUT
⑤ C̄S̄


REF+ (1)
REF- (3)
8 BIT A/D CONVERTER (SWITCHED CAPACITOR ARRAY)
8
ANALOG INPUT (2)
SAMPLE & HOLD
OUTPUT DATA REGISTER
8
4
8-1 DATA SELECTOR & DRIVER
6
DATA OUTPUT
SYSTEM CLOCK
C̄S̄ (5)
I/O CLOCK (7)
CONTROL & OUTPUT COUNTER

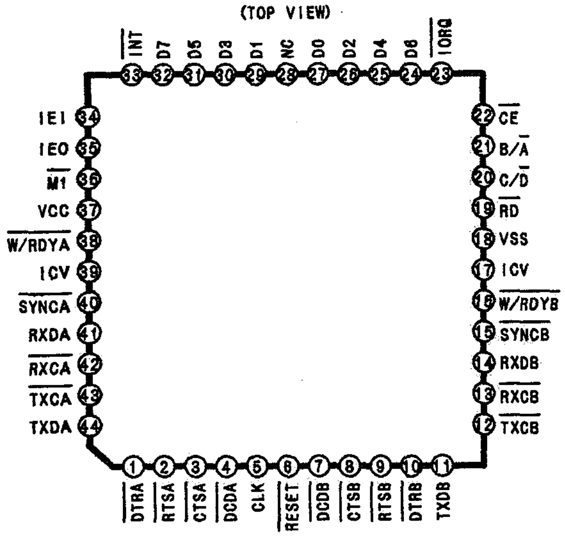
TE7751
(SUPER I/O EXPANDER)

BLOCK DIAGRAM

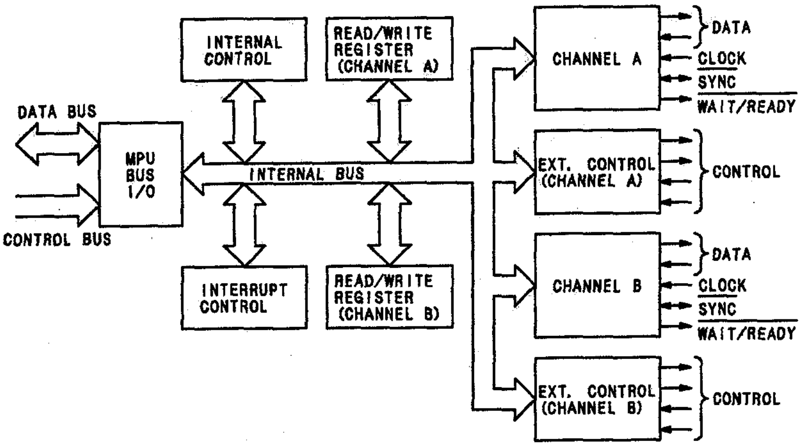

BD7~0
8
DATA BUS BUFFER
IA3
IA2
IA1
IA0
ADDRESS DECODER
IRESET
ICS
IRD/RW
IWR/MEN
CONTROL LOGIC
IIOS2
IIOS1
IIOS0
IMS
MODE SELECTOR
CR0
CR1
CR2
CR3
8
8
I/O PART 1
I/O PART 2
I/O PART 3
I/O PART 4
I/O PART 5
I/O PART 6
I/O PART 7
I/O PART 8
I/O PART 9
BP17~10
BP23~20
BP27~24
BP37~30
BP47~40
BP53~50
BP57~54
BP67~60
BP77~70
BP80
BP81
BP82
BP83
BP84
BP85
BP86
BP87
BP97~90
8
4
4
8
8
4
4
8
8
8
(TOP VIEW)
80
51
81
50
100
31
1
30

TMPZ84C43AF-8
(SERIAL INPUT/OUTPUT CONTROLLER)

(TOP VIEW)


INT 33
D7 32
D5 31
D3 30
D1 29
NC 28
D0 27
D2 26
D4 25
D6 24
IORQ 23
IEI 34
IEO 35
M1 36
VCC 37
W/RDYA 38
ICV 39
SYNCA 40
RXDA 41
RXCA 42
TXCA 43
TXDA 44
22 CE
21 B/A
20 C/D
19 RD
18 VSS
17 ICV
16 W/RDYB
15 SYNCB
14 RXDB
13 RXCB
12 TXCB
1 DTRA
2 RTSA
3 CTSA
4 DCDA
5 CLK
6 RESET
7 DCDB
8 CTSB
9 RTSB
10 DTRB
11 TXDB

FUNCTION BLOCK DIAGRAM


INTERNAL CONTROL
READ/WRITE REGISTER (CHANNEL A)
DATA BUS
MPU BUS I/O
INTERNAL BUS
CONTROL BUS
INTERRUPT CONTROL
READ/WRITE REGISTER (CHANNEL B)
CHANNEL A
DATA
CLOCK
SYNC
WAIT/READY
EXT. CONTROL (CHANNEL A)
CONTROL
CHANNEL B
DATA
CLOCK
SYNC
WAIT/READY
EXT. CONTROL (CHANNEL B)
CONTROL

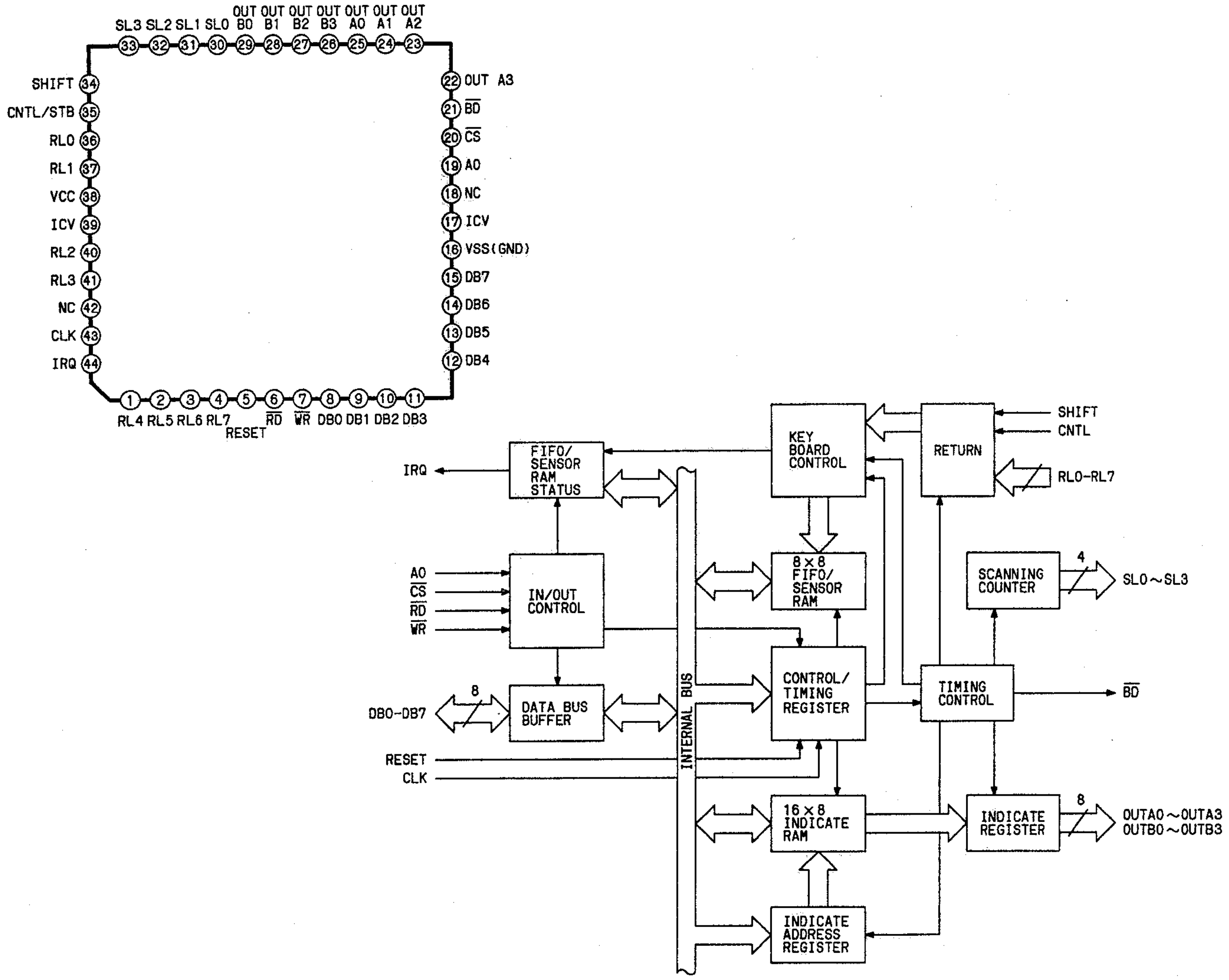
I/O CHART

PIN NO.	NAME	I/O	FUNCTION
1 10	$\overline{\text{DTRA}}$ $\overline{\text{DTRB}}$	O	DATA TERMINAL READY
2 9	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O	TRANSMIT REQUEST
3 8	$\overline{\text{CTSA}}$ $\overline{\text{CTSB}}$	I	TRANSMIT ABLE
4 7	$\overline{\text{DCDA}}$ $\overline{\text{DCDB}}$	I	DATA CARRIER DETECT
5	CLK	I	SINGLE PHASE CLOCK
6	$\overline{\text{RESET}}$	I	RESET
44 11	TXDA TXDB	O	SERIAL TRANSMIT DATA
43 12	$\overline{\text{TXCA}}$ $\overline{\text{TXCB}}$	I	TRANSMIT CLOCK
42 13	$\overline{\text{RXCA}}$ $\overline{\text{RXCB}}$	I	RECEIVE CLOCK
41 14	RXDA RXDB	I	SERIAL RECEIVE DATA

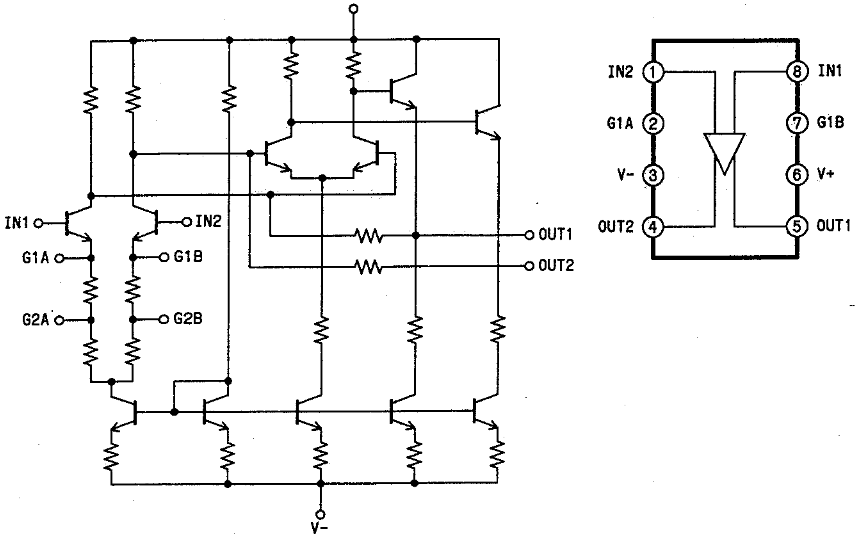
PIN NO.	NAME	I/O	FUNCTION
40 15	$\overline{\text{SYNCA}}$ $\overline{\text{SYNCB}}$	I/O	SYNC
38 16	$\overline{\text{W/RDYA}}$ $\overline{\text{W/RDYB}}$	O	WAIT/READY A, B
17	ICV	–	VCC OR OPEN
18	VSS	POWER	0V
19	$\overline{\text{RD}}$	I	READ SIGNAL
20	$\text{C}/\overline{\text{D}}$	I	COMMAND/DATA SELECT
21	$\text{B}/\overline{\text{A}}$	I	CHANNEL SELECT
22	$\overline{\text{CE}}$	I	CHIP ENABLE
23	$\overline{\text{IORQ}}$	I	I/O REQUEST
24~27 29~32	D0~D7	I/O	8 BIT BUS
33	$\overline{\text{INT}}$	O	INTERRUPT REQUEST
34	IEI	I	INTERRUPT INABLE INPUT
35	IEO	O	INTERRUPT INABLE OUTPUT
36	$\overline{\text{M1}}$	I	MACHINE CYCLE 1
37	VCC	POWER	+5V

TMP82C79F2

(CMOS PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE)


SL3 33
SL2 32
SL1 31
SL0 30
OUT B0 29
OUT B1 28
OUT B2 27
OUT B3 26
OUT A0 25
OUT A1 24
OUT A2 23
22 OUT A3
21 BD
20 CS
19 A0
18 NC
17 ICV
16 VSS(GND)
15 DB7
14 DB6
13 DB5
12 DB4
SHIFT 34
CNTL/STB 35
RL0 36
RL1 37
VCC 38
ICV 39
RL2 40
RL3 41
NC 42
CLK 43
IRQ 44
1 RL4
2 RL5
3 RL6
4 RL7
5 RESET
6 RD
7 WR
8 DB0
9 DB1
10 DB2
11 DB3
KEY BOARD CONTROL
RETURN
SHIFT
CNTL
RL0-RL7
FIFO/ SENSOR RAM STATUS
IRQ
8×8 FIFO/ SENSOR RAM
SCANNING COUNTER
4
SL0～SL3
A0
CS
RD
WR
IN/OUT CONTROL
CONTROL/ TIMING REGISTER
TIMING CONTROL
BD
DB0-DB7
8
DATA BUS BUFFER
INTERNAL BUS
RESET
CLK
16×8 INDICATE RAM
INDICATE REGISTER
8
OUTA0～OUTA3
OUTB0～OUTB3
INDICATE ADDRESS REGISTER

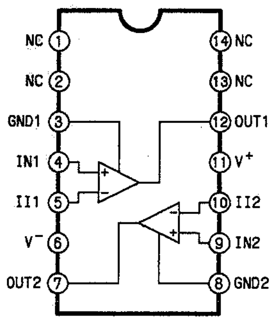
μPC1663


V+
IN1
IN2
G1A
G1B
G2A
G2B
OUT1
OUT2
V-
IN2 1
G1A 2
V- 3
OUT2 4
8 IN1
7 G1B
6 V+
5 OUT1

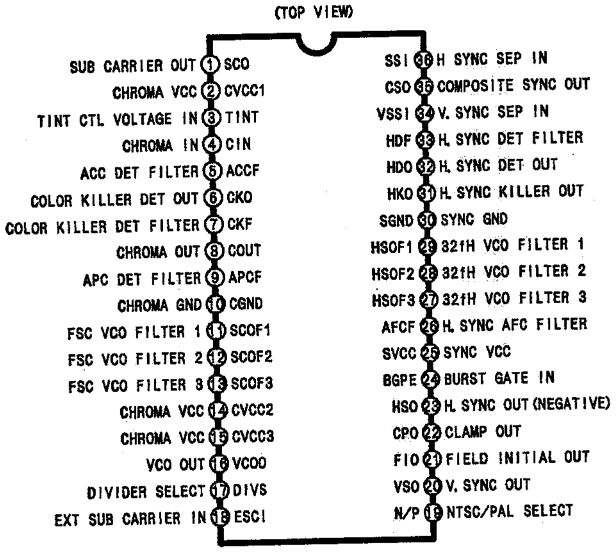
UPC319

(DUAL COMPARATOR)

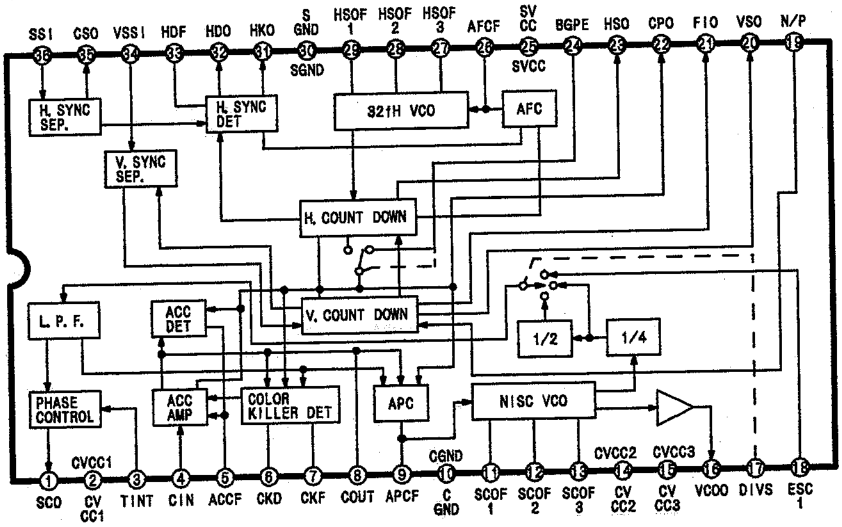
(TOP VIEW)


NC 1
NC 2
GND1 3
IN1 4
II1 5
V⁻ 6
OUT2 7
14 NC
13 NC
12 OUT1
11 V⁺
10 II2
9 IN2
8 GND2
+
-
-
+

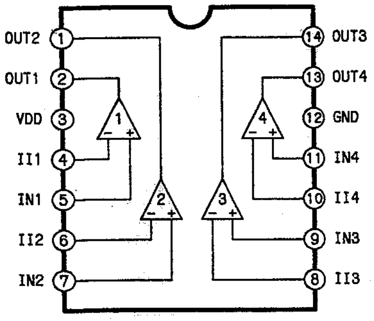
UPC1862GS
(VIDEO SIGNAL PROCESSOR CLOCK GENERATOR)


(TOP VIEW)
SUB CARRIER OUT ① SCO
CHROMA VCC ② CVCC1
TINT CTL VOLTAGE IN ③ TINT
CHROMA IN ④ CIN
ACC DET FILTER ⑤ ACCF
COLOR KILLER DET OUT ⑥ CKO
COLOR KILLER DET FILTER ⑦ CKF
CHROMA OUT ⑧ COUT
APC DET FILTER ⑨ APCF
CHROMA GND ⑩ CGND
FSC VCO FILTER 1 ⑪ SCOF1
FSC VCO FILTER 2 ⑫ SCOF2
FSC VCO FILTER 3 ⑬ SCOF3
CHROMA VCC ⑭ CVCC2
CHROMA VCC ⑮ CVCC3
VCO OUT ⑯ VCOO
DIVIDER SELECT ⑰ DIVS
EXT SUB CARRIER IN ⑱ ESCI
SSI ㊱ H SYNC SEP IN
CSO ㉟ COMPOSITE SYNC OUT
VSSI ㉞ V. SYNC SEP IN
HDF ㉝ H. SYNC DET FILTER
HDO ㉜ H. SYNC DET OUT
HKO ㉛ H. SYNC KILLER OUT
SGND ㉚ SYNC GND
HSOF1 ㉙ 32fH VCO FILTER 1
HSOF2 ㉘ 32fH VCO FILTER 2
HSOF3 ㉗ 32fH VCO FILTER 3
AFCF ㉖ H. SYNC AFC FILTER
SVCC ㉕ SYNC VCC
BGPE ㉔ BURST GATE IN
HSO ㉓ H. SYNC OUT (NEGATIVE)
CPO ㉒ CLAMP OUT
FIO ㉑ FIELD INITIAL OUT
VSO ⑳ V. SYNC OUT
N/P ⑲ NTSC/PAL SELECT

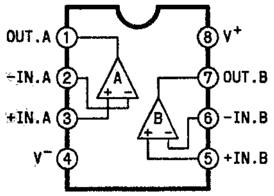
BLOCK DIAGRAM


SSI
CSO
VSSI
HDF
HDO
HKO
S GND
HSOF 1
HSOF 2
HSOF 3
AFCF
SV CC
BGPE
HSO
CPO
FIO
VSO
N/P
SGND
SVCC
H. SYNC SEP.
H. SYNC DET
32fH VCO
AFC
V. SYNC SEP.
H. COUNT DOWN
L. P. F.
ACC DET
V. COUNT DOWN
1/2
1/4
PHASE CONTROL
ACC AMP
COLOR KILLER DET
APC
NISC VCO
CVCC1
CGND
CVCC2
CVCC3
SCO
CV CC1
TINT
CIN
ACCF
CKD
CKF
COUT
APCF
C GND
SCOF 1
SCOF 2
SCOF 3
CV CC2
CV CC3
VCOO
DIVS
ESC 1

UPC339
(OPERATIONAL AMPLIFIER)
(TOP VIEW)

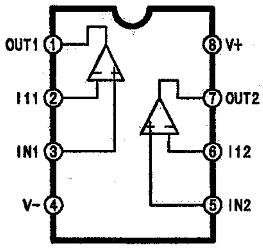

OUT2 ①
OUT1 ②
VDD ③
II1 ④
IN1 ⑤
II2 ⑥
IN2 ⑦
⑭ OUT3
⑬ OUT4
⑫ GND
⑪ IN4
⑩ II4
⑨ IN3
⑧ II3
1
2
3
4

UPC4082
(OPERATIONAL AMPLIFIER)
(TOP VIEW)


OUT.A ①
-IN.A ②
+IN.A ③
V⁻ ④
⑧ V⁺
⑦ OUT.B
⑥ -IN.B
⑤ +IN.B
A
B

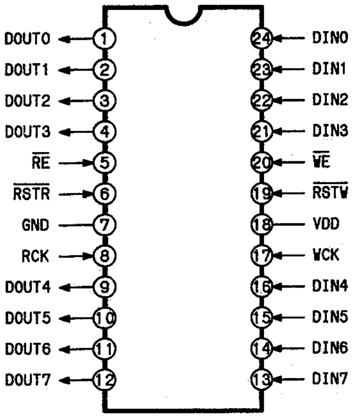
UPC4556
(OP AMP, WIDE BAND)

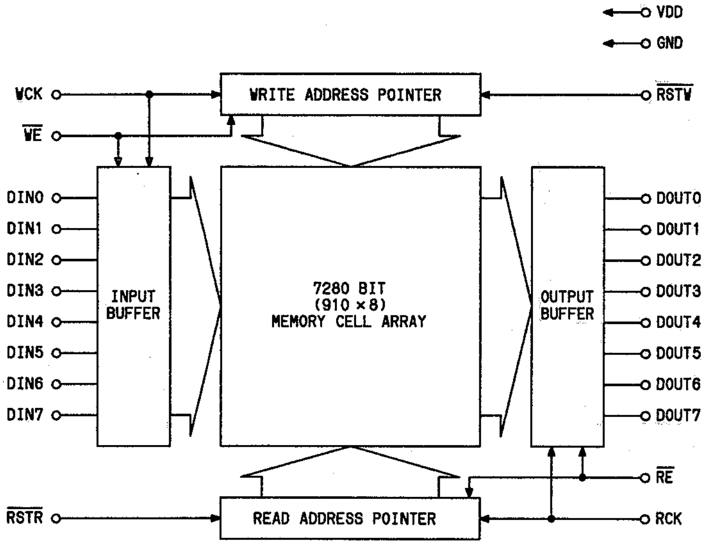
(TOP VIEW)


OUT1 ①
I11 ②
IN1 ③
V- ④
⑧ V+
⑦ OUT2
⑥ I12
⑤ IN2

μPD42101G (FIFO 1H DELAY)

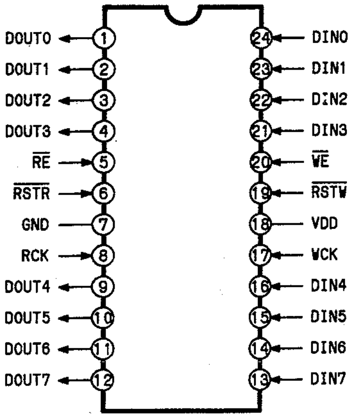
(TOP VIEW)

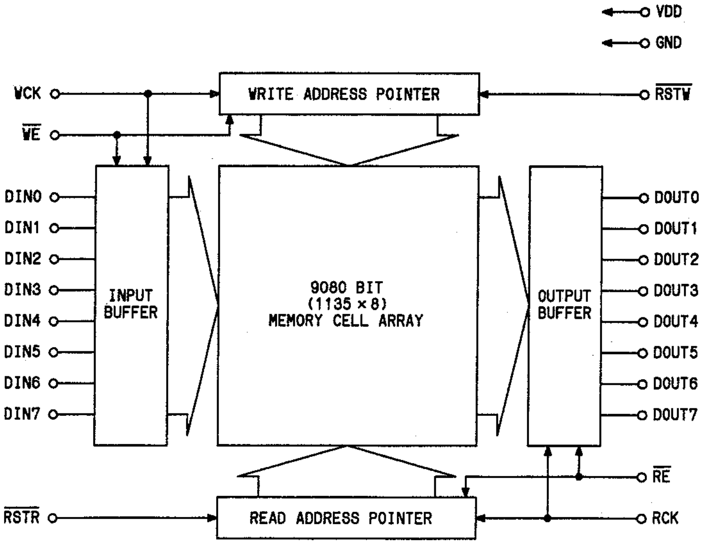

DOUT0 ①
DOUT1 ②
DOUT2 ③
DOUT3 ④
RE ⑤
RSTR ⑥
GND ⑦
RCK ⑧
DOUT4 ⑨
DOUT5 ⑩
DOUT6 ⑪
DOUT7 ⑫
㉔ DIN0
㉓ DIN1
㉒ DIN2
㉑ DIN3
⑳ WE
⑲ RSTW
⑱ VDD
⑰ WCK
⑯ DIN4
⑮ DIN5
⑭ DIN6
⑬ DIN7


VDD
GND
WCK
WE
RSTW
WRITE ADDRESS POINTER
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
INPUT BUFFER
7280 BIT
(910 × 8)
MEMORY CELL ARRAY
OUTPUT BUFFER
DOUT0
DOUT1
DOUT2
DOUT3
DOUT4
DOUT5
DOUT6
DOUT7
RE
RSTR
READ ADDRESS POINTER
RCK

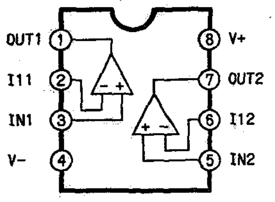
μPD42102G (FIFO 1H DELAY)

(TOP VIEW)


DOUT0 ①
DOUT1 ②
DOUT2 ③
DOUT3 ④
RE ⑤
RSTR ⑥
GND ⑦
RCK ⑧
DOUT4 ⑨
DOUT5 ⑩
DOUT6 ⑪
DOUT7 ⑫
㉔ DIN0
㉓ DIN1
㉒ DIN2
㉑ DIN3
⑳ WE
⑲ RSTW
⑱ VDD
⑰ WCK
⑯ DIN4
⑮ DIN5
⑭ DIN6
⑬ DIN7

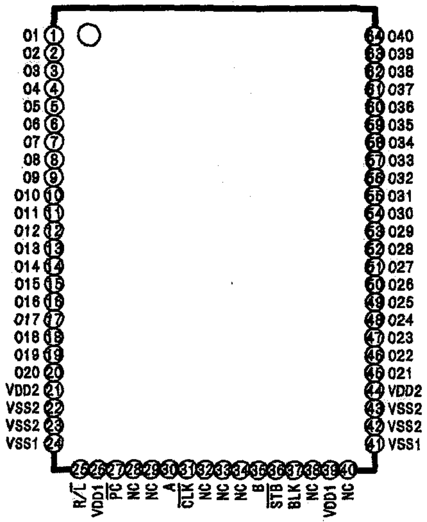

VDD
GND
WCK
WE
RSTW
WRITE ADDRESS POINTER
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
INPUT BUFFER
9080 BIT
(1135 × 8)
MEMORY CELL ARRAY
OUTPUT BUFFER
DOUT0
DOUT1
DOUT2
DOUT3
DOUT4
DOUT5
DOUT6
DOUT7
RE
RSTR
READ ADDRESS POINTER
RCK

UPC4558
(OPERATIONAL AMPLIFIER)
(TOP VIEW)

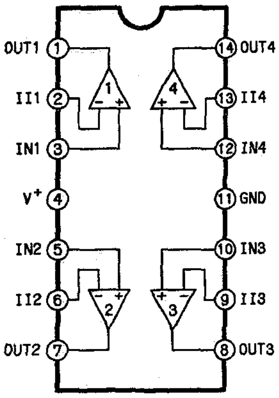

OUT1 1
II1 2
IN1 3
V- 4
IN2 5
II2 6
OUT2 7
V+ 8

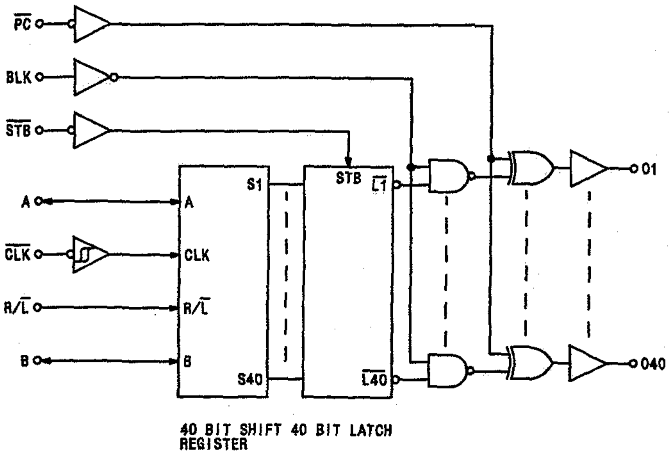
μPD16310GF
(DISPLAY TUBE DRIVER)

(TOP VIEW)


O1 1
O2 2
O3 3
O4 4
O5 5
O6 6
O7 7
O8 8
O9 9
O10 10
O11 11
O12 12
O13 13
O14 14
O15 15
O16 16
O17 17
O18 18
O19 19
O20 20
VDD2 21
VSS2 22
VSS2 23
VSS1 24
R/L̄ 25
VDD1 26
P̄C̄ 27
NC 28
NC 29
A 30
C̄L̄K̄ 31
NC 32
NC 33
NC 34
B 35
S̄T̄B̄ 36
BLK 37
NC 38
VDD1 39
NC 40
VSS1 41
VSS2 42
VSS2 43
VDD2 44
O21 45
O22 46
O23 47
O24 48
O25 49
O26 50
O27 51
O28 52
O29 53
O30 54
O31 55
O32 56
O33 57
O34 58
O35 59
O36 60
O37 61
O38 62
O39 63
O40 64

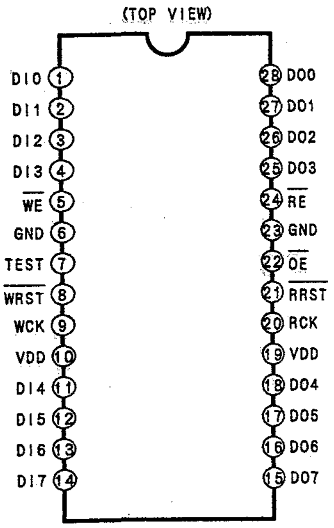
UPC4741
(OPERATIONAL AMPLIFIER)
(TOP VIEW)


OUT1 1
II1 2
IN1 3
V+ 4
IN2 5
II2 6
OUT2 7
OUT3 8
II3 9
IN3 10
GND 11
IN4 12
II4 13
OUT4 14


P̄C̄
BLK
S̄T̄B̄
A
C̄L̄K̄
R/L̄
B
A
CLK
R/L̄
B
S1
S40
STB
L̄1̄
L̄4̄0̄
O1
O40

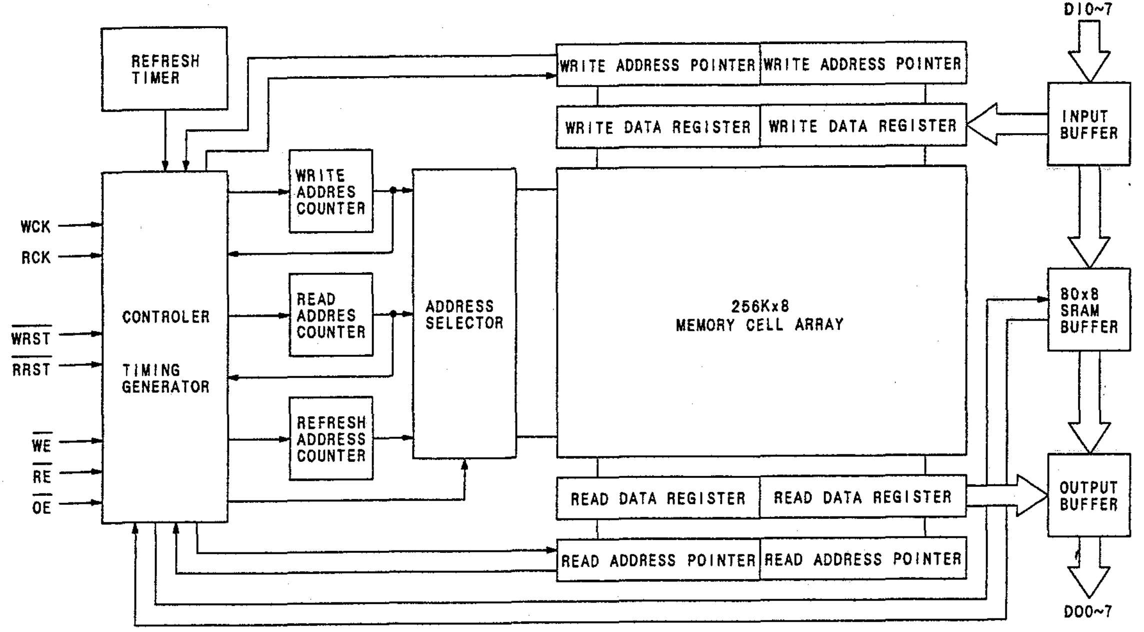
40 BIT SHIFT REGISTER 40 BIT LATCH

UPD42280
(2M BIT FIELD BUFFER)


(TOP VIEW)
DI0 1
DI1 2
DI2 3
DI3 4
$\overline{\text{WE}}$ 5
GND 6
TEST 7
$\overline{\text{WRST}}$ 8
WCK 9
VDD 10
DI4 11
DI5 12
DI6 13
DI7 14
28 DO0
27 DO1
26 DO2
25 DO3
24 $\overline{\text{RE}}$
23 GND
22 $\overline{\text{OE}}$
21 $\overline{\text{RRST}}$
20 RCK
19 VDD
18 DO4
17 DO5
16 DO6
15 DO7

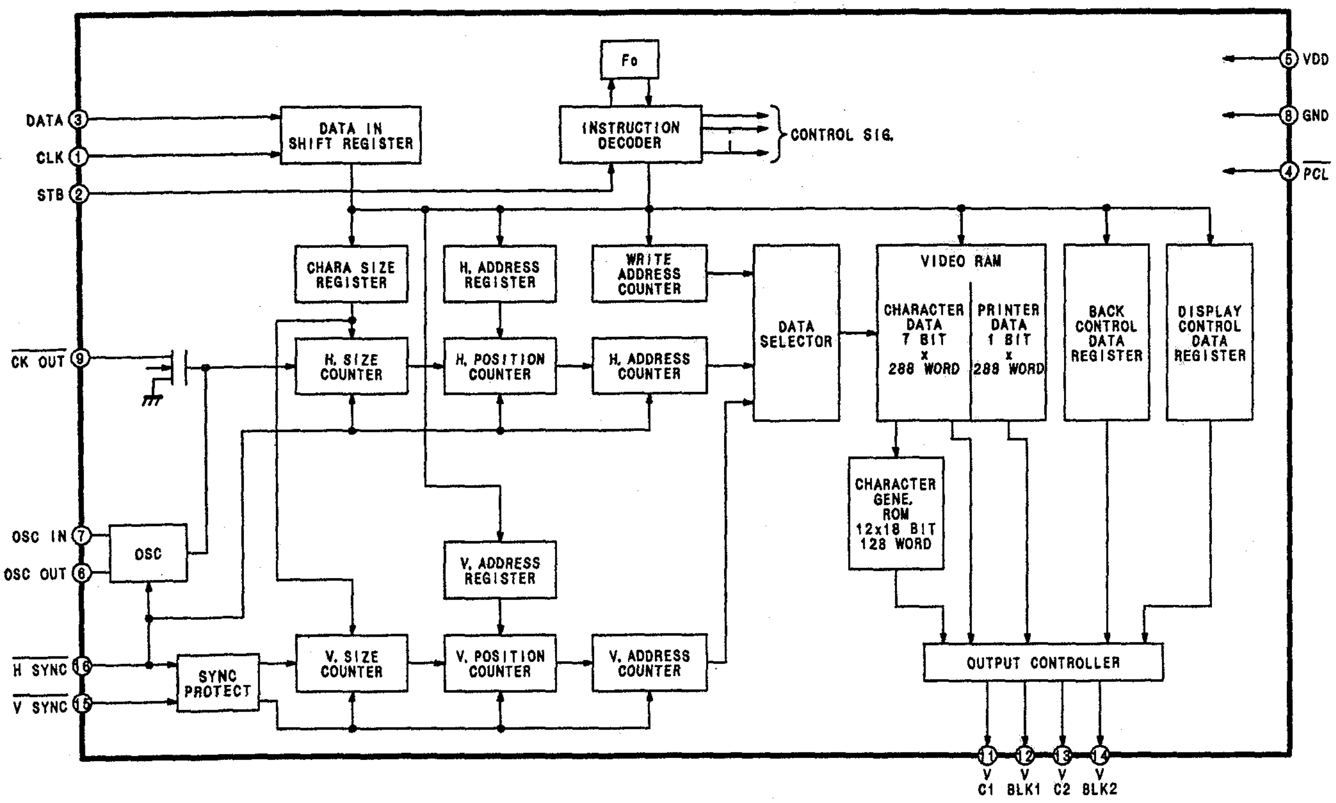
DI0~7:DATA INPUT
DO0~7:DATA OUTPUT
WCK :WRITE CLOCK
RCK :READ CLOCK
$\overline{\text{WE}}$:WRITE ENABLE IN
$\overline{\text{RE}}$:READ ENABLE IN
$\overline{\text{OE}}$:OUTPUT ENABLE IN
$\overline{\text{WRST}}$:WRITE RESET IN
$\overline{\text{RRST}}$:READ RESET IN
TEST :TEST TERMINAL

BLOCK DIAGRAM

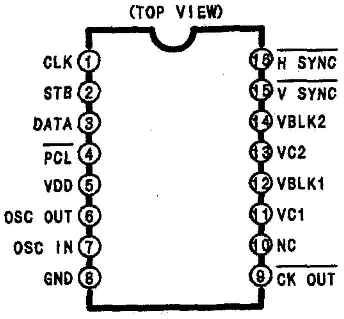

REFRESH TIMER
WCK
RCK
$\overline{\text{WRST}}$
$\overline{\text{RRST}}$
$\overline{\text{WE}}$
$\overline{\text{RE}}$
$\overline{\text{OE}}$
CONTROLER
TIMING GENERATOR
WRITE ADDRES COUNTER
READ ADDRES COUNTER
REFRESH ADDRESS COUNTER
ADDRESS SELECTOR
WRITE ADDRESS POINTER
WRITE ADDRESS POINTER
WRITE DATA REGISTER
WRITE DATA REGISTER
256Kx8 MEMORY CELL ARRAY
READ DATA REGISTER
READ DATA REGISTER
READ ADDRESS POINTER
READ ADDRESS POINTER
DI0~7
INPUT BUFFER
80x8 SRAM BUFFER
OUTPUT BUFFER
DO0~7

UPD6456

(ON-SCREEN CHARACTER DISPLAY)

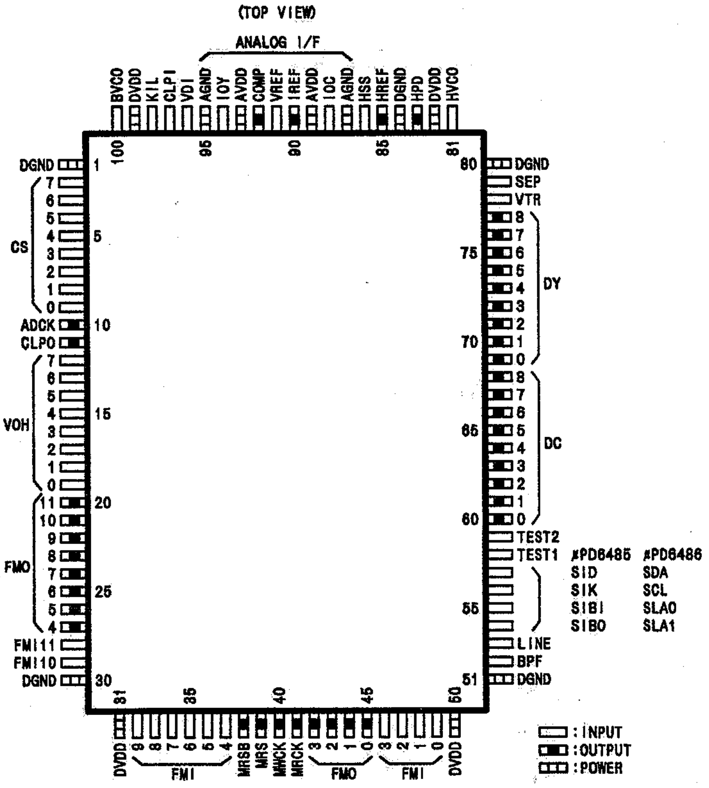


DATA ③
CLK ①
STB ②
CK OUT ⑨
OSC IN ⑦
OSC OUT ⑥
H SYNC ⑯
V SYNC ⑮
Fo
DATA IN SHIFT REGISTER
INSTRUCTION DECODER
CONTROL SIG.
⑤ VDD
⑧ GND
④ PCL
CHARA SIZE REGISTER
H. ADDRESS REGISTER
WRITE ADDRESS COUNTER
DATA SELECTOR
VIDEO RAM
CHARACTER DATA 7 BIT x 288 WORD
PRINTER DATA 1 BIT x 288 WORD
BACK CONTROL DATA REGISTER
DISPLAY CONTROL DATA REGISTER
H. SIZE COUNTER
H. POSITION COUNTER
H. ADDRESS COUNTER
OSC
V. ADDRESS REGISTER
CHARACTER GENE. ROM 12x18 BIT 128 WORD
SYNC PROTECT
V. SIZE COUNTER
V. POSITION COUNTER
V. ADDRESS COUNTER
OUTPUT CONTROLLER
⑪ V C1
⑫ V BLK1
⑬ V C2
⑭ V BLK2

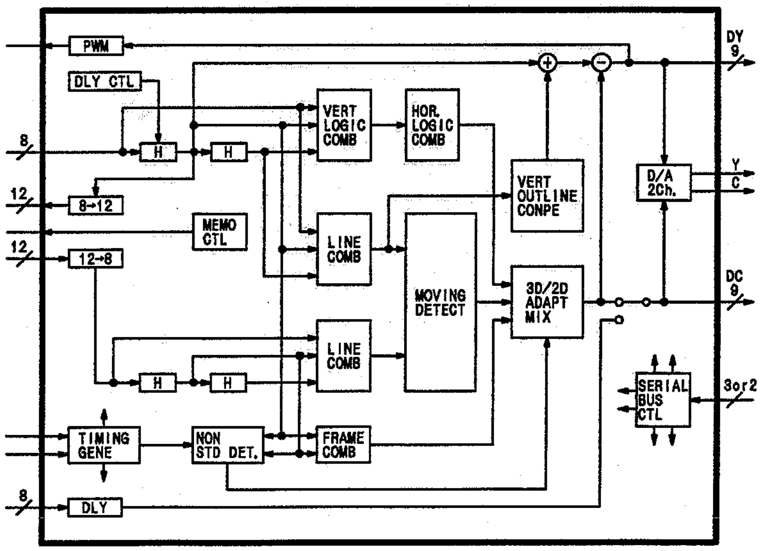


(TOP VIEW)
CLK ①
STB ②
DATA ③
PCL ④
VDD ⑤
OSC OUT ⑥
OSC IN ⑦
GND ⑧
⑯ H SYNC
⑮ V SYNC
⑭ VBLK2
⑬ VC2
⑫ VBLK1
⑪ VC1
⑩ NC
⑨ CK OUT

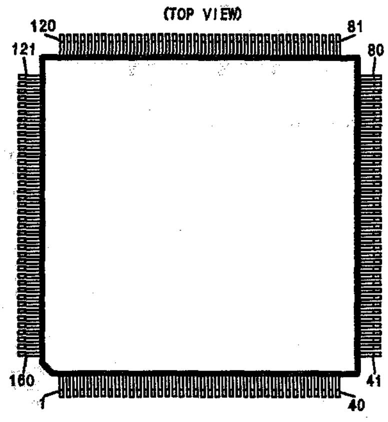
μPD6486GF
(NTSC Y/C SEPARATION)


(TOP VIEW)
ANALOG I/F
BVCO
DVDD
KIL
CLPI
VDI
AGND
IOY
AVDD
COMP
VREF
IREF
AVDD
IOC
AGND
HSS
HREF
DGND
HPD
DVDD
HVCO
100
95
90
85
81
80
1
5
10
15
20
25
30
31
35
40
45
50
51
55
60
65
70
75
DGND
CS
7
6
5
4
3
2
1
0
ADCK
CLPO
VOH
7
6
5
4
3
2
1
0
FMO
11
10
9
8
7
6
5
4
FMI11
FMI10
DGND
DVDD
9
8
7
6
5
4
FMI
MRSB
MRS
MWCK
MRCK
3
2
1
0
FMO
3
2
1
0
FMI
DVDD
DGND
SEP
VTR
DY
8
7
6
5
4
3
2
1
0
DC
8
7
6
5
4
3
2
1
0
TEST2
TEST1
μPD6485
SID
SIK
SIBI
SIBO
μPD6486
SDA
SCL
SLA0
SLA1
LINE
BPF
DGND
: INPUT
: OUTPUT
: POWER

BLOCK DIAGRAM


PWM
DLY CTL
8
H
H
VERT LOGIC COMB
HOR. LOGIC COMB
12
8→12
MEMO CTL
12
12→8
LINE COMB
MOVING DETECT
VERT OUTLINE CONPE
3D/2D ADAPT MIX
D/A 2Ch.
DY
9
Y
C
DC
9
H
H
LINE COMB
SERIAL BUS CTL
3or2
TIMING GENE
NON STD DET.
FRAME COMB
8
DLY

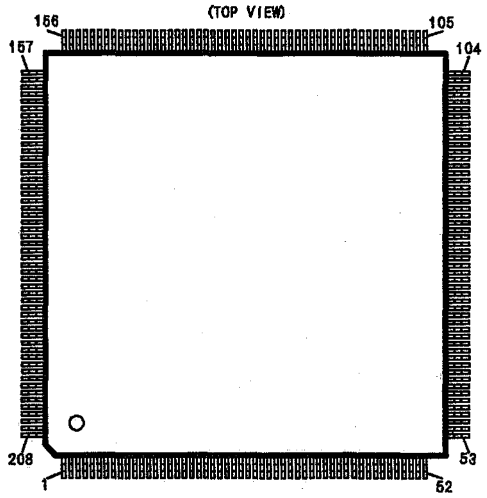
µPD65845G039



PIN ALIGNMENT

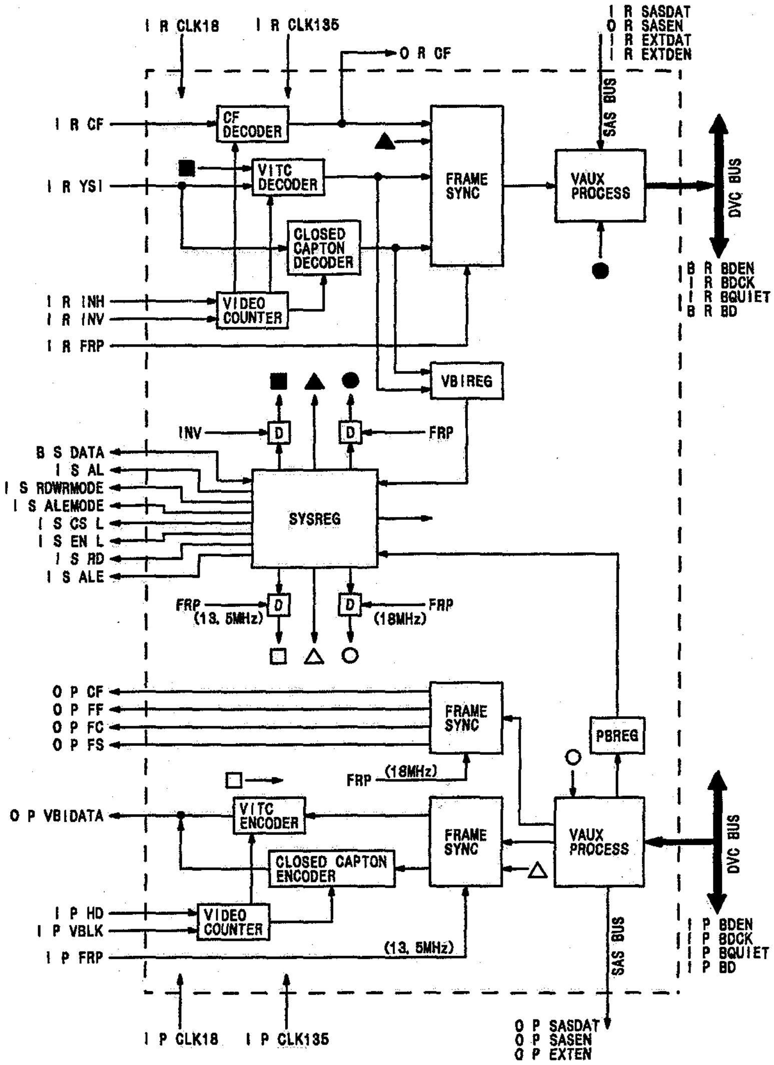
PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	VDD	41	GND	81	VDD	121	GND
2	FRP R	42	GND	82	I EEDAT	122	GND
3	SEQN0	43	CF0	83	HSE	123	FE CTRL0
4	SEQN1	44	CF1	84	CTLA	124	FE CTRL1
5	SEQN2	45	CF2	85	CTLB	125	CLK837
6	SEQN3	46	DLYDAT0	86	FRP P	126	AL0
7	GND	47	DLYDAT1	87	FIFORST	127	AL1
8	FRMSTRT	48	DLYDAT2	88	VDD	128	AL2
9	CFLOAD	49	DLYDAT3	89	FIFOCLK	129	AL3
10	FEFRMST	50	DLYDAT4	90	O EEDAT	130	AL4
11	GND	51	CLK18	91	O EDAT70	131	AL5
12	RECSTRT	52	TRANSIT	92	O EDAT71	132	GND
13	SBSTR	53	GND	93	O EDAT72	133	DATA0
14	TST SEQ0	54	RRST	94	GND	134	DATA1
15	TST SEQ1	55	WRST	95	GND	135	DATA2
16	TST SEQ2	56	SBSTP	96	O EDAT73	136	DATA3
17	TST SEQ3	57	DEDP0	97	O EDAT74	137	DATA4
18	SEQNEN	58	DEDP1	98	O EDAT75	138	DATA5
19	SEQNEN2	59	DEDP2	99	O EDAT76	139	DATA6
20	VDD	60	DEDP3	100	VDD	140	DATA7
21	GND	61	GND	101	GND	141	GND
22	OUT SEQ0	62	CLK8	102	PBCLK	142	CS N
23	OUT SEQ1	63	PBDAT1B	103	PBDATA	143	READ
24	OUT SEQ2	64	PBDAT8B0	104	PBDATA80	144	WRITE
25	OUT SEQ3	65	PBDAT8B1	105	PBDATA81	145	U ALMODE
26	GND	66	PBDAT8B2	106	PBDATA82	146	U RWMODE
27	SBSTP R	67	PBDAT8B3	107	VDD	147	ALE
28	DEDP R0	68	PBDAT8B4	108	PBDATA83	148	VDD
29	DEDP R1	69	PBDAT8B5	109	PBDATA84	149	TEST SW
30	DEDP R2	70	PBDAT8B6	110	PBDATA85	150	RST SW
31	DEDP R3	71	PBDAT8B7	111	PBDATA86	151	SBE
32	HID R	72	I EDAT70	112	PBDATA87	152	HIZ
33	GND	73	I EDAT71	113	GND	153	TCK
34	SBSTP P	74	I EDAT72	114	ATFCLK	154	TRS
35	DEDP P0	75	I EDAT73	115	I REC L	155	TMS
36	DEDP P1	76	I EDAT74	116	I SPA	156	TDI
37	DEDP P2	77	I EDAT75	117	TST DFRP	157	TDO
38	DEDP P3	78	I EDAT76	118	ATFCLK5	158	VDD
39	HID P	79	GND	119	GND	159	GND
40	VDD	80	GND	120	VDD	160	GND

μPD65868D022
(GATE ARRAY)



PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	GND	53	VDD	105	GND	157	VDD
2	GND	54	BTL0	106	GND	158	RVO
3	RCF0	55	BTL1	107	PSD0	159	RVZ
4	RCF1	56	BTL2	108	PSD1	160	RVW
5	RCV	57	GND	109	PSD2	161	RA1Z
6	INH	58	BTL3	110	PSD3	162	RA1W
7	INV	59	BTL4	111	PSE	163	RA2Z
8	RFP	60	BTL5	112	PEE	164	RA2W
9	N. C	61	BTL6	113	VDD	165	GND
10	N. C	62	GND	114	GND	166	VDD
11	SRM	63	GND	115	PBD0	167	RSD0
12	SAM	64	BTL7	116	PBD1	168	RSD1
13	SCS	65	BTL8	117	PBD2	169	RSD2
14	SRD	66	BTL9	118	PBD3	170	RSD3
15	SEN	67	VDD	119	PBD4	171	RSE
16	SAE	68	BFRM	120	PBD5	172	N. C
17	SD0	69	APF	121	PBD6	173	TCF0
18	SD1	70	ALP	122	PBD7	174	TCF1
19	SD2	71	ASE	123	PBE	175	TCV
20	GND	72	ALV	124	PBC	176	VARE
21	SD3	73	ATE	125	PBQ	177	VBRE
22	SD4	74	AAD0	126	PFP	178	N. C
23	SD5	75	AAD1	127	TCK	179	N. C
24	SD6	76	AAD2	128	TRS	180	GND
25	SD7	77	PIC	129	TMS	181	RSC
26	GND	78	VDD	130	VDD	182	GND
27	VDD	79	GND	131	GND	183	VDD
28	SAL0	80	PSC	132	TDI	184	RIC
29	SAL1	81	GND	133	TDO	185	GND
30	SAL2	82	N. C	134	HIZ	186	BCD0
31	SAL3	83	AAD3	135	RST	187	BCD1
32	SAL4	84	AAD4	136	GND	188	BCD2
33	SAL5	85	AAD5	137	RBE	189	BCD3
34	PVD0	86	AAD6	138	RBC	190	BCD4
35	PVD1	87	AAD7	139	RBQ	191	BCD5
36	PVD2	88	AAD8	140	RBD0	192	BCD6
37	PVD3	89	AAD9	141	RBD1	193	BCD7
38	PVD4	90	AAD10	142	RBD2	194	VDD
39	PVD5	91	AAD11	143	RBD3	195	GND
40	PVD6	92	AAD12	144	RBD4	196	BTCE
41	PVD7	93	AAD13	145	RBD5	197	BCDR
42	N. C	94	PCF0	146	RBD6	198	BTDR
43	N. C	95	PCF1	147	RBD7	199	RYI0
44	N. C	96	PCN	148	GND	200	RYI1
45	PVE	97	PCE	149	TST1	201	RYI2
46	PDE	98	PFF	150	RXD0	202	RYI3
47	PHD	99	PFS	151	RXD1	203	RYI4
48	PVB	100	PFC	152	RXD2	204	RYI5
49	VAPE	101	PFV	153	RXD3	205	RYI6
50	VBPE	102	TST2	154	RXE	206	RYI7
51	GND	103	TST3	155	GND	207	N. C
52	GND	104	VDD	156	GND	208	VDD

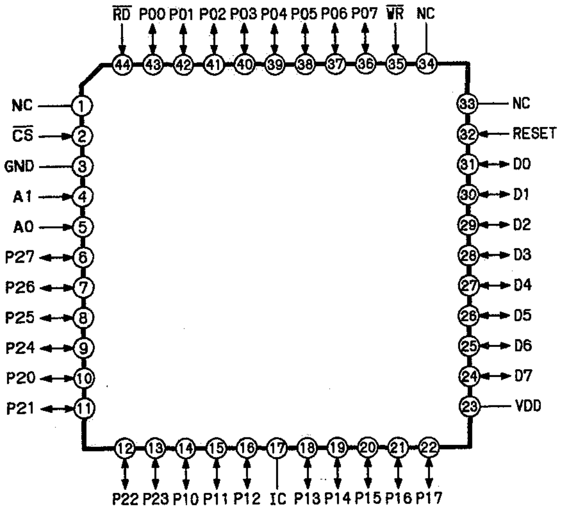
BLOCK DIAGRAM

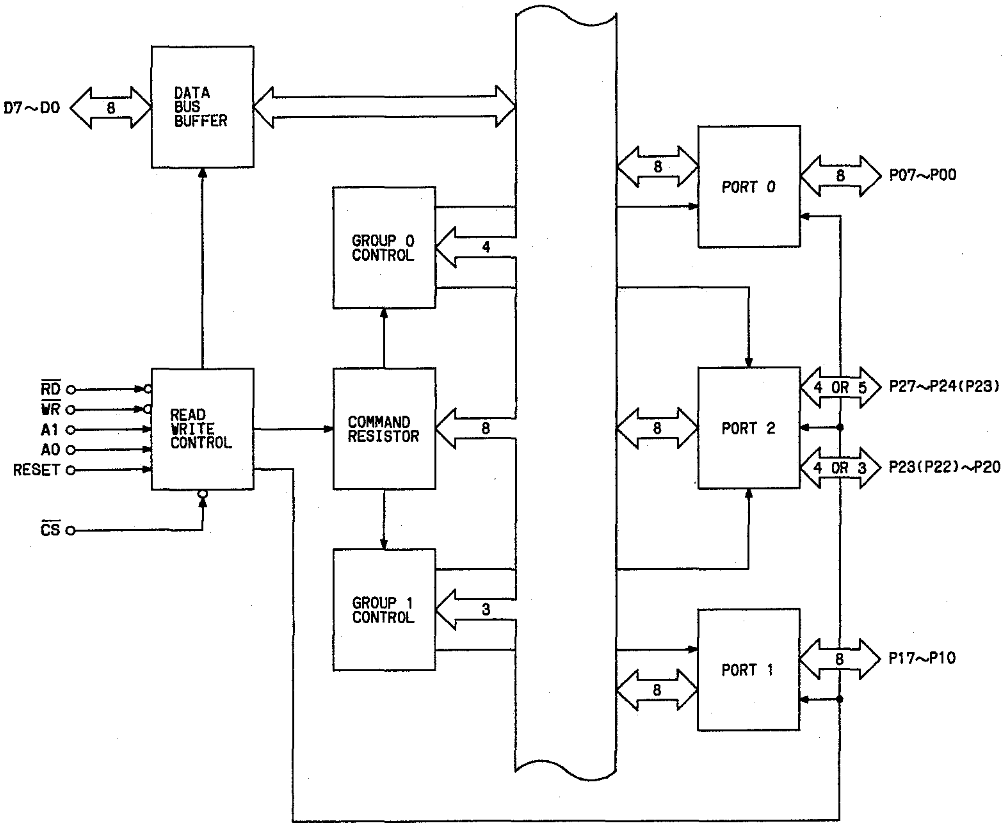


I R CLK18
I R CLK135
O R CF
I R SASDAT
O R SASEN
I R EXTDAT
I R EXTDEN
SAS BUS
I R CF
CF DECODER
VITC DECODER
I R YSI
CLOSED CAPTON DECODER
FRAME SYNC
VAUX PROCESS
DVC BUS
B R BDEN
I R BDCK
I R BQUIET
B R BD
I R INH
I R INV
VIDEO COUNTER
I R FRP
VBIREG
INV
D
FRP
B S DATA
I S AL
I S RDWRMODE
I S ALEMODE
I S CS L
I S EN L
I S RD
I S ALE
SYSREG
FRP (13. 5MHz)
(18MHz) FRP
O P CF
O P FF
O P FC
O P FS
FRAME SYNC
PBREG
FRP (18MHz)
O P VBIDATA
VITC ENCODER
CLOSED CAPTON ENCODER
FRAME SYNC
VAUX PROCESS
DVC BUS
I P HD
I P VBLK
VIDEO COUNTER
I P FRP
(13. 5MHz)
SAS BUS
I P BDEN
I P BDCK
I P BQUIET
I P BD
I P CLK18
I P CLK135
O P SASDAT
O P SASEN
O P EXTEN

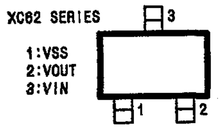
UPD71055G

(PARALLEL INTERFACE UNIT)

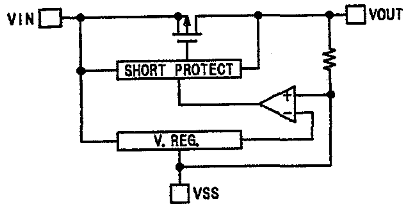

RD
P00
P01
P02
P03
P04
P05
P06
P07
WR
NC
44
43
42
41
40
39
38
37
36
35
34
NC 1
CS 2
GND 3
A1 4
A0 5
P27 6
P26 7
P25 8
P24 9
P20 10
P21 11
33 NC
32 RESET
31 D0
30 D1
29 D2
28 D3
27 D4
26 D5
25 D6
24 D7
23 VDD
12
13
14
15
16
17
18
19
20
21
22
P22
P23
P10
P11
P12
IC
P13
P14
P15
P16
P17


D7～D0
8
DATA BUS BUFFER
GROUP 0 CONTROL
4
PORT 0
8
8
P07～P00
RD
WR
A1
A0
RESET
CS
READ WRITE CONTROL
COMMAND RESISTOR
8
PORT 2
8
4 OR 5
P27～P24(P23)
4 OR 3
P23(P22)～P20
GROUP 1 CONTROL
3
PORT 1
8
8
P17～P10

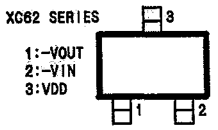
XC62APXX02M
(VOLTAGE REGULATOR)


XC62 SERIES
1:VSS
2:VOUT
3:VIN
1
2
3

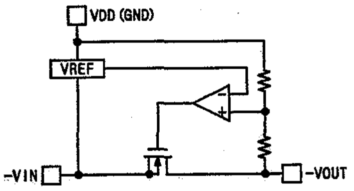
BLOCK DIAGRAM


VIN
VOUT
SHORT PROTECT
+
-
V. REG.
VSS

XC62DNXX02M
(VOLTAGE REGULATOR)

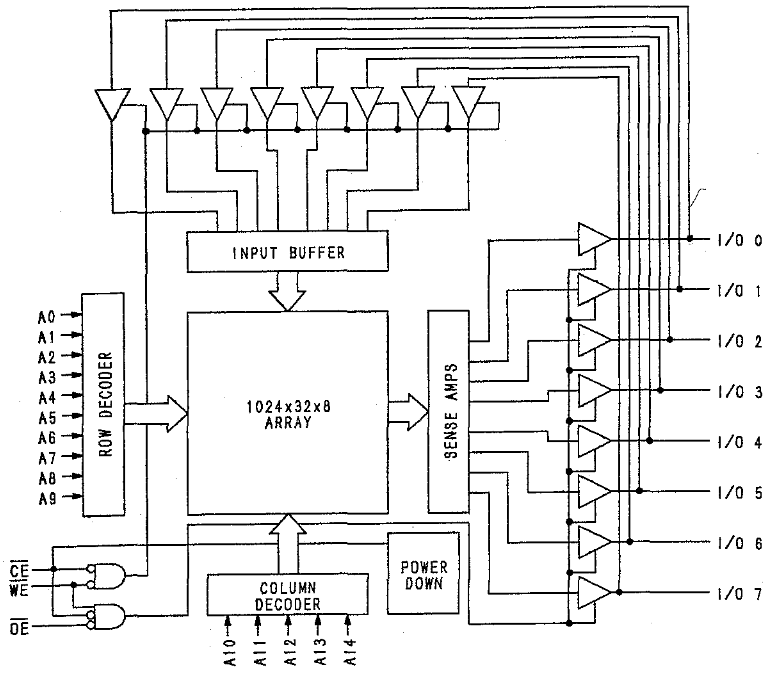

XC62 SERIES
1:-VOUT
2:-VIN
3:VDD
1
2
3

BLOCK DAIGRAM


VDD (GND)
VREF
+
-
-VIN
-VOUT

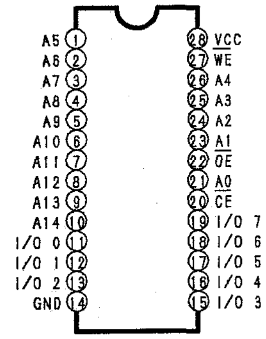
Y7C19935VC
(32Kx8 STATIC RAM)

LOGIC BLOCK DIAGRAM

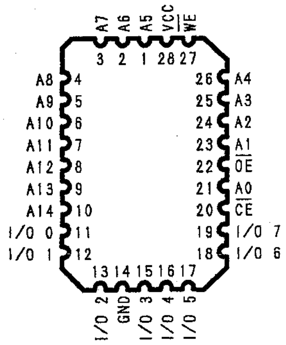

INPUT BUFFER
1024x32x8
ARRAY
ROW DECODER
SENSE AMPS
COLUMN DECODER
POWER DOWN
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
CE
WE
OE
I/O 0
I/O 1
I/O 2
I/O 3
I/O 4
I/O 5
I/O 6
I/O 7

PIN CONFIGURATIONS

DIP/SOJ
(TOP VIEW)

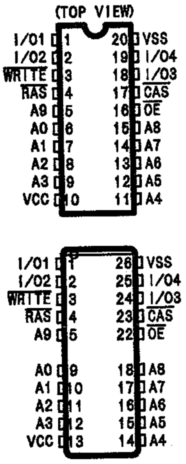

A5 1
A6 2
A7 3
A8 4
A9 5
A10 6
A11 7
A12 8
A13 9
A14 10
I/O 0 11
I/O 1 12
I/O 2 13
GND 14
28 VCC
27 WE
26 A4
25 A3
24 A2
23 A1
22 OE
21 A0
20 CE
19 I/O 7
18 I/O 6
17 I/O 5
16 I/O 4
15 I/O 3

LCC
(TOP VIEW)

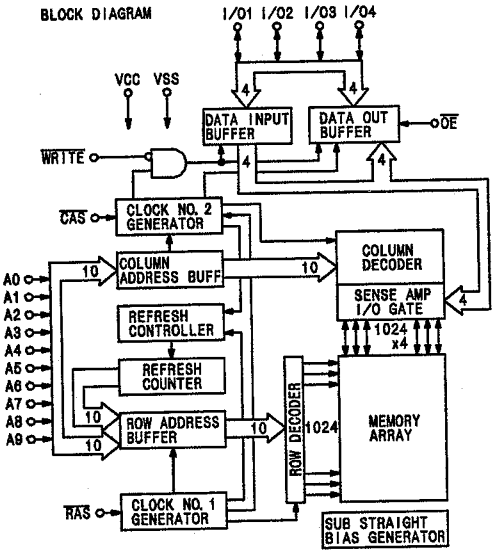

A7
A6
A5
VCC
WE
3 2 1 28 27
A8 4
A9 5
A10 6
A11 7
A12 8
A13 9
A14 10
I/O 0 11
I/O 1 12
26 A4
25 A3
24 A2
23 A1
22 OE
21 A0
20 CE
19 I/O 7
18 I/O 6
13 14 15 16 17
I/O 2
GND
I/O 3
I/O 4
I/O 5

T51440ASJ7EL
(4M 1,048,576 WORDSx4BITS D RAM)

(TOP VIEW)


I/01 1
I/02 2
WRITE 3
RAS 4
A9 5
A0 6
A1 7
A2 8
A3 9
VCC 10
20 VSS
19 I/04
18 I/03
17 CAS
16 OE
15 A8
14 A7
13 A6
12 A5
11 A4
I/01 1
I/02 2
WRITE 3
RAS 4
A9 5
A0 9
A1 10
A2 11
A3 12
VCC 13
26 VSS
25 I/04
24 I/03
23 CAS
22 OE
18 A8
17 A7
16 A6
15 A5
14 A4

BLOCK DIAGRAM


I/01 I/02 I/03 I/04
VCC VSS
DATA INPUT BUFFER
DATA OUT BUFFER
OE
WRITE
CAS
CLOCK NO. 2 GENERATOR
COLUMN ADDRESS BUFF
COLUMN DECODER
SENSE AMP I/O GATE
REFRESH CONTROLLER
REFRESH COUNTER
ROW ADDRESS BUFFER
ROW DECODER
MEMORY ARRAY
1024 x4
1024
10
4
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
RAS
CLOCK NO. 1 GENERATOR
SUB STRAIGHT BIAS GENERATOR

V 17729

Order No. VSD9611SB617

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Test Audio Level

Please use this supplement together with the Service Manual as follows :			
Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	17	VSD9606M501A/B	I6TKA0001

Board : AUDIO LCD (VEP04522B)

Test Audio Level may be out of specification. To improve the Test Audio Level, resistor R4051 is changed from 47KΩ to 22KΩ on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
R4051	ERJ3GEYJ473	ERJ3GEYJ223	M. RESISTOR CH 1/16W 22K	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
R4051	2-71	C-8 (2/9)	3-16	F-1 (F)

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V17729

Order No. VSD9611SB618

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Reduction of High Power Consumption

Please use this supplement together with the Service Manual as follows :			
Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	18	VSD9606M501A/B	I6TKA0001

Board : Power (VEP01643A)

Symptom : Power consumption may be couple of watts higher than specification.

Cause : When the chattering may occur at Power Supply (AC100V), regulator IC voltage is over specification . It results in Regulator IC break.

Remedy : To prevent it, the over-voltage protect circuit is added. The following modification is performed.

1). Change diode D1013 from MA8062-M to MA8100-M on the foil side.
2). Add a diode D1020 (MA142WK) to the pattern on the foil side.
3). Add a transistors Q1025 (2SD1820A-R) and Q1043 (UN5111) to the pattern on the foil side.
4). Add a transistor QR1003 (UN5211) to the pattern on the foil side.
5). Add a resistors (1/16W, 10KΩ) R1084, R1152 and R1156 to the pattern on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
D1013	MA8062-M	MA8100-M	DIODE	1	
D1020	—	MA142WK	DIODE	0→1	
Q1025	—	2SD1820A-R	TRANSISTOR	0→1	
Q1043	—	UN5111	TRANSISTOR	0→1	
QR1003	—	UN5211	TRANSISTOR-RESISTOR	0→1	
R1084	—	ERJ3GEYJ103	M. RESISTOR CH 1/16W 10K	0→1	
R1152	—	ERJ3GEYJ103	M. RESISTOR CH 1/16W 10K	0→1	
R1156	—	ERJ3GEYJ103	M. RESISTOR CH 1/16W 10K	0→1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
D1013	2-68	B-11 (1/2)	3-14	B-2 (F)
D1020	2-68	F-10 (1/2)	3-14	C-2 (F)
Q1025	2-68	D-10 (1/2)	3-14	B-2 (F)
Q1043	2-68	E-10 (1/2)	3-14	C-2 (F)
QR1003	2-68	C-11 (1/2)	3-14	D-1 (F)
R1084	2-68	D-10 (1/2)	3-14	B-2 (F)
R1152	2-68	D-10 (1/2)	3-14	B-2 (F)
R1156	2-68	F-10 (1/2)	3-14	C-2 (F)

10031TE4627

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V 17729

Order No. VSD9611SB619

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Reduction of White Vertical Noise

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	19	VSD9606M501A/B	K6TKA0001

Board : EVF Video (VEP29022A)

Symptom : White vertical noise may appear on the left side of the monitor.

Cause : As the FET drive circuit is overdriven, FET rising is delayed. It results in vertical noise.

Remedy : To prevent it, resistor R9015 is changed from 2.2KΩ to 9.1KΩ.

Part Number

Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
R9015	ERJ3GEYJ222	ERJ3GEYJ912	M. RESISTOR CH 1/16W 9.1K	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
R9015	2-86	B-8	---	---

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VA7729

Order No. VSD9611SB620

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of V Synchronization

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	20	VSD9606M501A/B	K6TKA0001

Board : EVF Video (VEP29022A)

Symptom : Vertical sync may not be synchronized.

Cause : As V Free Run frequency depends on +B voltage, V Free Run adjustment value at the tool is changed with connected AJ-D700.

Remedy : To prevent it, V Free Run frequency is changed to center position. The following modification is performed.

1). Delete resistor R9017 (1/10W, 10KΩ) from the component side as shown in figures 1 and 2.
2). Add a resistor R9096 (1/4W, 8.2KΩ) between pin #5 of IC9002 and R9017 after the removing portion on the component side as shown in figures 1 and 2.
3). V Free Run frequency is changed from 43Hz ± 1Hz to 46Hz ± 0.5Hz as shown below.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
R9017 R9096	VRE0034E103 ---	--- ER0S2CKF8201	M. RESISTOR CH 1/10W 10K M. RESISTOR 1/4W 8.2K	1→0 0→1	

10-2. V Free Run Adjustment

BOARD	H Def	
SPEC	52 ± 1Hz (NTSC) →	**54 ± 0.5Hz (NTSC)**
	43 ± 1Hz (PAL) →	**46 ± 0.5Hz (PAL)**
TEST	TP9002	
ADJUST	VR9002	
M.EQ	Frequency Counter	

Changed

1. Adjust the **VR9002** so that the frequency at the **TP9002** is within specification without input signal.

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EVF Video Schematic Diagram

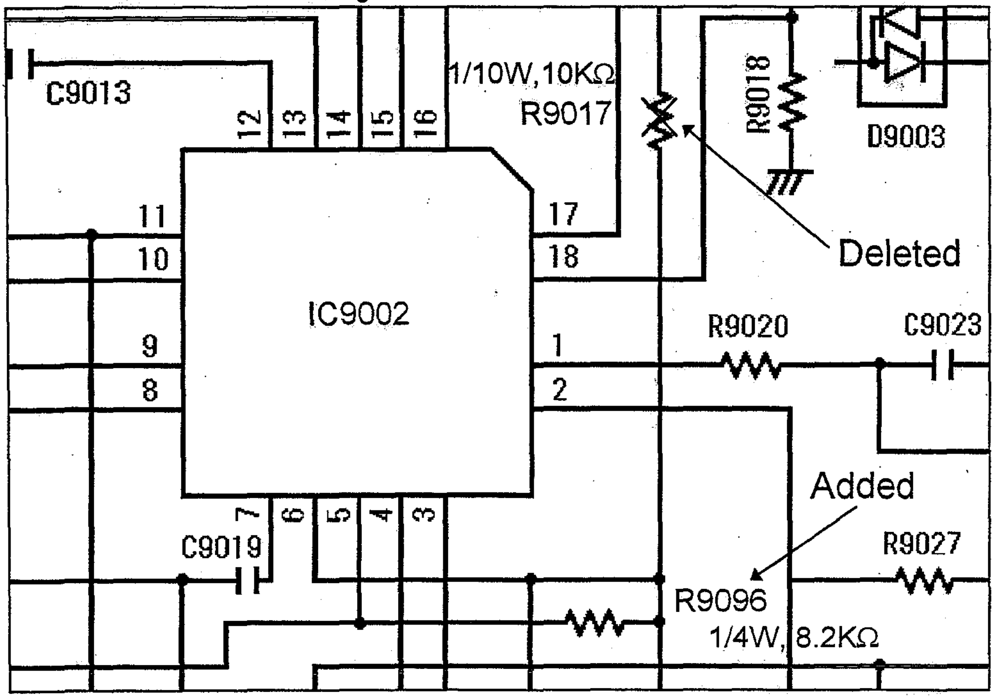
C9013
12
13
14
15
16
1/10W,10KΩ
R9017
R9018
D9003
11
10
17
18
Deleted
IC9002
R9020
C9023
9
8
1
2
Added
7
6
5
4
3
C9019
R9027
R9096
1/4W, 8.2KΩ

Fig. 1 Page 2-86 (D-6)

EVF Video P.C.Board (VEP29022A)

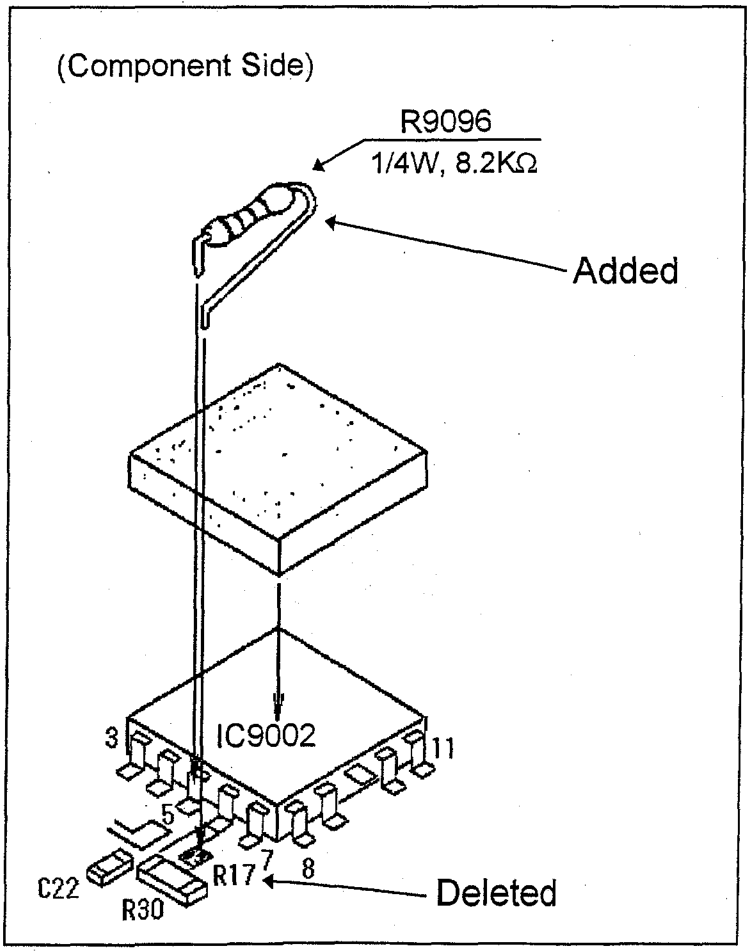
(Component Side)
R9096
1/4W, 8.2KΩ
Added
IC9002
3
11
5
7
8
C22
R30
R17
Deleted

Fig. 2

VA7729

Order No. VSD9611SB621

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Change of ROM Type

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	21	VSD9606M501A/B	K6TKA0001

Board : Video Main (VEP03B96B)

To improve manufacturing productivity, IC501 is changed from one time memory type PROM to masking type PROM.

Part Number

Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC501	VSI2079A	M37709M4L161	SBC PROM	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC501	2-65	D-5 (5/7)	3-12	B-2 (F)

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VA7728

Order No. VSD9611SB622

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Burst Level VR Variable Range

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	22	VSD9606M501A/B	J6TKA0001

Board : Camera Encoder (VEP23276B)

Symptom : Burst level cannot be adjusted.

Cause : As the burst ratio conversion output signal is input to the Encoder IC without through the buffer, burst level is decreased.

Remedy : To prevent it, volume VR3007 is changed on the component side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
VR3007	EVM7JSX30B53	EVM7JGA00B23	VOLUME	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
VR3007	2-26	G-5 (3/7)	3-7	A-2 (C)

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VA7729

Order No. VSD9612SB623

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of LSI IC

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	23	VSD9606M501A/B	L6TKA0001

Board : Camera DSP (VEP23275A)

To have a timing margin of LSI IC, IC3102 is changed from VY06633 to VY06633A on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC3102	VY06633	VY06633A	IC	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC3102	2-21	D-9 (2/4)	3-6	B-2 (F)

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V17729

Order No. VSD9612SB624

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Audio Distortion

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	24	VSD9606M501A/B	L6TKA0001

Board : Video Main (VEP03B96B)

Symptom : Audio distortion rate may be big.

Cause : Audio clock jitter may increase due to the noise from the power supply (3.0V) of Audio VCO circuit.

Remedy : To prevent it, the Audio VCO circuit is improved. The following modification is performed.

1). Add a capacitor C150 (25V/0.1µF) to the pattern on the component side.
2). Add a capacitor C151 (25V/0.1µF) to the pattern on the component side.
3). Add a capacitor C152 (6.3V/47µF) to the pattern on the component side.
4). Add an IC IC35 to the pattern on the component side.
5). Delete coils L12 and L23 from the component side.
6). Cut the foil of terminal O of IC35 on the component side as shown in figures 1 and 2.
7). Connect a jumper wire between terminal O of IC35 and land of L23 on the component side as shown in figures 1 and 2.
8). Connect a jumper wire between plus side of C41 and plus side of C152 on the component side as shown in figures 1 and 2.

Part Number

Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C150, 151	—	ECUX1E104ZFV	C. CAPACITOR CH 25V 0.1U	0→2	
C152	—	ECEV0GV470Q	E. CAPACITOR CH 6.3V 47U	0→1	
IC35	—	XC62AP3002P	IC	0→1	
L12	—	VLQ0464K6R8	COIL 6.8UH	1→0	
L23	—	VLQ0464K6R8	COIL 6.8UH	1→0	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C150	2-62	B-2 (2/7)	3-12	A-1 (C)
C151	2-62	B-2 (2/7)	3-12	A-1 (C)
C152	2-62	B-2 (2/7)	3-12	A-1 (C)
IC35	2-62	B-2 (2/7)	3-12	A-1 (C)
L12	2-62	D-5 (2/7)	3-12	B-1 (C)
L23	2-62	E-8 (2/7)	3-12	B-1 (C)

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Video Main (2/7) Schematic Diagram

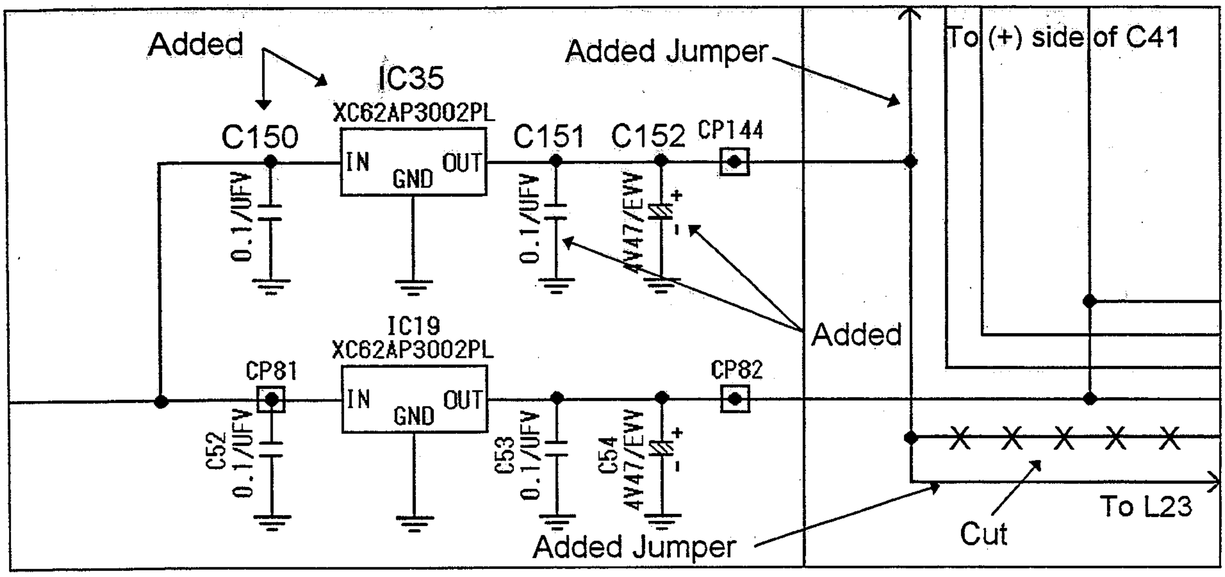
Added
IC35
XC62AP3002PL
Added Jumper
To (+) side of C41
C150
IN
GND
OUT
C151
C152
CP144
0.1/UFV
0.1/UFV
4V47/EVV
Added
IC19
XC62AP3002PL
CP81
CP82
C52
0.1/UFV
C53
0.1/UFV
C54
4V47/EVV
Added Jumper
Cut
To L23

Fig. 1 Page 2-7

Video Main P.C.Board (VEP03B96B)

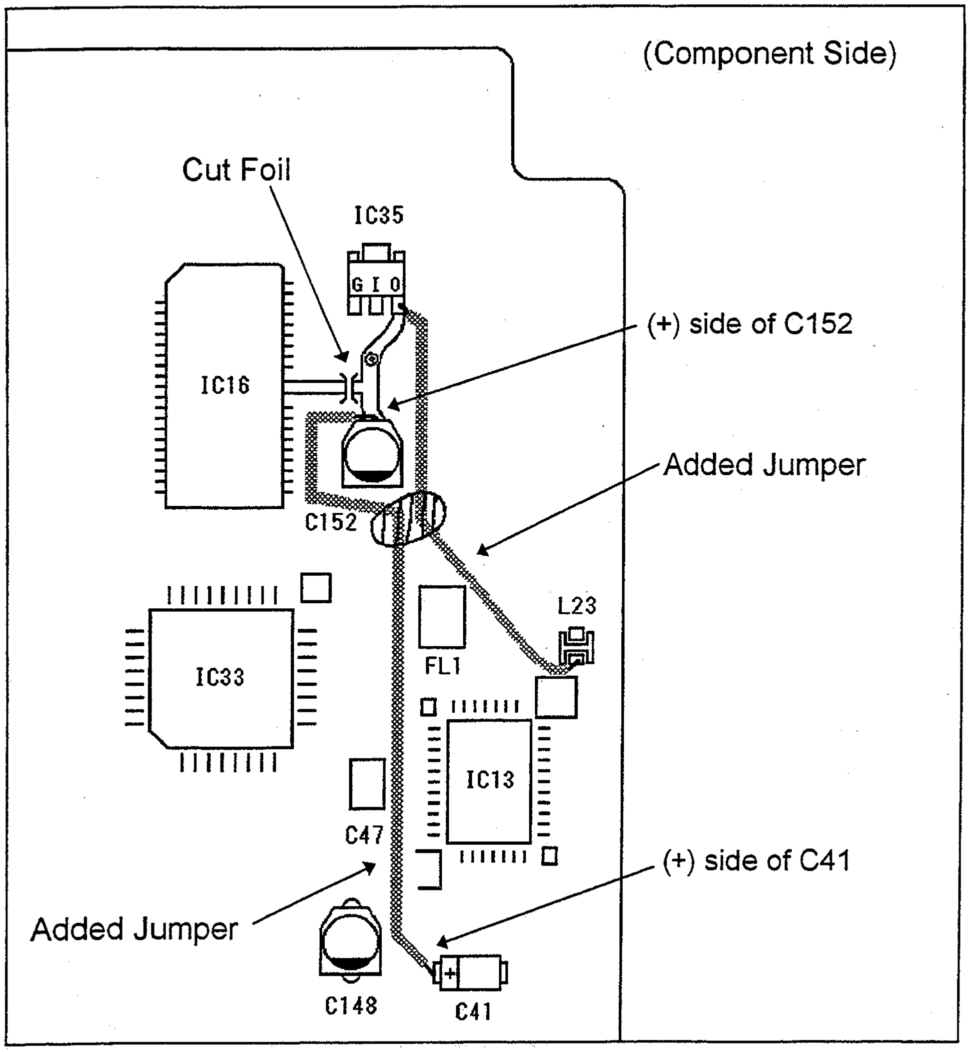
(Component Side)
Cut Foil
IC35
G I O
(+) side of C152
IC16
C152
Added Jumper
L23
FL1
IC33
IC13
C47
(+) side of C41
Added Jumper
C148
C41

Fig. 2 Page 3-12

VA7728/VA7729
✓

Order No. VSD9701SB625

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Time Code Back Up

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	25	VSD9606M501A/B	A7TKA0001

Board : Audio LCD (VEP04522B)

Symptom : 1). Time code back up battery may last about 6 month.
2). Time code count may be shifted during TC Free Run mode when the power is turned OFF.

Cause : 1). Due to the excess process of LCD micro-computer during power save mode.
2). Due to the TC back up process malfunction of LCD micro-computer.

Remedy : To improve the above matters, the following modification is performed.

*** The unit produced before Serial Number L6TKA******
LCD micro-computer IC6501 is changed from UPD75316BE58 to UPD75316BE83

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC6501	UPD75316BE58	UPD75316BE83	IC	1	

*** The unit produced after Serial Number L6TKA******
LCD micro-computer IC6501 is changed from VSI2449 to UPD75316BE83.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC6501	VSI2449	UPD75316BE83	IC	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC6501	2-76	C~D-3~4 (7/9)	3-17	F-1 (F)

< Modification Method >

1. Loosen the 4 screws (A) and remove the Right Side Panel.
2. Loosen the 5 screws (B) and remove the insulation sheet on the Audio LCD Board.
3. Replace the Back Up battery (CR2032) on the Backup Battery P.C.Board to new one.

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4. Replace IC6501 on the Audio LCD P.C.Board from UPD75316BE58 or VSI2449 to UPD75316BE83 as follows;
   1). Unsolder the solder of the IC6501. (UPD75316BE58 or VSI2449)
   2). Float all legs of IC6501 warming the legs.
   3). Confirm that all legs of IC6501 are completely come off from the Board.
   4). Attach the bit of minus driver which wrapped up with the cellophane adhesive tape to the one corner of the IC, and hit the driver with the light hammer.
   5). Repeat this step to the other corners and then remove the IC.

   * Note * Be careful that do not damage the foil under the IC6501 due to the strong adhesive when remove IC.

   6). Install new IC6501 (UPD75316BE83).
5. After above modification, the following items are confirmed.
   1). Display Tube Confirmation
      a). Confirm that the Display Tube is indicated during Power ON.
      b). Confirm that the Display Tube is observed that there is no display missing.
   2). LCD Light SW Confirmation
      a). Confirm that the LCD light is turned ON during LCD light SW ON.
   3). MENU SW Confirmation
      a). Confirm that the Menu in the EVF is indicated when the Menu SW is turned ON.
   4). Color Bar/Camera Switching Confirmation
      a). When the Color Bar/Camera SW is switched to BARS, confirm that the color bar is indicated in the EVF and the TEST signal of Audio is output. (AUDIO IN SW is Front side)
   5). CTL/TC Switching Confirmation
      a). Confirm that the characters of DF and TCG are indicated in the Display Tube when the CTL/TC SW is switched to TC side.
      b). Confirm that the DF and TCG display are disappeared when the CTL/TC SW is switched to CTL side.
   6). TC RESET Confirmation
      a). Confirm that the CTL/TC SW is turned to TC side and TCG SW is turned to F-RUN.
      b). Confirm that the TCG SW is turned to SET when the time code is proceeded about 10 counts.
      c). Confirm that the hour position of time code count is stopped after flashing and then the time code count is reset when press the RESET button.
   7). SUPER IRIS Confirmation
      a). Confirm that the ON/OFF of Super Iris is indicated in the EVF pressing the Super Iris button.
   8). MIC Input Front/Rear Confirmation
      a). Confirm on the LCD Display that Audio sound is input from the MIC IN when the MIC is connected setting the AUDIO IN to FRONT MIC side.
      b). Confirm on the LCD Display that Audio sound is input from the MIC IN when the MIC is connected to the AUDIO IN on the rear side setting the AUDIO IN to REAR MIC side. (Both CH1 and CH2)
         * Note * Be careful the monitor setting during REAR MIC confirmation.
   9). POWER SW Confirmation
      a). Confirm that the Power Supply is functioned normally when the Power SW is turned ON/OFF repeatedly.
      b). Confirm that the Display Tube and LCD Light are indicated normally when the Power is turned ON.
   10). RECRUN, SET, FREE and HOLD Confirmation
      a). Confirm that the TCG SW is set to R-RUN when the CTL/TC SW is set to TC side after inserting the tape.
      b). Confirm that the TC count is proceeded at only REC mode and stop it at REC/PAUSE mode.
      c). Confirm that the Hour position of time code count is flashed when the TCG SW is turned to SET side.
      d). Confirm that the TC count is proceeded with no relation to mode setting when the TCG SW is turned to FREE side.
      e). Confirm that the TC count is held when the HOLD button is pressed proceeding the Time Code count.
   11). REAR MIC Jitter Noise Confirmation
      a). Confirm that the AUDIO IN is set to REAR MIC side with no audio input.
      b). Confirm the audio sound on the Headphone OUT that there is no jitter noise.
         * Note * When the jitter noise may appear, confirm the flat cable on the LCD panel again.
   12). Warning Lamp Confirmation
      a). Confirm that the no recorded portion of the tape is played back.
      b). Confirm that the Warning Lamp is flashed after play back it for a while.
         * Note * Confirm the tape remaining display during Playback mode.

13). MENU Initial Setting

- a). Confirm that the MENU is indicated in the EVF after turn the MENU SW ON pressing the [SHIFT], [+], [-] and [PAGE] buttons simultaneously.
- b). Confirm that the MENU screen is set to DESIGN pressing the PAGE button.
- c). Confirm that the cursor “→“ is set to “MENU ALL INIT” pressing the SHIFT button.
- d). Confirm that the “INIT OK” is indicated pressing the [+] or [-] button.

14). Initial SW Setting is as follows. (Factory Setting)

SW Name	Setting	Factory Setting
LIGHT	ON/OFF	OFF
DISPLAY	CTL/TC/UB	CTL
MONITOR	CH1/CH1·2/CH2	CH1·2
	ST/MIX	ST
RET VIDEO	INT/EXT	INT
AUDIO IN	CH1 (FRONT MIC/REAR MIC/REAR LINE)	FRONT (MIC)
	CH2 (FRONT MIC/REAR MIC/REAR LINE)	FRONT (MIC)
AUDIO SELECT	CH1 (AUTO/MAN)	AUTO
	CH2 (AUTO/MAN)	AUTO
TCG	F-RUN/SET/R-RUN	R-RUN
MENU	SET/OFF	OFF
POWER	ON/OFF	OFF
VTR	SAVE/STBY	STBY
GAIN	H/M/L	L
OUTPUT	BARS. AUTO KNEE OFF/ CAM. AUTO KNEE OFF/ CAM. AUTO KNEE ON	CAM. AUTO KNEE ON
WHITE BAL	PRST/A/B	B
SHUTTER	OFF/ON/SEL	OFF
AUTO W/B BAL	AWB/ABB	CENTER
BACK TALLY	ON/OFF	OFF
ANTON BRACKET	LIGHT CONTROL ON/OFF	OFF
ALARM	ALARM	CENTER
MONITOR	MONITOR	CENTER
AUDIO LEVEL CH1	AUDIO LEVEL CH1	CENTER
AUDIO LEVEL CH2	AUDIO LEVEL CH2	CENTER
AUDIO CH1	AUDIO CH1	MAX
FILTER	FILTER	1

✓ VA928 + VA929

Order No. VSD9705SB641

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Reduction of Block Error Noise

Please use this supplement together with the Service Manual as follows :			
Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	41	VSD9606M501A/B	C7TKA0001

Board : Video Main (VEP03B96B)

Symptom : Block Error noise may appear on the picture.

Cause : Due to the IC bug.

Remedy : To reduce the Block Error noise, IC3 is changed from MN67371F to MN673711 on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC3	MN67371F	MN673711	IC	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC3	2-61	B~C-1~3 (1/7)	3-12	C-2 (F)

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[illegible] + [illegible]

Order No. VSD9705SB643-1

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of PCM Audio Noise (Audio VCO)

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	43	VSD9606M501A/B	D7TKA0001

Board : VTR System Control (VEP06A22B)
Video Main (VEP03B96B)

Symptom : PCM Audio noise may recorded under low temperature.

Cause : Audio VCO PLL may not be locked under low temperature.

Remedy : To reduce the PCM Audio noise, the following modification is performed.

< VTR System Control >

1). PROM IC6006 software version is up-graded from 1.2 to 1.3.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC6006	VSI2334B	VSI2334C	VTR SYSCON PROM Ver. 1.3	1	

< TEST MENU >

CAM SYSCON IC3502 : 1.2 098A
CAM SYSCON IC3505 : 1.2 D423
* VTR SYSCON IC6006 : 1.3 96B0

*** Note ***

1). **When PROM is replaced, PROM Socket Cover must be replaced to new one at the same time as follows.**

2). **When PROM is replaced, MENU setting is returned to factory setting. If the MENU setting is returned to user setting, MENU data is saved to IC CARD before replacement of PROM.**

Regarding above method, please refer to the Technical Bulletin No. VSD9610SB614.

< Video Main >

1). Resistor R71 is changed from 0Ω to 1.5KΩ on the component side as shown in figures 1 and 2.

2). Resistor R70 (VRT0145) is added between R71 and R73 (GND side) on the component side as shown in figures 1 and 2.

*** Note *** After this modification, 6-1. AUDIO VCO Adjustment is required. Please refer to the Service Manual Page 4-26.

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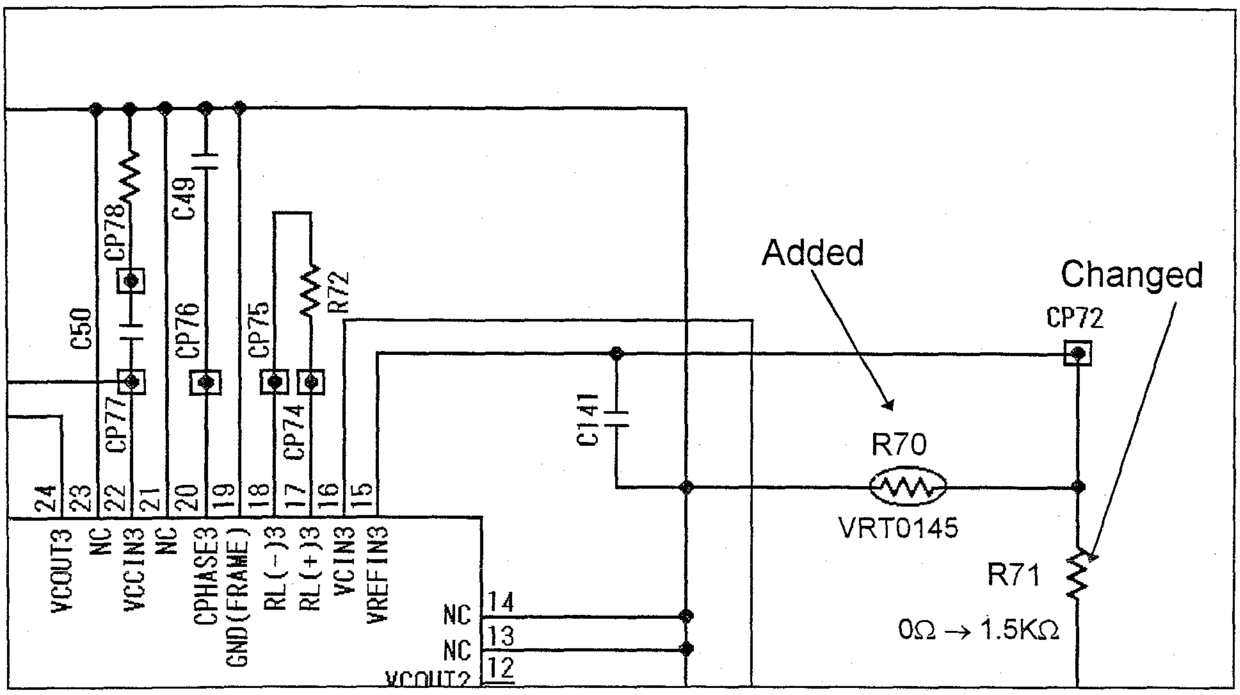
Part Number

Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
R70	---	VRT0145	THERMISTER	0→1	
R71	ERJ3GEY0R00	ERJ3GEYJ152	M. RESISTOR CH 1/16W 1.5K	1	

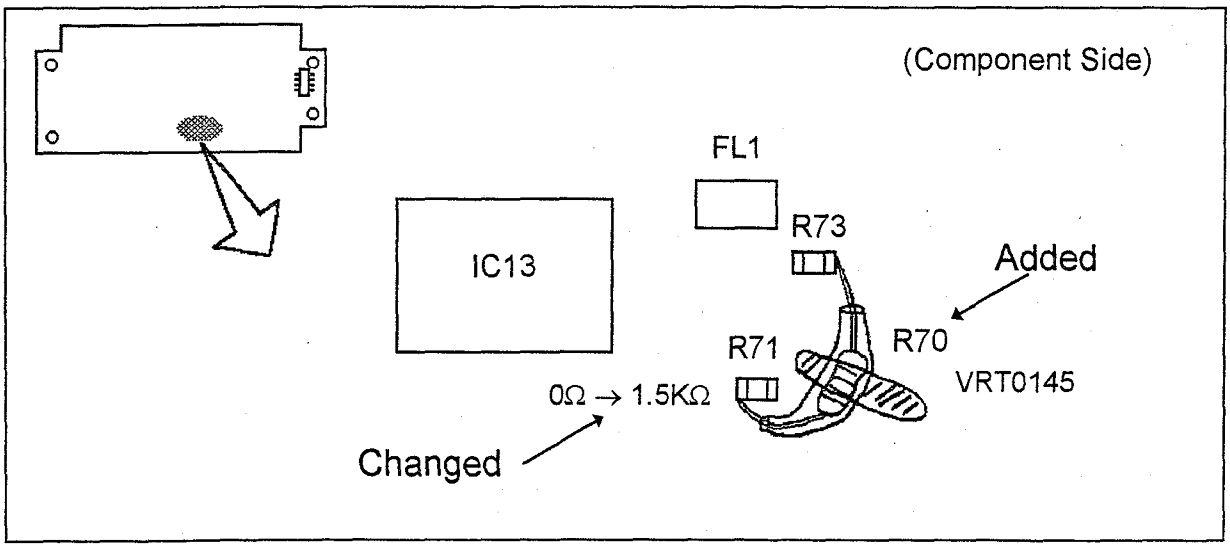
Video Main (2/7) Schematic Diagram



C50
CP78
C49
CP76
CP75
R72
CP77
CP74
C141
Added
Changed
CP72
R70
VRT0145
R71
0Ω → 1.5KΩ
24
23
22
21
20
19
18
17
16
15
VCOUT3
NC
VCCIN3
NC
CPHASE3
GND(FRAME)
RL(-)3
RL(+)3
VCIN3
VREFIN3
NC
14
13
NC
12
VCOUT2

Fig. 1 Page 2-62 (E-8)

Video Main P.C.Board (VEP03B96B)



(Component Side)
FL1
IC13
R73
Added
R71
R70
VRT0145
0Ω → 1.5KΩ
Changed

Fig. 2 Page 3-12 (B-1)

+V 17728 + V 17729 ✓

Order No. VSD9710SB648

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of QUAD Adjustment

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	49	VSD9606M501A/B	D7TKA0001

Board : Camera ENC (VEP23276B)
Video I/F (VEP03D53A)

To have a margin to capacitor for QUAD Adjustment, the following modification is performed.

< Camera ENC >
1). Capacitor C3026 is changed from 50V/10pF to 50V/6pF on the foil side.

Part Number					
Ref. No.	Original Part No.	New Parf No.	Part Name & Descriptions	Pcs	Remarks
C3026	ECUX1H100DCV	ECUX1H060DCV	C. CAPACITOR CH 50V 6P	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C3026	2-26	F-4 (3/7)	3-7	A-2 (F)

< Video I/F >
1). Capacitor C639 (50V/10pF) is deleted from the component side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C639	ECUX1H100DCV	—	C. CAPACITOR CH 50V 10P	1→0	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C639	2-37	F-6 (6/7)	3-9	B-2 (C)

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10212TE4757

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v17728 + v17725 ✓
v19646 ✓ v20164 ✓

Order No. VSD9710SB650

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Cleaning Solenoid Motion Sound

Please use this supplement together with the Service Manual as follows :			
Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	51	VSD9606M501A/B	F7TKA0001
AJ-D800E/EN	2	VSD9708M606A/B	F7TKA0001

Board : Servo (VEP02437B)

To decrease the motion sound of the Cleaning Solenoid, power supply voltage of the Cleaning Solenoid is changed from UNREG to 10.5V. The following modification is performed.

1). Resistor R749 (1/8W,0Ω) is deleted from the foil side.

2). Resistor R750 (1/8W,0Ω) is added to no mounted pattern of the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
R749	ERJ8GEY0R00	---	M. RESISTOR CH 1/8W 0	1→0	
R750	---	ERJ8GEY0R00	M. RESISTOR CH 1/8W 0	0→1	

AJ-D700

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
R749	2-53	D-7 (7/9)	3-11	B-4 (F)
R750	2-53	D-7 (7/9)	3-11	B-4 (F)

AJ-D800

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
R749	SCM-59	D-7 (7/9)	CBA-11	B-4 (F)
R750	SCM-59	D-7 (7/9)	CBA-11	B-4 (F)

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V.9728 + V.9729 ✓

Order No. VSD9710SB651

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Software Version Up Grade

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	52	VSD9606M501A/B	F7TKA0001

Board : VTR System Control (VEP06A22B)

The following software has been up-dated to add the functioning of the VTR.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC6006	VSI2334C	VSI2334D	VTR SYSCON PROM Ver. 1.4	1	

< TEST MENU >

CAM SYSCON IC3502 : 1.2 A807
CAM SYSCON IC3505 : 1.2 D695
* VTR SYSCON IC6006 : 1.4 8EC0

*** Note ***

1). Regarding below method, please refer to the Technical Bulletin No. **VSD9610SB614**.
   - a). When PROM is replaced, PROM Socket Cover must be replaced to new one at the same time as follows.
   - b). When PROM is replaced, MENU setting is returned to factory setting. If the MENU setting is returned to user setting, MENU data is saved to IC CARD before replacement of PROM.

2). The hardware modification of the VTR Main Board must be required since the following software version. (CAM SYSCON/1.2, VTR SYSCON/1.3). When the software is up-graded this time, please confirm the P.C. Board. If the P.C. Board is not modified, the hardware modification must be performed. Please refer to the Technical Bulletin No. **VSD9705SB643**.

Symptom : When the two units (AJ-D700) are set to Time Code Slave Lock and GENLOCK and then go to REC mode, the REC mode is suddenly released.

Cause : When the Time Code Slave Lock and GENLOCK are set simultaneously, there may be a communication error between System Control and Servo.

Remedy : To prevent it, PROM IC6006 software version is up-graded from 1.3 to 1.4.

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V19646 + V20164

Order No. VSD9710SB656

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Change of Screws

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	59	VSD9606M501A/B	G7TKA0001
AJ-D800E/EN	9	VSD9708M606A/B	G7TKA0001

Board : Video I/F (VEP03D53A)
VTR System Control (VEP06A22B) - AJ-D700
VTR System Control (VEP06A22C) - AJ-D800
Camera ENC (VEP23276B)
Camera SYNC (VEP23277B) - AJ-D700
Camera SYNC (VEP23446B) - AJ-D800
Camera System Control (VEP26074C)
Camera System Control (VEP26074D)

When the Shield Plate is fixed with the screws, the Shield Plate may be deformed. To prevent it, the screws are changed from XSN2+6 to XSB2+6.

Video I/F Board (VEP03D53A)

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
	XSN2+6	XSB2+6	SCREW	3	

VTR System Control Board (VEP06A22B/C)

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
	XSN2+6	XSB2+6	SCREW	2	

Camera ENC Board (VEP23276B)

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
	XSN2+6	XSB2+6	SCREW	2	

Camera SYNC Board (VEP23277B/VEP23446B)

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
	XSN2+6	XSB2+6	SCREW	2	

Camera System Control Board (VEP26074C/D)

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
	XSN2+6	XSB2+6	SCREW	2	

TE4859

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V19928 + V19929 ✓

Order No. VSD9711SB662

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Software Version Up Grades

Please use this supplement together with the Service Manual as follows :			
Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	66	VSD9606M501A/B	I7TKA0001

Board : Camera System Control (VEP26074C)
VTR System Control (VEP06A22B)

The following software has been up-dated to add the functioning of the VTR.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC3502	VSI2241B	VSI2241C	CAM SYSCON PROM Ver. 1.3	1	
IC3505	VSI2242B	VSI2242C	CAM SYSCON PROM Ver. 1.3	1	
IC6006	VSI2334D	VSI2334E	VTR SYSCON PROM Ver. 1.5	1	

< TEST MENU >

* CAM SYSCON IC3502 : 1.3 912D
* CAM SYSCON IC3505 : 1.3 ECC4
* VTR SYSCON IC6006 : 1.5 5BC5

*** Note ***

1). Regarding below method, please refer to the Technical Bulletin No. **VSD9610SB614.**
  a). When PROM is replaced, PROM Socket Cover must be replaced to new one at the same time as follows.
  b). When PROM is replaced, MENU setting is returned to factory setting. If the MENU setting is returned to user setting, MENU data is saved to IC CARD before replacement of PROM.
2). The hardware modification of the VTR Main Board must be required since the following software version. (CAM SYSCON/1.2, VTR SYSCON/1.3). When the software is up-graded this time, please confirm the P.C. Board. If the P.C. Board is not modified, the hardware modification must be performed. Please refer to the Technical Bulletin No. **VSD9705SB643.**

< Additional Function >

1. < FUNCTION 2/5 Screen >

1. S.IRIS SW
   1-1. S.IRIS SW OFF can be available.
   When S.IRIS SW is pressed, S.IRIS/30dB/OFF can be selected.
   1-2. When the mode sets to OFF, S.IRIS SW is ignored in spite of pressing.
   1-3. When the GAIN SW (L/M/H) is switched, the unit accepts the GAIN SW mode in spite of FORCE 30dB mode (Menu 30dB/S. IRIS SW ON).

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2. Synchro Scan Select function is changed.
When the S.SCAN mode of Function Menu 2/5 is ON, VF DISPLAY of Option Menu is SPECIAL and S.SCAN SW of Front is ON pressing the MODE CHECK SW, the status of the MODE CHECK is still displayed. It is improved. When the status of the MODE CHECK is displayed although the MODE CHECK SW is OFF, it is not displayed.

```
        - FUNCTION 2/5 -

→SUPER V              : FRM 1
 FILTER INH           : OFF
 SHOCKLESS AWB        : NORMAL
 S.IRIS SW            : S.IRIS
 S. SCAN SEL          : ON   ⇦
```

Changed from OFF

Item	Variable Range	VF Display	Remarks
S. IRIS SW	S.IRIS 30dB **OFF**	ENG	Super iris (S.IRIS) / 30 dB / OFF switching
S.SCAN SEL	ON **OFF**	ENG	Synchro scan ON/OFF switching ON : S.SCAN speed can be varied by the SUPER IRIS/MODE CHECK switch. OFF : Normal mode

2. < SET UP CARD Screen >

1. The following Camera Menu data READ/WRITE ON/OFF select function is introduced.

```
        - SET UP CARD -

→READ (→CAM)
 WRITE (→CARD)
 CARD CONFIG.
 ID READ / WRITE    :  ON
 FUNCTION 1 - 2 R/W :  ON  ⇦   Added
 L/M/H SET R/W      :  ON  ⇦   Added
 LEVEL 1 - 6 R/W    :  ON  ⇦   Added
```

Item	Variable Range	VF Display	Remarks
FUNC 1~2 R/W	ON OFF	USER ENG	READ/WRITE for FUNCTION1 and FUNCTION2 is switched ON or OFF when data is read from or written on the SET UP CARD. ON : READ/WRITE is enabled. OFF : READ/WRITE is disabled.
L/M/H SET R/W	ON OFF	USER ENG	READ/WRITE for LOW SETTING, MID SETTING and HIGH SETTING is switched ON or OFF when data is read from or written on the SET UP CARD. ON : READ/WRITE is enabled. OFF : READ/WRITE is disabled.
LEVEL 1~6 R/W	ON OFF	USER ENG	READ/WRITE for LEVEL 1/6, 2/6, 3/6, 4/6, 5/6 and 6/6 is switched ON or OFF when data is read from or written on the SET UP CARD. ON : READ/WRITE is enabled. OFF : READ/WRITE is disabled.

3. AWB NG Warning Function

1. When the AWB SW is turned ON (START) while AWB is NG, the following Warning Display is indicated.
   * Note * When the AWB is changed from NG position to regular position (FLT 1/2/3/4), this Warning Display is turned OFF.

```
AWB NG
CHECK FILTER
```

4. < OPTION Menu>

*** This Menu is only Engineer Security purpose, so it is not written on the Operating Instructions.**

This Menu is opened as following Setting.
Set the Menu SW pushing [SHIFT/ITEM] key and [PAGE SW] key simultaneously.

```
      - OPTION MENU -

 →ENG SECURITY   : OFF
  TONE MODE      : NORMAL
  METER SELECT   : CH1
  VF DISPLAY     : NORMAL
  TC OUT         : TCG
  TCG SET        : RESET
  BATT WARNING   : ON
```

⇧ Added

Item	Variable Range	VF Display	Remarks
VF DISPLAY	NORMAL SPECIAL	ENG	NORMAL : Status which selected by the Menu is displayed in the View Finder. SPECIAL : Status which selected by the Menu is displayed in the View Finder only when the MODE CHECK SW is pressed.
TC OUT	TCG TCG/TCR	ENG	TCG : TCG is only output. TCG/TCR : TCR is output during V-V mode. TCG is output during E-E mode. * **Note * When the TCR is output as it is, it is output adding two frames because it is two frames delay than picture.**
TCG SET	RESET HOLD	ENG	RESET : REGEN is performed when the unit goes to REC mode after power is turned from OFF to ON in spite of TCG setting. HOLD : REGEN is not performed when the unit goes to REC mode after power is turned from OFF to ON with TCG setting
BATT WARNING	ON OFF	ENG	ON : When the ALARM, TALLY LED is ON during TAPE NEAR END mode, they are ON as it is. OFF : When the ALARM, TALLY LED is ON during TAPE NEAR END mode, they are OFF by MODE CHECK SW is ON.

1. VF DISPLAY NORMAL/SPECIAL select function is introduced.
   Status display in the View Finder is only displayed when the MODE CHECK SW is pressed.
2. TCG/TCR Output function from TC OUT of the Rear Side Panel is introduced.
3. TCG RESET/HOLD select function is introduced.
   When the unit goes to REC mode after the power is turned from OFF to ON with TCG setting, the REGEN is performed in spite of TCG setting. To prevent it, this function is added.
4. Battery Warning ON/OFF select function is introduced.
   When the ALARM and TALLY END are ON during TAPE NEAR END mode, they can be turned OFF by the MODE CHECK SW is ON.

< Improvement of Performance >

1. < LEVEL 3/6 Screen >

1. Variable range of WHITE CLIP LEVEL is changed from “238 ~ 254” to “214 ~ 254”.

```
        - LEVEL 3/6 -

→M. PED            : +006
 MANUAL KNEE       : ON
 KNEE POINT        : 197
 KNEE SLOPE        : 24    ⇦  Changed from 12
 WHITE CLIP        : ON
 WHITE CLIP LEVEL  : 244   ⇦  Changed from 254
```

Item	Variable Range	VF Display	Remarks
KNEE SLOPE	0 : **24** 25	ENG	Manual knee inclination setting.
WHITE CLIP LEVEL	**214** : **244** : 254	ENG	White clip level setting.

2. < LEVEL 5/6 Screen >

1. Variable range of MATRIX is changed from “-25 ~ +25” to “-31 ~ +31”.

3. < LEVEL 6/6 Screen >

1. Normal 2 mode on the A. IRIS MODE is introduced.

```
        - LEVEL 6/6 -

→H PHASE COARSE   : 07
 H PHASE FINE     : 128
 SC PHASE COARSE  : 0
 SC PHASE FINE    : 128
 A.IRIS LEVEL     : 063
 A.IRIS PEAK / AVE: 075
 A.IRIS MODE      : NORM1   ⇦  Added
 S.IRIS LEVEL     : 072
```

Item	Variable Range	VF Display	Remarks
A. IRIS MODE	NORM1 NORM2 CENTR	ENG	Audio iris mode selection NORM1 : Light metering over entire screen (except for edges). **NORM2 : Light metering over entire screen (except for top).** CENTR : Light metering which is focused solely on the screen center. The iris value which matches the subject is set for this mode even when the brightness of the subject at the center differs from that at the screen edges.

4. VF TAPE REMAIN Display Change
   When the tape remaining is more than 30 minutes, it can be displayed till 60 minutes in the View Finder as follows.

Current Display	F-30, 30-25, ,,,,,, 5-0
New Display	F-60, 60-55, ,,,,,, 5-0

   * Note * TAPE REMAIN on the Front LCD is not changed. When the tape remaining is more than 30 minutes, it displays “FULL”.

5. VF IRIS Display Change
   As the IRIS Display in the View Finder falls on the one character of the Audio Level Meter, it is changed as follows.

Number of Character	5 numbers of character → **4 numbers of character**
Character Change	“CLOSE” → “**_ _ _ C**” (Because only CLOSE is 5 numbers of characters)

6. Improvement of TC DF/NDF Mode Change
   When TC MODE on the Menu is selected "DF" and then LCD Display on the Front Panel indicates CTL or UB, the unit goes to NDF mode. It is improved.

7. Improvement of PHANTOM MIC Power ON/OFF
   When the AUDIO IN SW (CH1/CH2) on the Front Panel is set to LINE, the PHANTOM MIC power is still turned ON. To prevent it, when the AUDIO IN SW (CH1/CH2) on the Front Panel is set to LINE, the PHANTOM MIC power is turned OFF.

8. ANTON BATT (DIGITAL) Voltage Detect Level Change
   The time until UNDER CUT functions is too long after the BATT NEAR END WARNING of the ANTON BATT (DIGITAL) is displayed. It is improved.

9. Improvement of Filter Display
   When the Optical filter is NG position, FLT4 is displayed. It is improved.

17728
17729 ✓
20161
19646

Order No. VSD9712SB666

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Introduction of Auto EQ/RF Adjustment System

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D700E/EN	70	VSD9606M501A/B	---
AJ-D800E/EN	21	VSD9708M606A/B	---

In order to increase serviceability of EQ/RF Adjustment, New Auto EQ/RF Adjustment System has been introduced.

1. Preparation

To perform the EQ/RF adjustment automatically, the following adjustment system should be prepared.

1-1. Special Tools

No.	Current Part No.	New Part No.	Tool Name	Remarks
1	VFK1163	VFK1163	EQ Adj. Tool	See Paragraph 2-2
2	VFK1158	VFK1158A	B.E.R. Counter	See Paragraph 2-1
3	VFK1160A	VFK1160B	Auto EQ Adj. Software	
4	VFK1162A	Same as current	EVR Software	
5	VFKW1000AA	Same as current	EVR I/F Box	
6	VFKW1000C	Same as current	EVR RS-232C Cable	
7	VFK1180	Same as current	EVR Sub I/F Board	
8	VFK1187	Same as current	EVR Cable	
9	VFK1185	Same as current	B.E.R. Cable	
10	VFM3580KM	Same as current	Alignment Tape (1)	NTSC System
11	VFM3680KM	Same as current	Alignment Tape (1)	PAL System
11	VFK1300	Same as current	A/D board	DAQ-12

▨ : Modification or new type is needed.

1-2. Measuring Equipment

No.	Name of Equipment	Remarks
1	Personal Computer	IBM PC/AT Compatible
2	Monitor TV	
3	DC Power Supplier	DC 6V
4	DC Power Supplier	DC 8.5-12V
5	Oscilloscope	More than 100MHz

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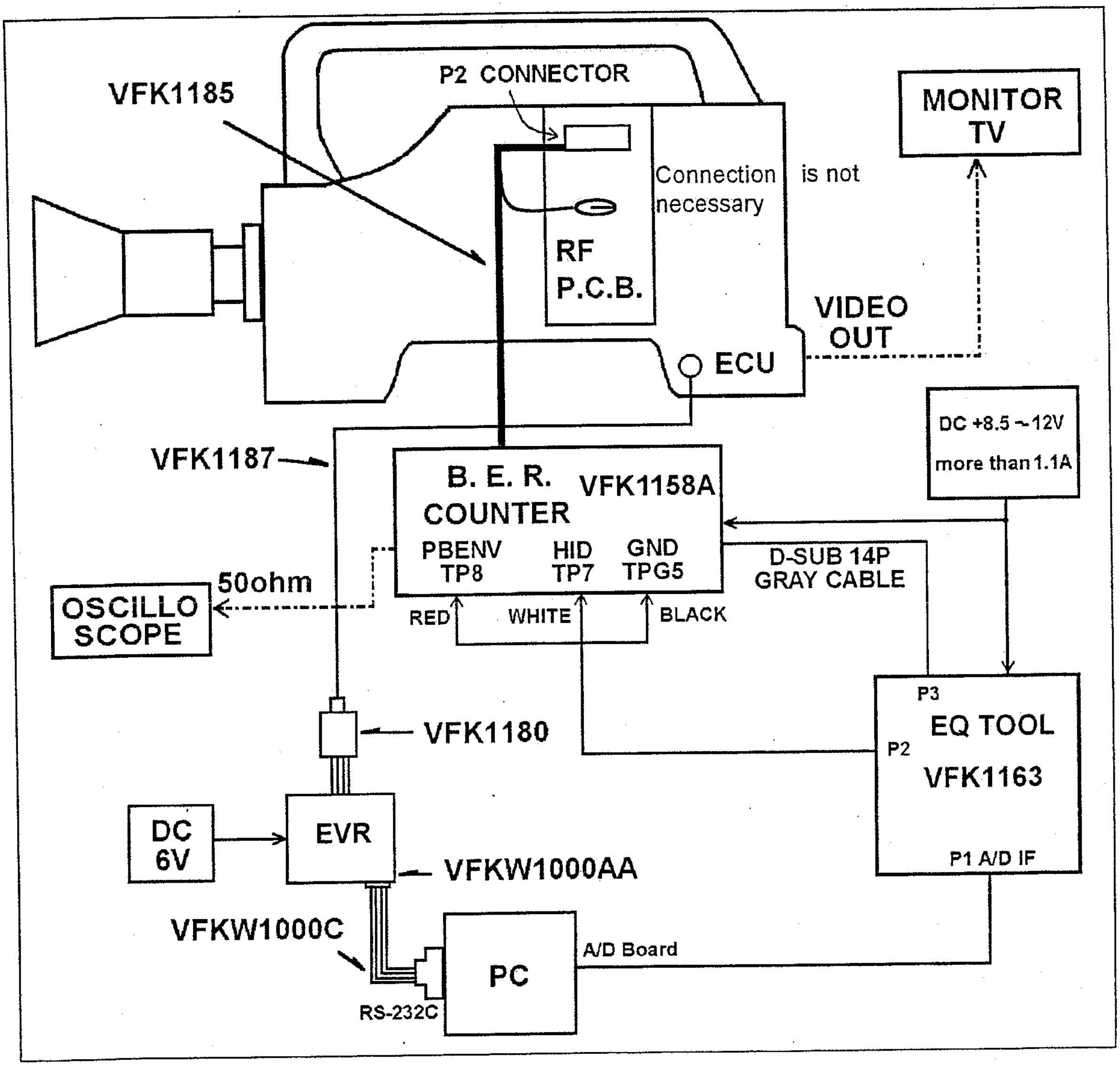
1-3. System Diagram



VFK1185
P2 CONNECTOR
Connection is not necessary
MONITOR TV
RF P.C.B.
VIDEO OUT
ECU
VFK1187
B. E. R. COUNTER
VFK1158A
PBENV TP8
HID TP7
GND TPG5
DC +8.5 ~ 12V more than 1.1A
D-SUB 14P GRAY CABLE
OSCILLO SCOPE
50ohm
RED
WHITE
BLACK
P3
EQ TOOL
P2
VFK1163
VFK1180
DC 6V
EVR
VFKW1000AA
P1 A/D IF
VFKW1000C
PC
A/D Board
RS-232C

Fig. 1

2. Modification

2-1. VFK1158 (Current B.E.R. Counter)

When modifying the current B.E.R. Counter with modification kit VFK1158AKIT, the B.E.R. counter performs the same function as VFK1158A.

2-1-1. Modification Kit (VFK1158AKIT)

The modification kit consisted of the following items.

Part Name	Part No.	Quantity
Main P.C. Board	VFK1158KIT	1
Cable	---	1
Auto EQ Software	VFK1160B	1

2-1-2. Modification Procedure

1. Unscrew the 4 screws from the right and left panel (each 2 screws) and remove the Top Panel.

2. Remove the P.C. Board.
   1). Remove the 3 screws from the connector side on the Bottom Panel.
   2). Remove 4 screws from the Front Panel.
   3). Remove 3 screws from the LED side on the Main P.C. Board.
   4). Remove the Main P.C. Board from the front upper direction.
3. Remove IC4 from the socket on the original Main P.C. Board and insert it to the new Main P.C. Board (VFK1158AKIT). It is difficult to remove IC4, so use a metal sharp sticker and remove the IC slowly.
4. Set the new Main P.C. Board (VFK1158AKIT) with IC4 as reverse procedures of removal.
5. The Top Panel can not be set, because the 14Pin Connector is added. If the Top Panel must be used, bend the side panel at the connector side or cut it.

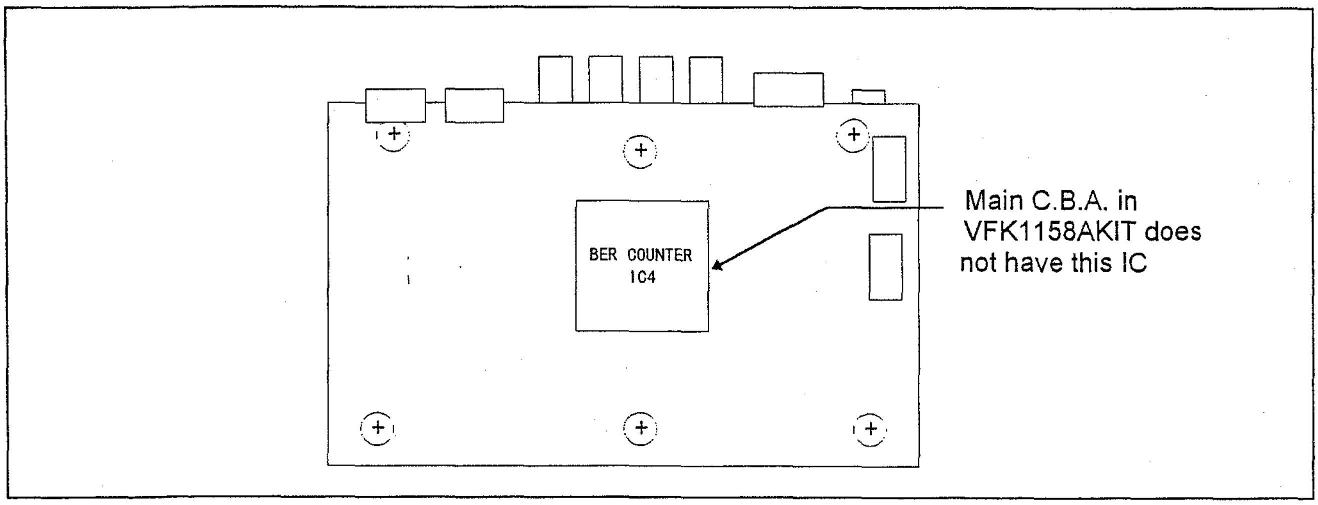


Fig. 2

2-2. VFK1163 (EQ Tool)

VFK1158A or modified VFK1158 (with VFK1158AKIT) needs to be supplied –5V from VFK1163 via pin #1 of 15Pin cable, so VFK1163 should be modified for this reason.
Since July, '97 production of VFK1163, the following modification has been introduced and mark "A" has been added on the serial number plate

2-2-1. Modification Procedure

1. Unscrew 4 screws and remove the Top Cover.
2. Add a jumper wire between pin # 1 of P3 and (-) pole of capacitor C8 as shown below.
3. Install the Top Cover as reverse procedures of removal.

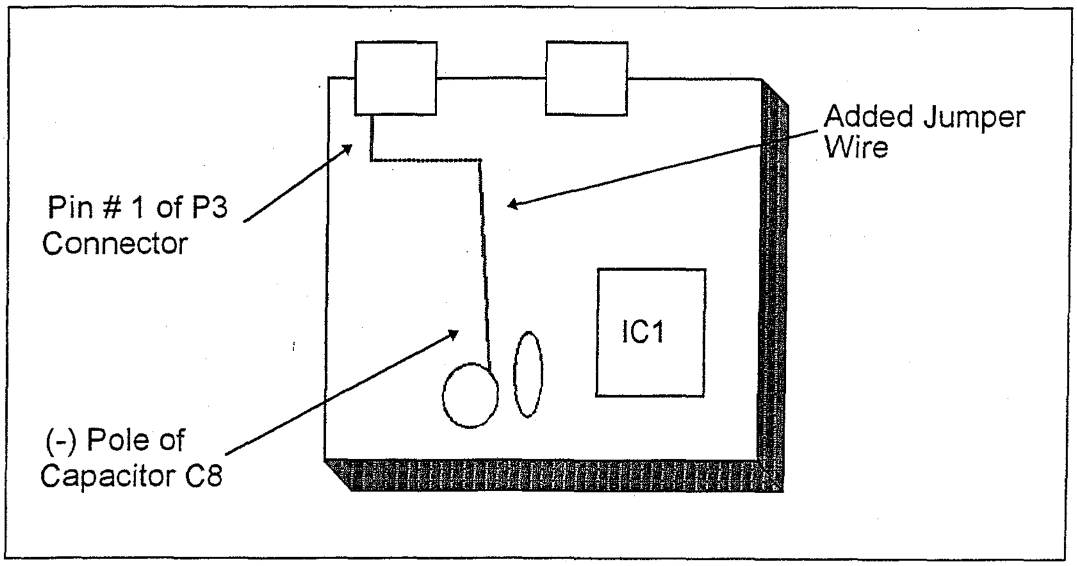


Fig. 3

3. Adjustment Procedures

8. RF Adjustment

8-1. System Hook UP and Setting

- **System Hook UP**

1. Connect the Camera with the Auto EQ/RF Adjustment System as shown Figure 1.
2. IC connection clip cable from the VFK1185 is not necessary (open).
3. Set the switches on the B.E.R. counter as follows.
   ERROR COUNT SW : ON
   CH SELECT SW : AUTO
   (L/R : Any one)

- **Menu Setting on Camera Recorder**

1. Open the operation panel.
2. Press [SHIFT], [+] and [-] buttons, and set the MENU switch to the SET position.
3. Set the menu setting as follows:
   PAGE : SERVICE ADJ.
   ECU CONNECT :EVR
   CONCEAL :OFF
   INNER ECC :OFF
   OUTER ECC :OFF
   SERVO MODE :ATF
4. After the above menu setting, close the menu mode.

- **Auto Adjustment System Normalization (Calibration)**

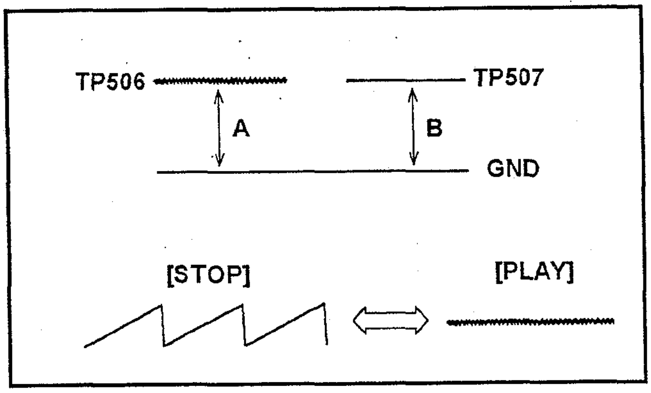
The system normalization (calibration) should be performed when using the adjustment system at the first time (after the completion of the system hook up) or changing the A/D board, PC or EQ tool.
Also, we recommend to perform it regularly
The auto adjustment system normalization procedure, please refer to paragraph 4. In this supplement service manual.

8-2. PLL VCO Adjustment

BOARD	RF
SPEC.	A=B=2.0±0.1V
TEST	TP506, TP507
ADJUST	EVR
MODE	PLAY
TAPE	Color Bar
M.EQ	Oscilloscope, EVR

EVR Setting
CMD : 02 DATA : **7A** ADR : **0B**

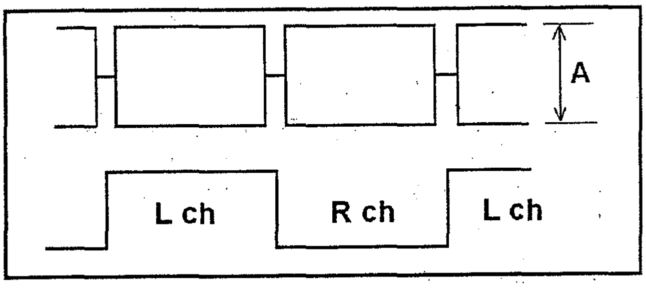
1. Monitor the waveform at **TP506** and **507** in the DC mode.
2. Press the [→] or [←] key in the EVR so that the levels A and B are the same.



8-3. R/P Envelope Level Confirmation

BOARD	RF
SPEC.	A≧70mV
TEST	R/P ENV,HSW (B.E.R. Counter) (50Ω terminated)
MODE	PLAY
TAPE	Color Bar
M.EQ	Oscilloscope

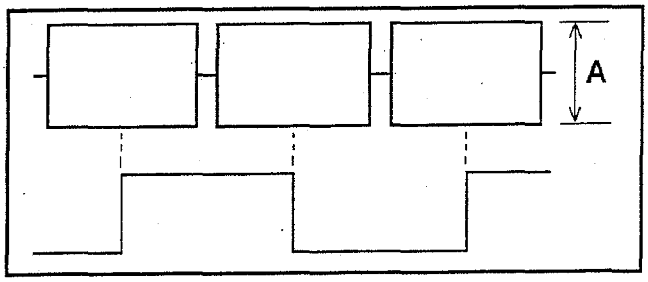
1. Confirm that the waveform is as flat.



8-4. PB Envelope Level Adjustment

BOARD	RF
SPEC.	100±10mV
TEST	PB ENV, HSW(B.E.R. Counter) (50Ω terminated)
ADJUST	VR400(PB L), VR401(PB R)
MODE	PLAY
TAPE	Color Bar
M.EQ	Oscilloscope

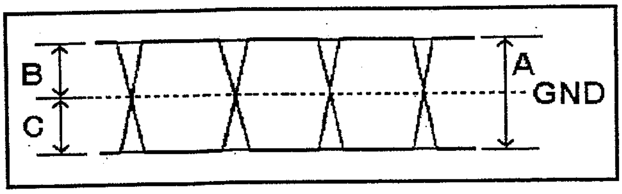
1. Confirm that the waveform is as shown in the figure below.
2. Adjust the **VR400**(L ch) and **VR401**(R ch) so that the level A is within the specification.



8-5. HSE Input Confirmation

BOARD	RF
TEST	TP201, TP300(Trigger)
ADJUST	VR200(DUTY)
MODE	REC
TAPE	Blank Tape
M.EQ	Oscilloscope

1. Set the oscilloscope to AC mode.
2. Monitor the **TP201** and confirm that A is 1.3 ± 0.1V.
3. Confirm that B and C are the same.
4. If necessary, adjust the **VR200** slightly.



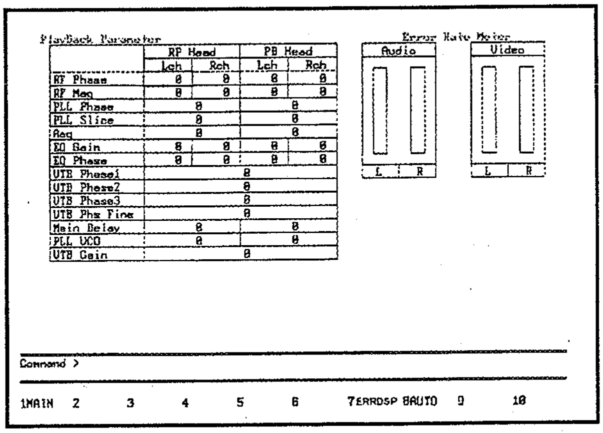
8-6. PB Equalizer Adjustment(Auto)

Menu Setting

1. Open the operation panel.
2. Pressing [SHIFT], [+] and [-] buttons, set the MENU switch to the SET position.
3. Set the menu as follows:
   PAGE : SERVICE ADJ.
   - ECU CONNECT :EVR
   - CONCEAL :OFF
   - INNER ECC :OFF
   - OUTER ECC :OFF
   - SERVO MODE :ATF
4. After the above setting, close the menu.

Auto Adjustment Software Boot UP

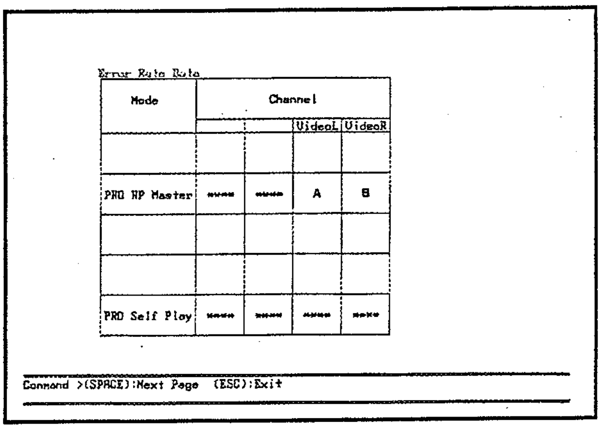
1. Copy the all files contained in floppy disk (VFK1160B) to a directory of hard disc drive. (ex. C:¥DVCEQ)
2. Execute DVCRF.EXE file on DOS command prompt condition. (ex. "C:¥DVCEQ¥DVCRF")
3. Select (2) AJ-D700 in DVCPRO MODEL SELECT.
4. Select (1) NORMAL in PROGRAM SELECT.
5. Wait about 20 seconds for the parameter loading. To short cut this 20 seconds, confirm the power switch of the all equipment are turned ON and then press the "ENTER" key.
6. Personal Computer (PC) asks "Do you transfer BOOT PROGRAM ?" then once turn the power switch of the EVR I/F box OFF and ON, and then select the [Y].
7. PC asks whether any error has happened or not.
8. MAIN MENU is available.
   F1 MENU
   1. PB Adjustment
   2. REC Adjustment
   3. Result
   4. File
   5. Restart
   6. End
9. Select 1.PB Adjustment.
10. Select whether downloading data from VTR or not.
11. Press F8 to select the AUTO.
12. Confirm that there is no tape in the VTR and press the [ENTER] key.
13. PC asks "Initial Adjust ?". Select the [Y].
14. Select 1. All Adjust in PB Auto Menu.
15. Insert the Alignment tape and play back the color bar portion according to the instruction on the display.
16. During the auto adjustment don't touch the VTR,TOOL and PC.
    Please note that the audio error rate is not displayed in the auto adjustment.



PlayBack Parameter

	RF Head		PB Head	
	Lch	Rch	Lch	Rch
RF Phase	0	0	0	0
RF Mag	0	0	0	0
PLL Phase	0		0	
PLL Slice	0		0	
Agc	0		0	
EQ Gain	0	0	0	0
EQ Phase	0	0	0	0
VTB Phase1	0			
VTB Phase2	0			
VTB Phase3	0			
VTB Phs Fine	0			
Main Delay	0		0	
PLL VCO	0		0	
VTB Gain	0			

```
Command >
1MAIN  2    3    4    5    6    7ERRDSP 8AUTO  9    10
```



Error Rate Data

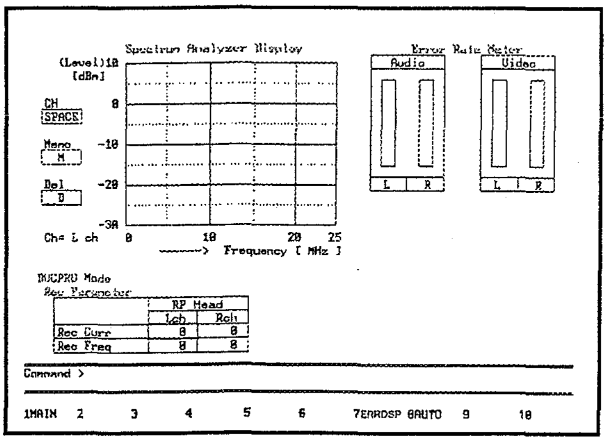
Mode	Channel			
			VideoL	VideoR
PRO RP Master	****	****	A	B
PRO Self Play	****	****	****	****

```
Command >(SPACE):Next Page  (ESC):Exit
```

17. Adjustment may complete after 5-6 minuets.
18. Error rate is measured and displayed.
19. Confirm that the data A and B are green color. If there is any red color, try the same adjustment again after cleaning of the video head and tape transportation.

8-7. Rec. Curr. & Freq. Adjustment

1. Open the MAIN MENU according to the same procedure as the PB Equalizer Adjustment.
2. Select 2. REC Adjustment in the MAIN MENU.
3. PC asks whether download the VTR data from the VTR or not.
4. Select [Y] so that the VTR adjustment data are saved in to the PC.
5. Press F8 to select the AUTO.
6. Select 1.Adjust start in the sub menu.
7. Insert the alignment tape and play back the color bar portion according to the instruction on the display.
8. After memorizing the playback data, insert a blank tape and start a recording according to the instruction on the display.
9. During the adjustment, don't touch the VTR and PC adjustment system.
10. During the adjustment, audio error rate in not displayed.



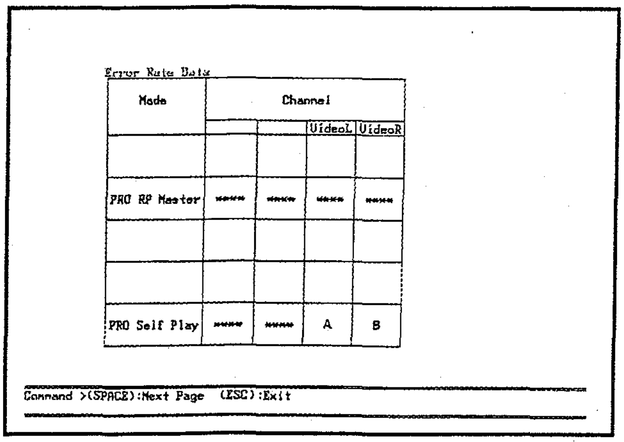
DVCPRO Mode
Rec Parameter

	RF Head	
	Lch	Rch
Rec Curr	8	8
Rec Freq	8	8

Command >

1MAIN 2 3 4 5 6 7ERRDSP 8AUTO 9 10

11. Rewind the recorded tape which was recorded on the blank tape and play back the recorded portion according to the instruction on the display.
12. The error rate is measured and displayed.
13. Confirm that the data A and B are green color.



Error Rate Data

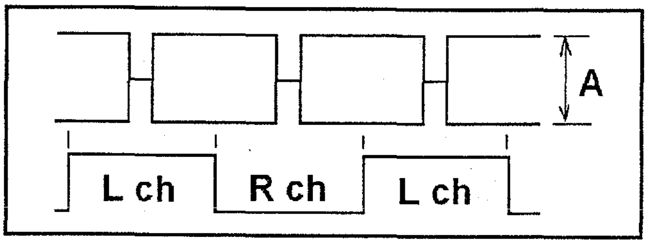
Mode	Channel			
			VideoL	VideoR
PRO RP Master	*****	*****	*****	*****
PRO Self Play	*****	*****	A	B

Command >(SPACE):Next Page (ESC):Exit

8-8. Confidence PB Adjustment

BOARD	RF
SPEC.	100±10mV
TEST	PB ENV, HSW (B.E.R. Counter) (50Ω terminated)
ADJUST	VR400(PB L), VR401(PB R)
INPUT	Internal Color Bar
MODE	REC
TAPE	Blank Tape
M.EQ	Oscilloscope

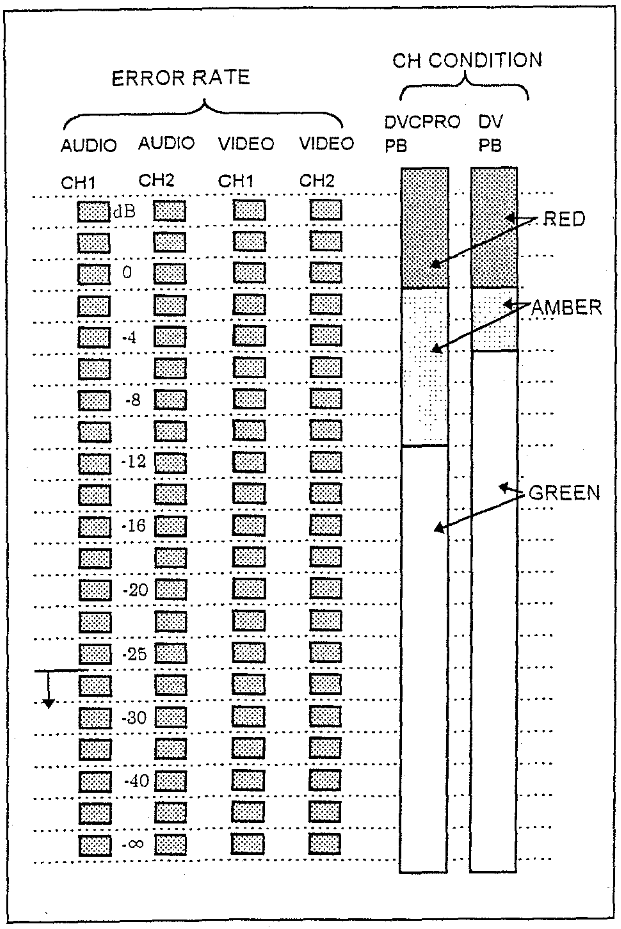
1. Place the unit in the confidence PB mode.
2. Adjust **VR400** *and* **401** *so that the level A is within the specification.*



8-9. Final Confirmation

BOARD	RF
TEST	VIDEO OUT
INPUT	Internal Color Bar
MODE	REC, PLAY
M.EQ	B.E.R. Counter, Monitor TV

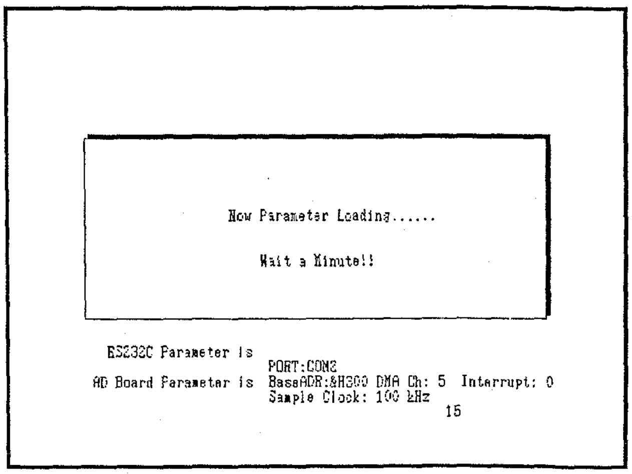
1. Record the internal color bar signal.
2. Play back the recorded portion.
3. Confirm that the error rate is less than **250** on the L and R channels.
4. Play back the recorded portion on a studio editing DVCPRO and confirm that the error rate is less than A as shown in the figure below..
5. If it is not less than A, readjust Rec Current and Frequency Response.
6. Set the menu as follows:
   PAGE : SERVICE ADJ.
   INNER ECC :ON
   OUTER ECC :ON
7. Confirm that there is no error in the playback picture.



4. Important Notice

4-1. Auto Adjustment System Normalization (Calibration) Procedure

1. Boot up the auto adjustment system according paragraph 8-6.

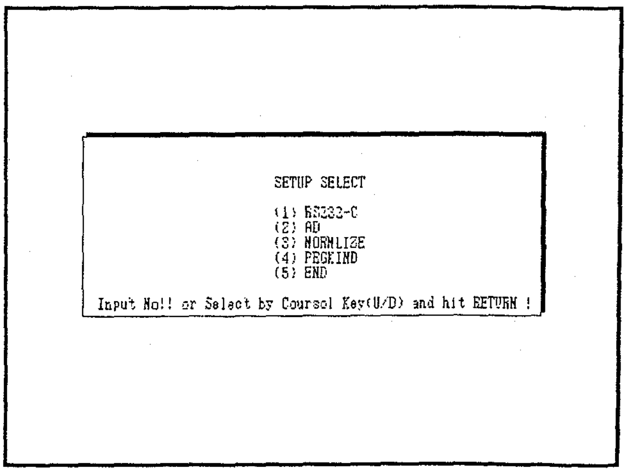


```
Now Parameter Loading......

Wait a Minute!!

RS232C Parameter Is
                        PORT:COM2
AD Board Parameter is   BaseADR:&H300 DMA Ch: 5  Interrupt: 0
                        Sample Clock: 100 kHz
                                                  15
```

2. During parameter count down, press the "F2" as shown in figure below.
3. Select "(3) NORMALIZE" when the display shows "SET UP SELECT as shown the figure below.

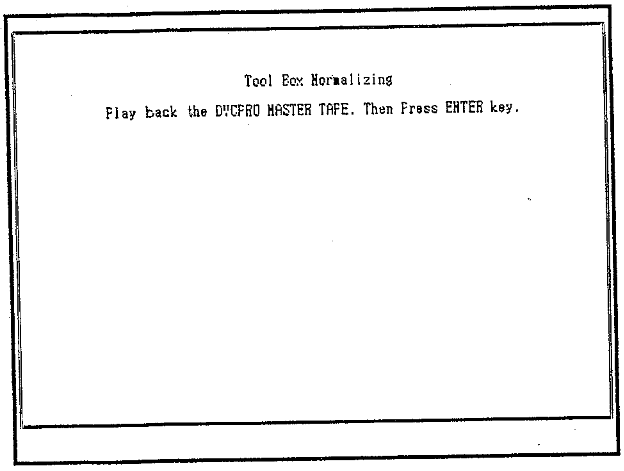


```
SETUP SELECT

(1) RS232-C
(2) AD
(3) NORMLIZE
(4) PEGKIND
(5) END

Input No!! or Select by Coursol Key(U/D) and hit RETURN !
```

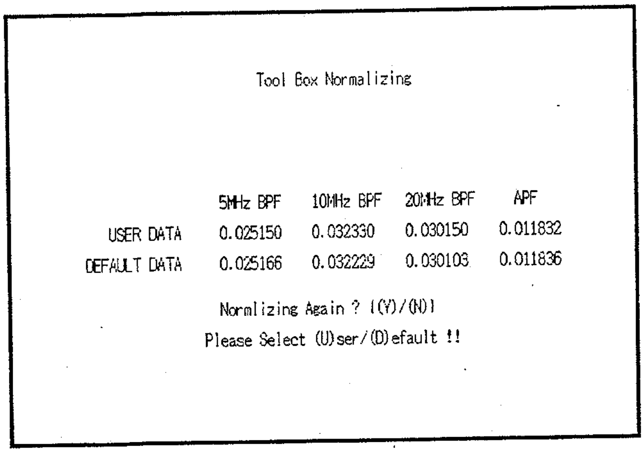
4. When display shows “TOOL BOX NORMALIZING”, play back the color bar portion of the alignment tape and press the ENTER key.



```
                    Tool Box Normalizing

   Play back the DVCPRO MASTER TAPE. Then Press ENTER key.
```

5. Wait for the completion of USER DATA measurement. When measurement is completed, the display shows the USER DATA and DEFAULT DATA at the upper side of the display.
6. Compare the USER DATA and DAFAULT DATA, and confirm that the difference is within ± 0.01 as shown in figure below.
7. The PC asks “NORMALIZING AGAIN?”



```
                      Tool Box Normalizing


                5MHz BPF    10MHz BPF   20MHz BPF     APF
   USER DATA    0.025150    0.032330    0.030150    0.011832
DEFAULT DATA    0.025166    0.032229    0.030103    0.011836

                  Normlizing Again ? [(Y)/(N)]
                Please Select (U)ser/(D)efault !!
```

8. If value is within the specification, press the “N” key.
9. The PC asks “PLEASE SELECT (U)ser/(D)efault”.
10. Press “U” to select the USER. This USER data becomes as the DEFAULT data from the next operation as shown in figure above.
11. If the value is not within the specification, confirm the connection of the adjustment system and quality of the alignment tape, and perform the above steps 7 and 8 again.
12. (“NORMALIZING AGAIN?”, press the “Y”)
13. If it is not improved after several times may be something wrong with the EQ tool.
14. When performing the Auto Adjustment System Normalization regularly under condition of the same combination of the PC, A/D Board and EQ Tool, the difference of USER DATA and DEFAULT DATA should be within ± 0.005.